



## 512K x 72 Synchronous Pipeline Burst ZBL SRAM

### FEATURES

- Fast clock speed: 150, 133, and 100MHz
- Fast access times: 3.8ns, 4.2ns, and 5.0ns
- Fast OE# access times: 3.8ns, 4.2ns, and 5.0ns
- High performance 3-1-1-1 access rate
- $3.3V \pm 5\%$  power supply
- I/O supply voltage 3.3V or 2.5V
- Common data inputs and data outputs
- Byte write enable and global write control
- Six chip enables for depth expansion and address pipeline
- Internally self-timed write cycle
- Burst control pin (interleaved or linear burst sequence)
- Automatic power-down for portable applications
- Commercial, industrial and military temperature ranges
- Packaging:
  - 152 PBGA package 17 x 23mm

### BENEFITS

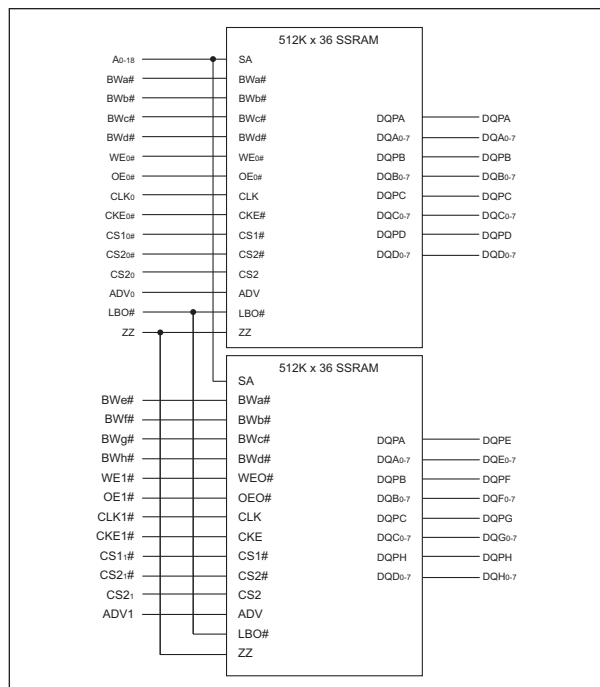
- 30% space savings compared to equivalent TQFP solution
- Reduced part count
- 24% I/O reduction
- Laminate interposer for optimum TCE match
- Low Profile
- Reduce layer count for board routing
- Suitable for hi-reliability applications
- User configurable as 1M x 36 or 2M x 18
- Upgradable to 1M x 72 (contact factory for availability)

### DESCRIPTION

The WEDC SyncBurst - SRAM employs high-speed, low-power CMOS design that is fabricated using an advanced CMOS process. WEDC's 32Mb SyncBurst SRAMs integrate two 512K x 36 SSRAMs into a single BGA package to provide 512K x 72 configuration. All synchronous inputs pass through registers controlled by a positive-edge-triggered single-clock input (CLK). The ZBL or Zero Bus Latency Memory utilizes all the bandwidth in any combination of operating cycles. Address, data inputs, and all control signals except output enable and linear burst order are synchronized to input clock. Burst order control must be tied "High or Low." Asynchronous inputs include the sleep mode enable (ZZ). Output Enable controls the outputs at any given time. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation and provides increased timing flexibility for incoming signals.

\* Product is subject to change without notice.

### FUNCTIONAL BLOCK DIAGRAM





### PIN CONFIGURATION (TOP VIEW)

	1	2	3	4	5	6	7	8	9
<b>A</b>	-	ADV <sub>0</sub>	OE <sub>0</sub> #	DQb <sub>2</sub>	DQb <sub>4</sub>	DQb <sub>6</sub>	dn <sub>u</sub>	DQa <sub>6</sub>	DQa <sub>2</sub>
<b>B</b>	CKE <sub>0</sub> #	WE <sub>0</sub> #	DQb <sub>7</sub>	DQb <sub>5</sub>	DQb <sub>3</sub>	DQb <sub>0</sub>	DQa <sub>7</sub>	DQa <sub>3</sub>	DQa <sub>1</sub>
<b>C</b>	CLK <sub>0</sub>	CS <sub>20</sub> #	DQc <sub>2</sub>	DQpc	DQpb	DQb <sub>1</sub>	DQd <sub>7</sub>	DQa <sub>4</sub>	DQa <sub>0</sub>
<b>D</b>	BW <sub>a</sub> #	BW <sub>b</sub> #	DQC <sub>3</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	DQD <sub>6</sub>	DQA <sub>5</sub>	DQPA
<b>E</b>	BW <sub>c</sub> #	BW <sub>d</sub> #	DQC <sub>4</sub>	V <sub>ccq</sub>	V <sub>ccq</sub>	V <sub>ccq</sub>	DQD <sub>5</sub>	DQPD	ZZ
<b>F</b>	CS <sub>10</sub> #	CS <sub>20</sub>	DQC <sub>5</sub>	V <sub>ccq</sub>	V <sub>ccq</sub>	V <sub>ss</sub>	DQD <sub>4</sub>	DNU*	A <sub>0</sub>
<b>G</b>	A <sub>7</sub>	DQC <sub>0</sub>	DQC <sub>7</sub>	V <sub>ss</sub>	V <sub>cc</sub>	V <sub>cc</sub>	DQD <sub>3</sub>	A <sub>1</sub>	A <sub>3</sub>
<b>H</b>	A <sub>18</sub>	DQC <sub>1</sub>	DQC <sub>6</sub>	V <sub>cc</sub>	V <sub>cc</sub>	V <sub>cc</sub> '	DQD <sub>2</sub>	A <sub>2</sub>	A <sub>5</sub>
<b>J</b>	A <sub>9</sub>	A <sub>6</sub>	DQF <sub>2</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	DQD <sub>1</sub>	A <sub>4</sub>	A <sub>16</sub>
<b>K</b>	A <sub>8</sub>	DQF <sub>4</sub>	FQF <sub>3</sub>	V <sub>cc</sub>	V <sub>cc</sub>	V <sub>cc</sub>	DQD <sub>0</sub>	A <sub>14</sub>	A <sub>15</sub>
<b>L</b>	A <sub>17</sub>	DQF <sub>5</sub>	DQF <sub>6</sub>	V <sub>cc</sub>	V <sub>cc</sub>	V <sub>ss</sub>	DQE <sub>6</sub>	A <sub>12</sub>	A <sub>13</sub>
<b>M</b>	ADV <sub>1</sub>	OE <sub>1</sub> #	DQF <sub>7</sub>	V <sub>ss</sub>	V <sub>ccq</sub>	V <sub>ccq</sub>	DQE <sub>7</sub>	A <sub>10</sub>	A <sub>11</sub>
<b>N</b>	CKE <sub>1</sub> #	WE <sub>1</sub> #	DQPF	V <sub>ccq</sub>	V <sub>ccq</sub>	V <sub>ccq</sub>	DQE <sub>5</sub>	DQE <sub>3</sub>	LBO#
<b>P</b>	CLK <sub>1</sub>	CS <sub>21</sub> #	DQF <sub>1</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	DQE <sub>4</sub>	DQE <sub>2</sub>	DQE <sub>0</sub>
<b>R</b>	BW <sub>e</sub> #	BW <sub>f</sub> #	DQF <sub>0</sub>	DQG <sub>1</sub>	DQG <sub>4</sub>	DQH <sub>1</sub>	DQH <sub>2</sub>	DQE <sub>1</sub>	DQPE
<b>T</b>	BW <sub>g</sub> #	BW <sub>h</sub> #	DQG <sub>0</sub>	DQG <sub>2</sub>	DQG <sub>5</sub>	DQH <sub>0</sub>	DQH <sub>4</sub>	DQH <sub>7</sub>	DQPH
<b>U</b>	CS <sub>11</sub> #	CS <sub>21</sub>	DQG <sub>3</sub>	DQPG	DQG <sub>6</sub>	DQG <sub>7</sub>	DQH <sub>3</sub>	DQH <sub>5</sub>	DQH <sub>6</sub>

NOTE: DNU means Do Not Use and are reserved for future use.

\* Pin F<sub>8</sub> reserved for A<sub>19</sub> upgrade to 1M x 72



## FUNCTION DESCRIPTION

The WEDPZ512K72V-XBX is an ZBL SSRAM designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa. All inputs (with the exception of OE#, LBO# and ZZ) are synchronized to rising clock edges.

All read, write and deselect cycles are initiated by the ADV input. Subsequent burst addresses can be internally generated by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

Clock Enable (CKE#) pin allows the operation of the chip to be suspended as long as necessary. When CKE# is high, all synchronous inputs are ignored and the internal device registers will hold their previous values. NBL SSRAM latches external address and initiates a cycle when CKE and ADV are driven low at the rising edge of the clock.

Output Enable (OE#) can be used to disable the output at any given time. Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register, CKE# is driven low, the write enable input signals WE# are driven high, and ADV driven low. The internal array is read between the first rising edge and the second rising edge of the clock and the data is latched in the output register. At the second clock edge the data is driven out of the SRAM. During read operation OE# must be driven low for the device to drive out the requested data.

Write operation occurs when WE# is driven low at the rising edge of the clock. BW#[h:a] can be used for byte write operation. The pipe-lined ZBL SSRAM uses a late-late write cycle to utilize 100% of the bandwidth. At the first rising edge of the clock, WE# and address are registered, and the data associated with that address is required two cycles later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO# pin. When this pin is low, linear burst sequence is selected. And when this pin is high, Interleaved burst sequence is selected.

During normal operation, ZZ must be driven low. When ZZ is driven high, the SRAM will enter a Power Sleep Mode after two cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates after two cycles of wake up time.

## BURST SEQUENCE TABLE

(Interleaved Burst, LBO# = High)

LBO# Pin	High	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address ↓ Fourth Address		0	0	0	1	1	0	1	1
		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
		1	1	1	0	0	1	0	0

(Linear Burst, LBO# = Low)

LBO# Pin	High	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address ↓ Fourth Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
		1	1	0	0	0	1	1	0

NOTE 1: LBO pin must be tied to High or Low, and Floating State must not be allowed.



## TRUTH TABLES

## SYNCHRONOUS TRUTH TABLE

CEx#	ADV	WE#	BWx#	OE#	CKE#	CLK	Address Accessed	Operation
H	L	X	X	X	L	-	N/A	Deselect
X	H	X	X	X	L	-	N/A	Continue Deselect
L	L	H	X	L	L	-	External Address	Begin Burst Read Cycle
X	H	X	X	L	L	-	Next Address	Continue Burst Read Cycle
L	L	H	X	H	L	-	External Address	NOP/Dummy Read
X	H	X	X	H	L	-	Next Address	Dummy Read
L	L	L	L	X	L	-	External Address	Begin Burst Write Cycle
X	H	X	L	X	L	-	Next Address	Continue Burst Write Cycle
L	L	L	H	X	L	-	N/A	NOP/Write Abort
X	H	X	H	X	L	-	Next Address	Write Abort
X	X	X	X	X	H	-	Current Address	Ignore Clock

## NOTES:

1. X means "Don't Care."
2. The rising edge of clock is symbolized by (-).
3. A continue deselect cycle can only be entered if a deselect cycle is executed first.
4. WRITE# = L means Write operation in WRITE TRUTH TABLE.  
WRITE# = H means Read operation in WRITE TRUTH TABLE.
5. Operation finally depends on status of asynchronous input pins (ZZ and OE).
6. CEx# refers to the combination of CS1#, CS2 and CS2#.

## WRITE TRUTH TABLE

WE#	BWa#	BWb#	BWc#	BWd#	Operation
H	X	X	X	X	Read
L	L	H	H	H	Write Byte a
L	H	L	H	H	Write Byte b
L	H	H	L	H	Write Byte c
L	H	H	H	L	Write Byte d
L	L	L	L	L	Write All Bytes
L	H	H	H	H	Write Abort/NOP

## NOTES:

1. X means "Don't Care."
2. All inputs in this table must meet setup and hold time around the rising edge of CLK (-).
3. Replace BWa# with BWe#, BWb# with BWf#, BWc# with BWg# and BWd# with BWn# for operation of IC2.



## ABSOLUTE MAXIMUM RATINGS\*

V <sub>IN</sub> Voltage or any other pin relative to V <sub>SS</sub>	-0.3V to +4.6V
Voltage on V <sub>CC</sub> Supply Relative to V <sub>SS</sub>	-0.3V to +4.6V
Storage Temperature (BGA)	-55°C to +150°C
Maximum Operating Junction Temperature	125°C

\* Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Electrical Characteristics

-55°C ≤ T<sub>A</sub> ≤ +125°C

Description	Symbol	Conditions	Min	Max	Units	Notes
Input High (Logic 1) Voltage	V <sub>IH</sub>	3.3V I/O	2.0	V <sub>CC</sub> +0.5	V	1
			2.5V I/O	V <sub>CC</sub> +0.5		
Input Low (Logic 0) Voltage	V <sub>IL</sub>	3.3V I/O	-0.3	0.7	V	1
			2.5 I/O	0.7		
Input Leakage Current	I <sub>IL</sub>	V <sub>CC</sub> = Max, 0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-4	+4	μA	2
Output Leakage Current	I <sub>OL</sub>	Output(s) Disabled, V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>CCQ</sub>	-2	+2	μA	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA	2.4	—	V	1
		I <sub>OH</sub> = -1mA (2.5V I/O)	2.0	—	V	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8.0mA (3.3V I/O)	—	0.4	V	1
		I <sub>OL</sub> = 1.0 mA (2.5V I/O)	—	0.4	V	
Supply Voltage	V <sub>CC</sub>		3.135	3.465	V	1
I/O Power Supply (3.3V)	V <sub>CCQ</sub>		3.135	3.465	V	1
I/O Power Supply (2.5V)	V <sub>CCQ</sub>		2.375	2.9	V	1

### NOTES:

- All voltages referenced to V<sub>SS</sub> (GND)
- ZZ pin has an internal pull-up, and input leakage = ± 20 μA.

## DC CHARACTERISTICS

-55°C ≤ T<sub>A</sub> ≤ +125°C

Description	Symbol	Conditions	150 MHz (Max)	133 MHz (Max)	100 MHz (Max)	Units	Notes
Power Supply Current: Operating	I <sub>DD</sub>	Device Selected; All Inputs ≤ V <sub>IL</sub> or ≥ V <sub>IH</sub> ; Cycle Time ≥ TCYC MIN; V <sub>CC</sub> = MAX; Output Open	700	650	600	mA	1
Power Supply Current: Standby	I <sub>SB2</sub>	Device Deselected; V <sub>CC</sub> = MAX; All Inputs ≤ V <sub>IL</sub> or ≥ V <sub>IH</sub> All Inputs Static; CLK Frequency = MAX Output Open, ZZ ≥ V <sub>CC</sub> - 0.2V	120	120	120	mA	
Clock Running Standby Current	I <sub>SB</sub>	Device Deselected; V <sub>CC</sub> = MAX; All Inputs ≤ V <sub>SS</sub> + 0.2 or ≥ V <sub>CC</sub> - 0.2; f = max ; ZZ ≤ V <sub>IL</sub>	200	180	160	mA	

### NOTES:

- I<sub>DD</sub> is specified with no output current and increases with faster cycle times.  
I<sub>DD</sub> increases with faster cycle times and greater output loading.

## BGA CAPACITANCE

T<sub>A</sub> = +25°C, f = 1MHz

Description	Symbol	Max	Units	Notes
Control Input Capacitance (LBO#, zz)	C <sub>IC</sub>	16	pF	1
Control Input Capacitance	C <sub>I</sub>	8	pF	1
Input/Output Capacitance (DQ)	C <sub>O</sub>	10	pF	1
Address Capacitance	C <sub>A</sub>	16	pF	1
Clock Capacitance	C <sub>CK</sub>	6	pF	1

NOTES: 1. This parameter is not tested but guaranteed by design.

## THERMAL RESISTANCE

Parameter	Symbol	Max	Unit
Thermal Resistance: Die Junction to Ambient	θ <sub>JA</sub>	28.1	°C/W
Thermal Resistance: Die Junction to Ball	θ <sub>JB</sub>	16.0	°C/W
Thermal Resistance: Die Junction to Case	θ <sub>JC</sub>	7.1	°C/W

Note: Refer to Application Note "PBGA Thermal Resistance Correlation" for further information regarding WEDC's thermal modeling.





## AC CHARACTERISTICS

-55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol	150MHz		133MHz		100MHz		Units
		Min	Max	Min	Max	Min	Max	
Clock Time	t <sub>cyC</sub>	6.7		7.5		10.0		ns
Clock Access Time	t <sub>cD</sub>	—	3.8	—	4.2	—	5.0	ns
Output enable to Data Valid	t <sub>oE</sub>	—	3.8	—	4.2	—	5.0	ns
Clock High to Output Low-Z	t <sub>lZC</sub>	1.5	—	1.5	—	1.5	—	ns
Output Hold from Clock High	t <sub>oH</sub>	1.5	—	1.5	—	1.5	—	ns
Output Enable Low to output Low-Z	t <sub>lZOE</sub>	0.0	—	0.0	—	0.0	—	ns
Output Enable High to Output High-Z	t <sub>hZOE</sub>	—	3.0	—	3.5	—	3.5	ns
Clock High to Output High-Z	t <sub>hZC</sub>	—	3.0	—	3.5	—	3.5	ns
Clock High Pulse Width	t <sub>CH</sub>	2.5	—	2.5	—	3.0	—	ns
Clock Low Pulse Width	t <sub>CL</sub>	2.5	—	2.5	—	3.0	—	ns
Address Setup to Clock High	t <sub>AS</sub>	1.5	—	1.5	—	1.5	—	ns
CKE Setup to Clock High	t <sub>CES</sub>	1.5	—	1.5	—	1.5	—	ns
Data Setup to Clock High	t <sub>DS</sub>	1.5	—	1.5	—	1.5	—	ns
Write Setup to Clock High	t <sub>WS</sub>	1.5	—	1.5	—	1.5	—	ns
Address Advance to Clock High	t <sub>ADVS</sub>	1.5		1.5		1.5		ns
Chip Select Setup to Clock High	t <sub>CSS</sub>	1.5		1.5		1.5		ns
Address Hold to Clock high	t <sub>AH</sub>	0.5	—	0.5	—	0.5	—	ns
CKE Hold to Clock High	t <sub>CEH</sub>	0.5	-	0.5	—	0.5	—	ns
Data Hold to Clock High	t <sub>DH</sub>	0.5	—	0.5	—	0.5	—	ns
Write Hold to Clock High	t <sub>WH</sub>	0.5	—	0.5	—	0.5	—	ns
Address Advance to Clock High	t <sub>ADVH</sub>	0.5	—	0.5	—	0.5	—	ns
Chip Select Hold to Clock High	t <sub>CSH</sub>	0.5	—	0.5	—	0.5	—	ns

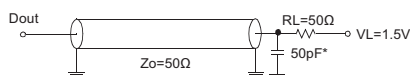
### NOTES:

1. All Address inputs must meet the specified setup and hold times for all rising clock (CLK) edges when ADV is sampled low and CSx# is sampled valid. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Chip enable must be valid at each rising edge of CLK (when ADV is Low) to remain enabled.
3. A write cycle is defined by WE# low having been registered into the device at ADV Low. A Read cycle is defined by WE# High with ADV Low. Both cases must meet setup and hold times.

## AC TEST CONDITIONS

Parameter	Value
Input Pulse Level	0 to 3.6V
Input Rise and Fall Time	1.0V/ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Output Load (A & B)

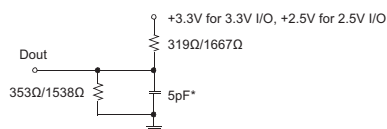
### OUTPUT LOAD (A)



V<sub>L</sub> = 1.5V for 3.3V I/O  
V<sub>CCQ</sub>/2 for 2.5V I/O

### OUTPUT LOAD (B)

FOR t<sub>lzc</sub>, t<sub>lzoe</sub>, t<sub>hzoe</sub>, and t<sub>hzc</sub>



\*Including Scope and Jig Capacitance



## SNOOZE MODE

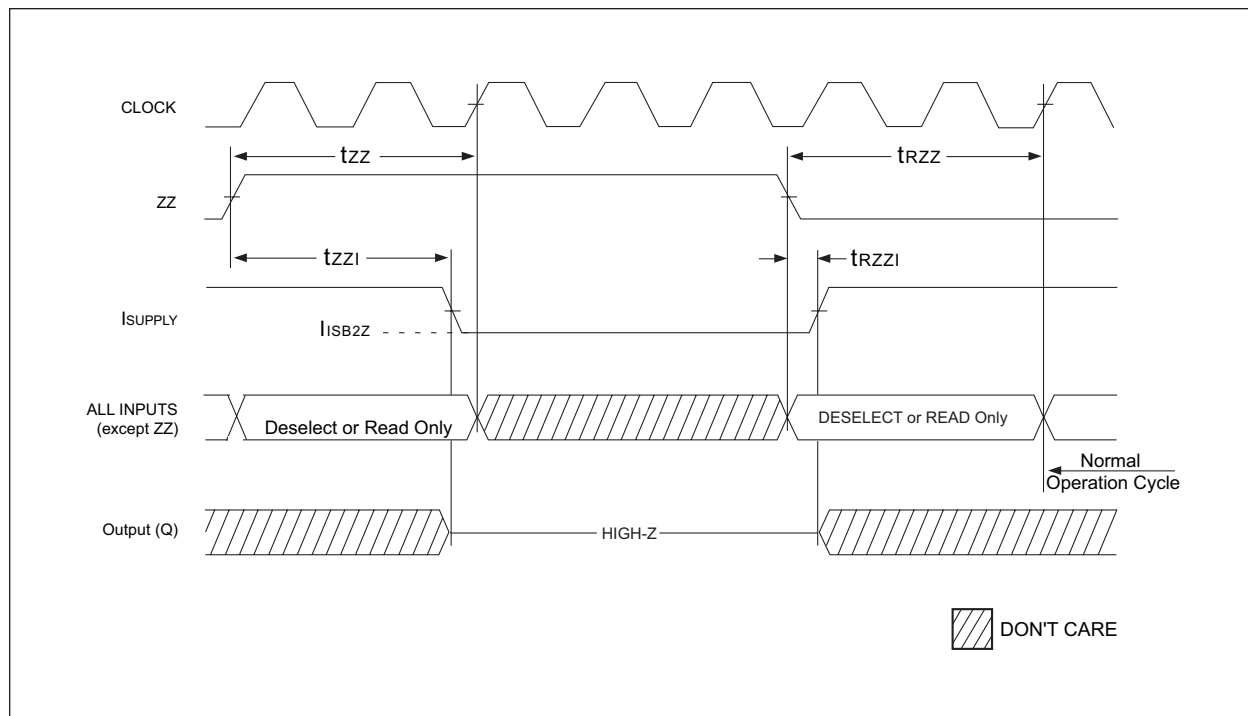
SNOOZE MODE is a low-current, “power-down” mode in which the device is deselected and current is reduced to  $ISB2Z$ . The duration of SNOOZE MODE is dictated by the length of time  $Z$  is in a HIGH state. After the device enters SNOOZE MODE, all inputs except  $ZZ$  become gated inputs and are ignored.  $ZZ$  is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE.

When  $ZZ$  becomes a logic HIGH,  $ISB2Z$  is guaranteed after the setup time  $t_{zz}$  is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.

**Snooze Mode**

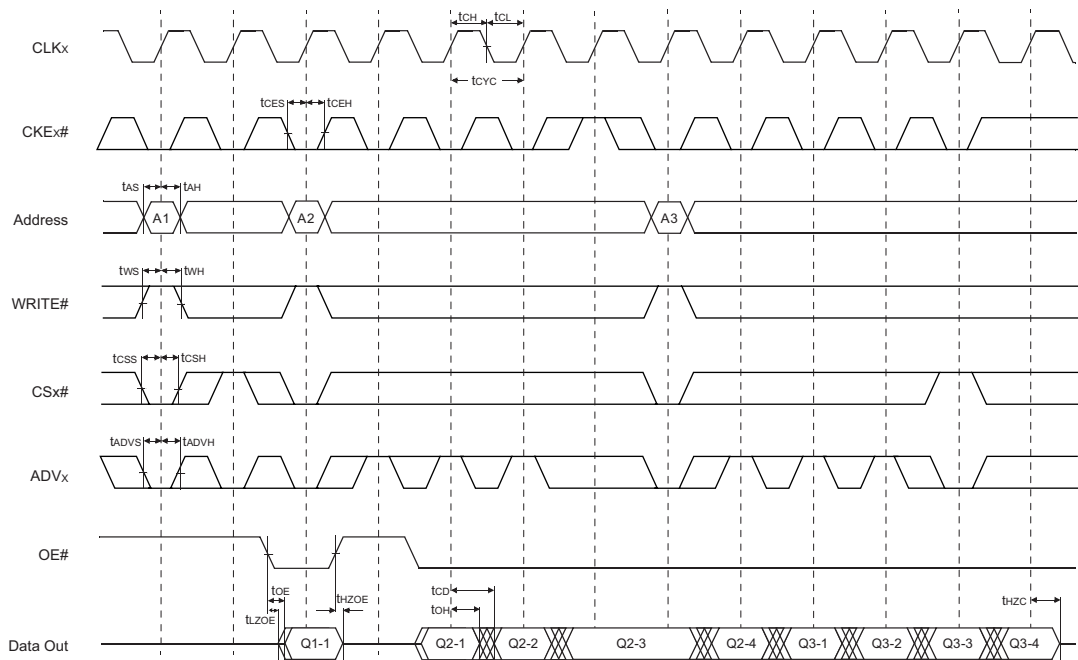
Description	Conditions	Symbol	Min	Max	Units
Current during SNOOZE MODE	$ZZ \geq V_{IH}$	$ISB2Z$		20	mA
$ZZ$ active to input ignored		$t_{zz}$		2	cycle
$ZZ$ inactive to input sampled		$tr_{zz}$	2		cycle
$ZZ$ active to snooze current		$t_{zz1}$		2	cycle
$ZZ$ inactive to exit snooze current		$tr_{zz1}$	0		ns

**FIGURE 2 – SNOOZE MODE TIMING DIAGRAM**





### FIGURE 3 – TIMING WAVEFORM OF READ CYCLE



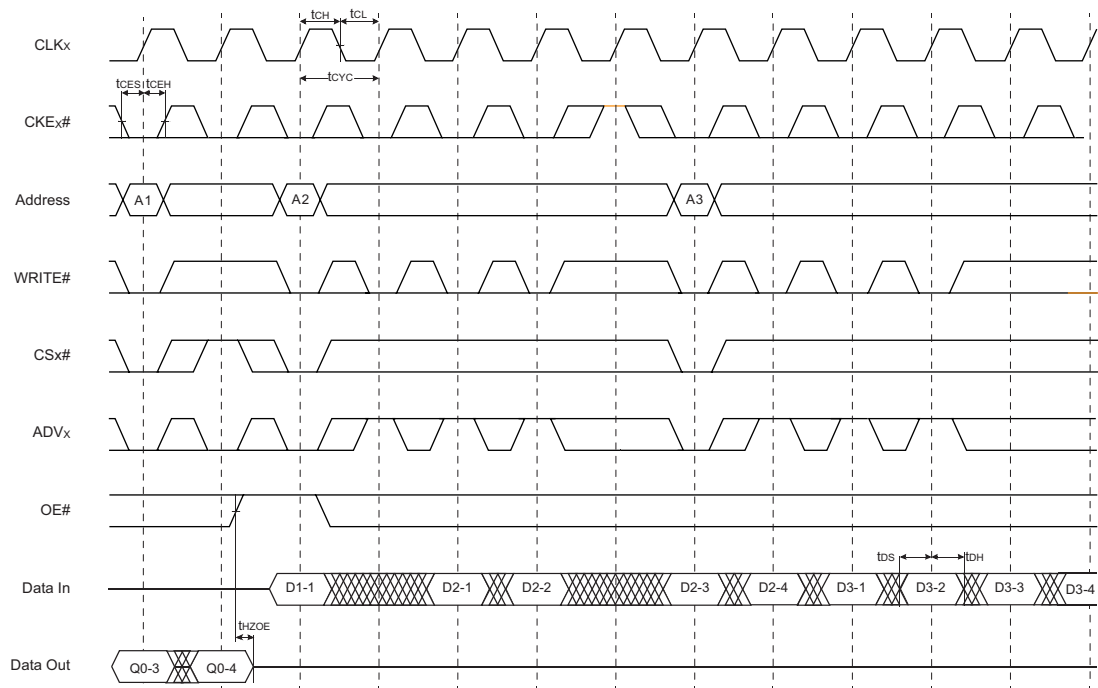
NOTES: WRITE# = L means WE# = L, and BW# = L  
CSx# refers to the combination of CS10#, CS20# and CS21#, or CS11#, CS21 and CS21#.

□ Don't Care  
X Undefined





### FIGURE 4 – TIMING WAVEFORM OF WRITE CYCLE

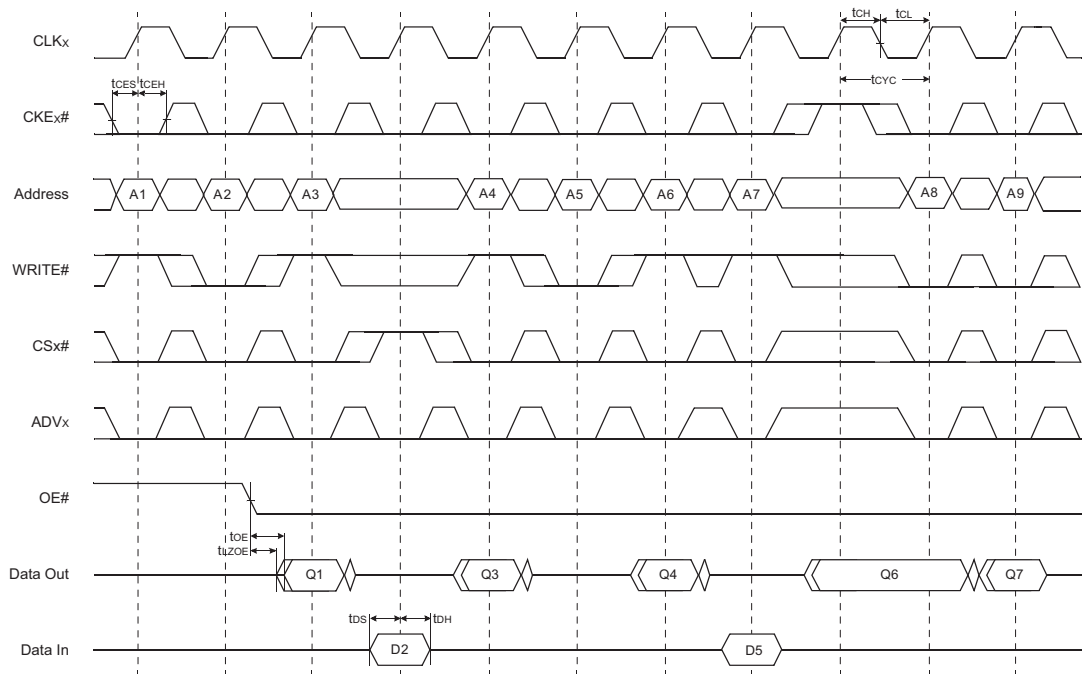


NOTES: WRITE# = L means WE# = L, and BW# = L  
CSx# refers to the combination of CS1#, CS2# and CS2#/, or CS1#/, CS2# and CS2#/.

□ Don't Care  
X Undefined



**FIGURE 5 – TIMING WAVEFORM OF SINGLE READ/WRITE**

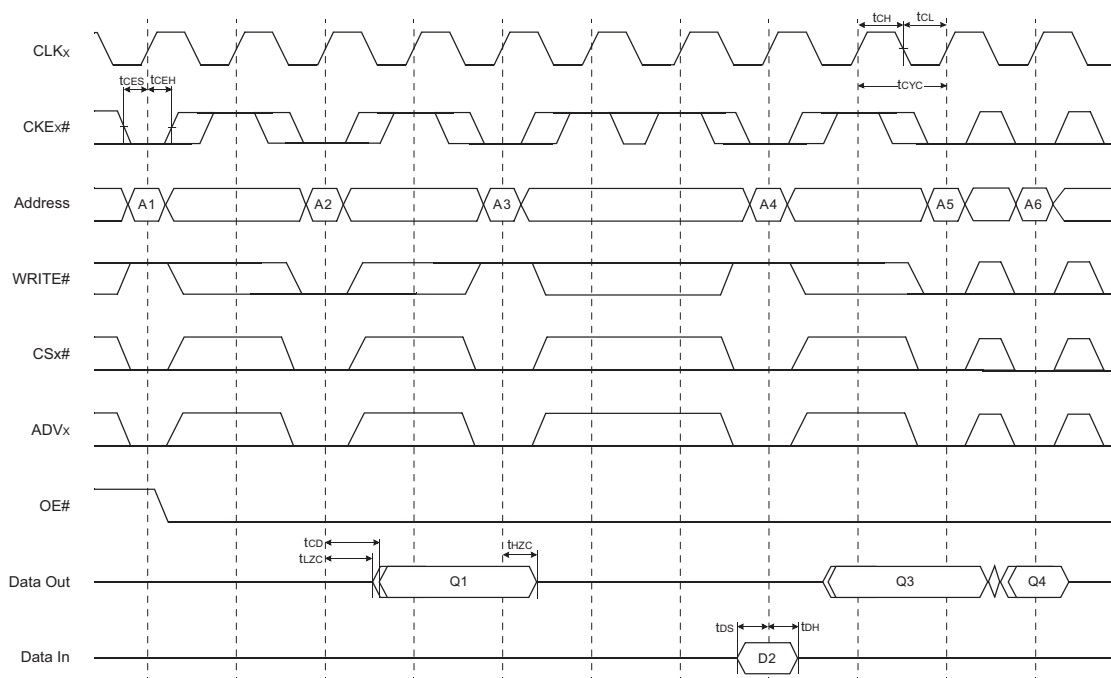


NOTES: WRITE# = L means WE# = L, and BW# = L  
CSx# refers to the combination of CS1#, CS2# and CS2#, or CS1#, CS2# and CS2#.

□ Don't Care  
⊗ Undefined



FIGURE 6 – TIMING WAVEFORM OF CKE OPERATION

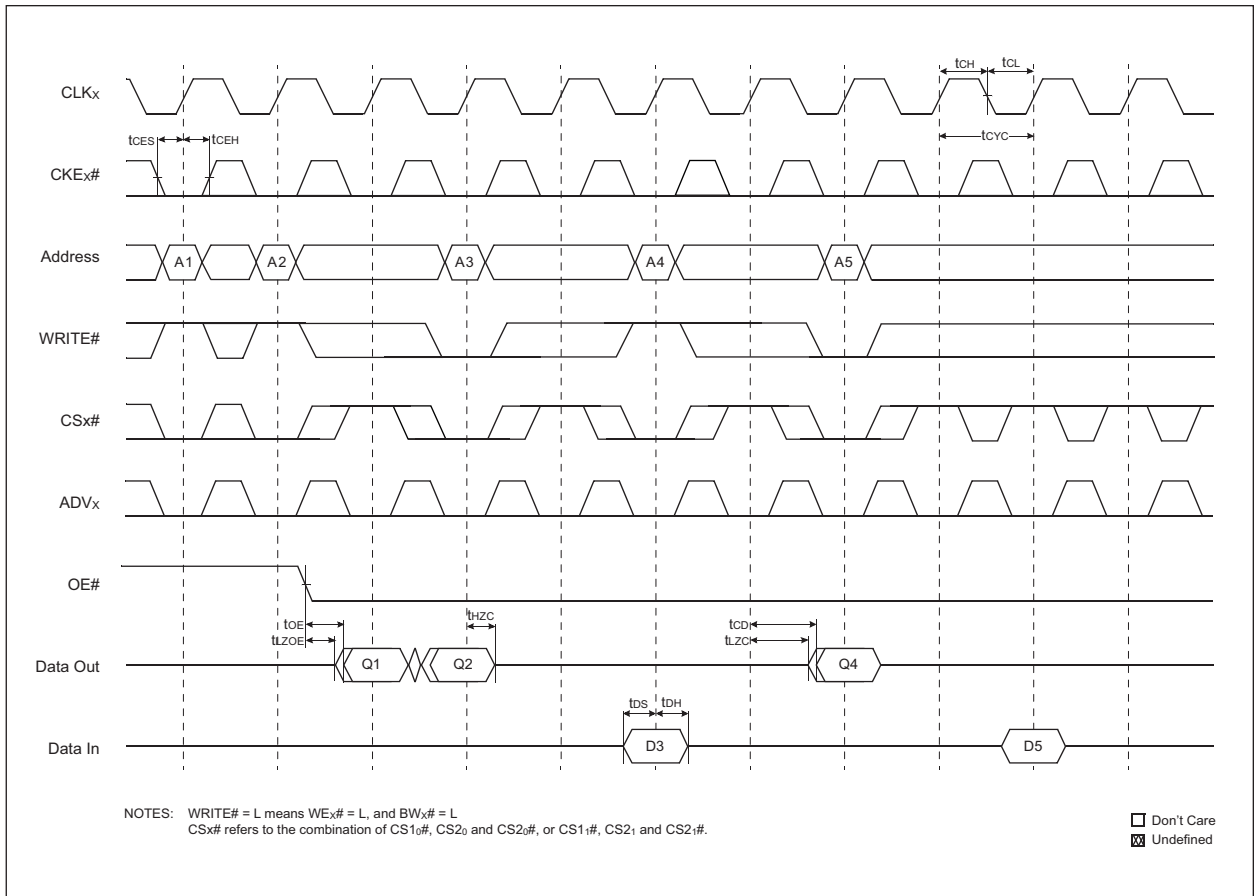


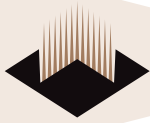
NOTES: WRITE# = L means WE<sub>x</sub># = L, and BW<sub>x</sub># = L  
CS<sub>x</sub># refers to the combination of CS1<sub>0</sub>#, CS2<sub>0</sub># and CS2<sub>1</sub>#, or CS1<sub>1</sub>#, CS2<sub>1</sub># and CS2<sub>2</sub>#.

□ Don't Care  
⊞ Undefined

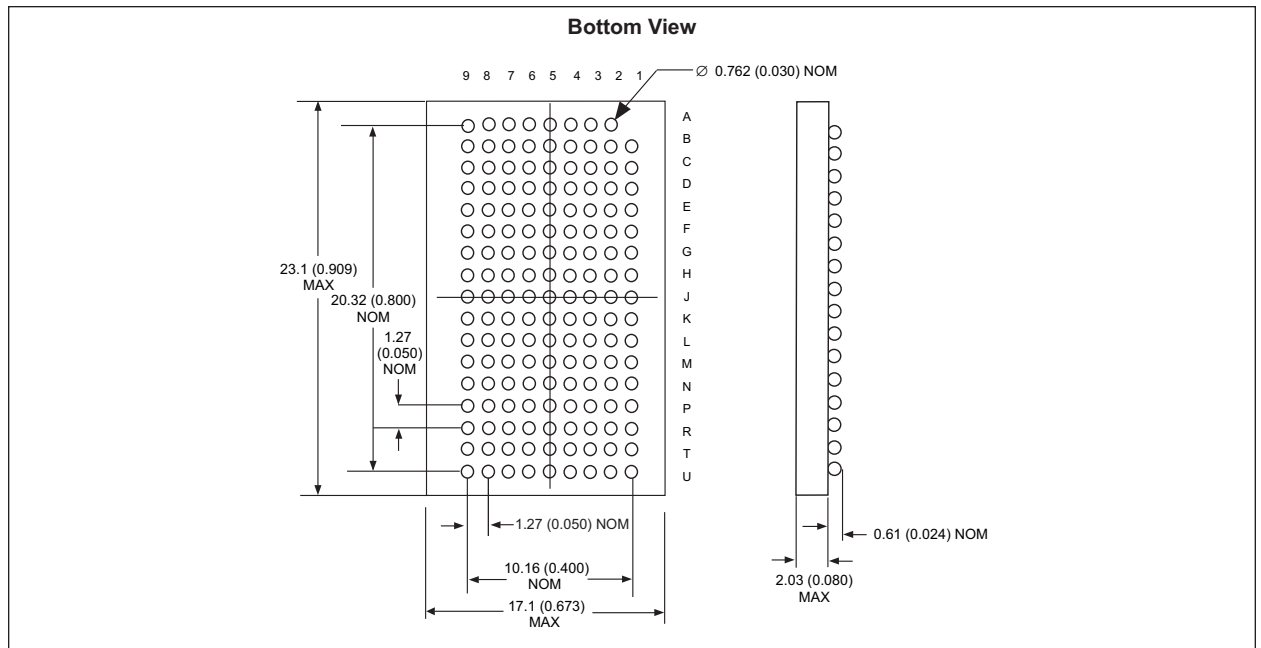


## FIGURE 7 – TIMING WAVEFORM OF CE OPERATION





### PACKAGE DIMENSION: – 152 BUMP PBGA



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

### ORDERING INFORMATION

**WED P Z 512K 72 V - XXX B X**

**DEVICE GRADE:**

<b>M</b> = Military	-55°C to +125°C
<b>I</b> = Industrial	-40°C to +85°C
<b>C</b> = Commercial	0°C to +70°C

**PACKAGE:**

**B** = 152 Plastic Ball Grid Array (PBGA)

**FREQUENCY (MHz)**

<b>100</b> = 100MHz
<b>133</b> = 133MHz
<b>150</b> = 150MHz

**3.3 V Voltage**

**CONFIGURATION, 512K x 72**

**SSRAM ZBL**

**PLASTIC**

**WHITE ELECTRONIC DESIGNS CORP.**



## Document Title

512K x 72 Synchronous Pipeline Burst ZBL SRAM

## Revision History

Rev #	History	Release Date	Status
Rev 0	Initial Release	May 2001	Advanced
Rev 1	Changes (Pg. 1) 1.1 Change status from Advanced to Preliminary	March 2001	Preliminary
Rev 2	Changes (Pg. 1, 2) 1.1 Block Diagram: Address lines should be A0-18 1.2 Pin Configuration: Add Note *Pin F8 reserved for A19 upgrade to 1Mx72.	March 2002	Preliminary
Rev 3	Changes (Pg. 1, 5) 1.1 BGA Capacitance: Remove references to temperature in individual conditions 1.2 Change $C_i$ from 10pF to 8pF 1.3 Change $C_A$ from 20pF to 16pF 1.4 Change $C_{CK}$ from 7pF to 6pF 1.5 Add Control Input Capacitance ( $C_{IC}$ ) 16pF	November 2002	Preliminary
Rev 4	Changes (Pg. 5) 1.1 Add Thermal Resistance table 1.2 Update current values 1.3 Update package mechanical drawing	May 2003	Preliminary
Rev 5	Changes (Pg. 1, 5, 14) 1.1 Remove reference to Preliminary status 1.2 Add Maximum Operating Junction Temperature of 125°C	June 2003	Preliminary
Rev 6	Changes (Pg. 1, 13, 14) 1.1 Change mechanical drawing to new style	November 2003	Preliminary
Rev 7	Changes (Pg. 1, 5, 14) 1.1 Change VIL 3.3V to 0.7V maximum 1.2 Change status to Final	February 2006	Final