TEMIC
Semiconductors

SUP/SUB65P06-20

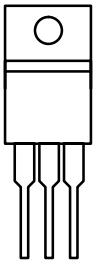
P-Channel Enhancement-Mode Transistors

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–60	0.020	–65[a]

175°C Rated
Maximum Junction Temperature

TO-220AB



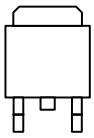
G D S

Top View

SUP65P06-20

DRAIN connected to TAB

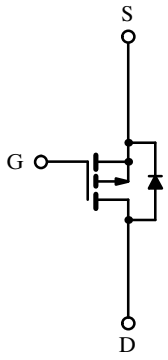
TO-263



G D S

Top View

SUB65P06-20



P-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current (T_J = 175°C)	T_C = 25°C	I_D	–65[a]	A
	T_C = 125°C		–39	
Pulsed Drain Current		I_{DM}	–200	
Avalanche Current		I_{AR}	–60	
Repetitive Avalanche Energy[b]	L = 0.1 mH	E_{AR}	180	mJ
Power Dissipation	T_C = 25°C (TO-220AB and TO-263)	P_D	187[d]	W
	T_A = 125°C (TO-263)[c]		3.7	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 175	°C

Thermal Resistance Ratings

Parameter		Symbol	Limit	Unit
Junction-to-Ambient	PCB Mount (TO-263)[c]	R_{thJA}	40	°C/W
	Free Air (TO-220AB)	R_{thJA}	62.5	
Junction-to-Case		R_{thJC}	0.8	

Notes:
a. Package limited.
b. Duty cycle ≤ 1%.
c. When mounted on 1" square PCB (FR-4 material).
d. See SOA curve for voltage derating.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70289.
A SPICE Model data sheet is available for this product (FaxBack document #70543).

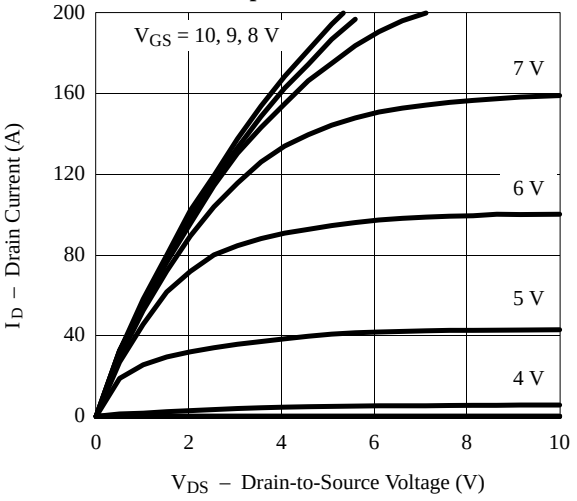
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = –250 µA	–60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = –250 µA	–2.0	–3.0	–4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –60 V, V_{GS} = 0 V			–1	µA
		V_{DS} = –60 V, V_{GS} = 0 V, T_J = 125°C			–50	
		V_{DS} = –60 V, V_{GS} = 0 V, T_J = 175°C			–150	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = –5 V, V_{GS} = –10 V	–120			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = –10 V, I_D = –30 A		0.017	0.020	Ω
		V_{GS} = –10 V, I_D = –30 A, T_J = 125°C			0.033	
		V_{GS} = –10 V, I_D = –30 A, T_J = 175°C			0.042	
Forward Transconductance[b]	g_{fs}	V_{DS} = –15 V, I_D = –30 A	25			S
Dynamic[a]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = –25 V, f = 1 MHz		4500		pF
Output Capacitance	C_{oss}			870		
Reversen Transfer Capacitance	C_{rss}			350		
Total Gate Charge[c]	Q_g	V_{DS} = –30 V, V_{GS} = –10 V, I_D = –65 A		85	120	nC
Gate-Source Charge[c]	Q_{gs}			24		
Gate-Drain Charge[c]	Q_{gd}			22		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = –30 V, R_L = 0.47 Ω I_D ≃ –65 A, V_{GEN} = –10 V, R_G = 2.5 Ω		15	40	ns
Rise Time[c]	t_r			40	80	
Turn-Off Delay Time[c]	$t_{d(off)}$			65	120	
Fall Time[c]	t_f			30	60	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)[a]						
Continuous Current	I_s				–65	A
Pulsed Current	I_{SM}				–200	
Forward Voltage[b]	V_{SD}	I_F = –65 A, V_{GS} = 0 V		–1.1	–1.4	V
Reverse Recovery Time	t_{rr}	I_F = –65 A, di/dt = 100 A/µs		70	120	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			7	9	A
Reverse Recovery Charge	Q_{rr}			0.245	0.54	µC

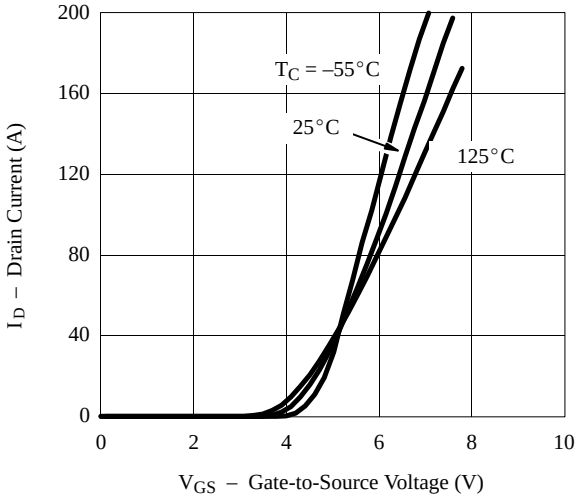
Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Noted)

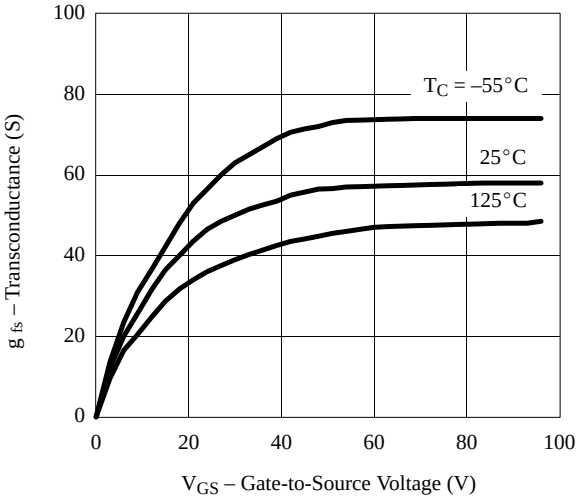
Output Characteristics



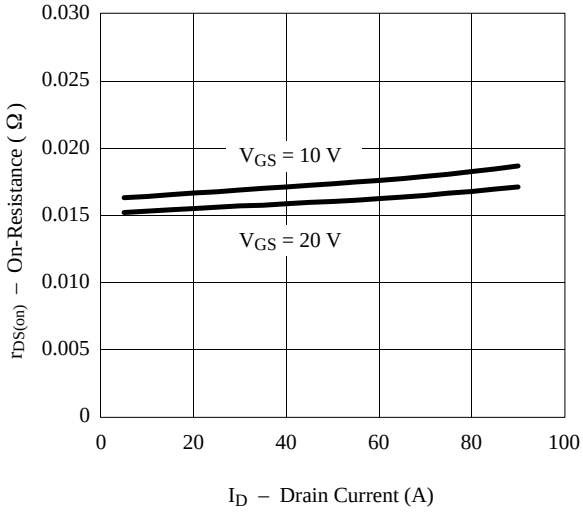
Transfer Characteristics



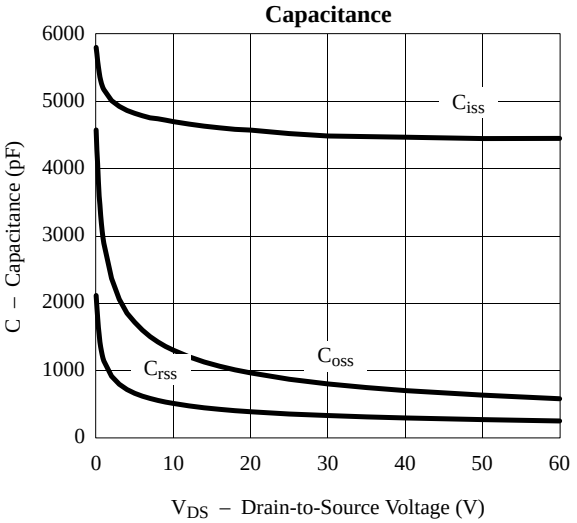
Transconductance



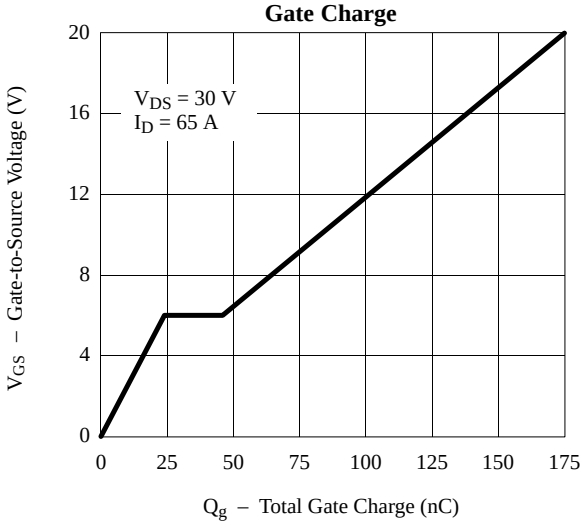
On-Resistance vs. Drain Current



Capacitance

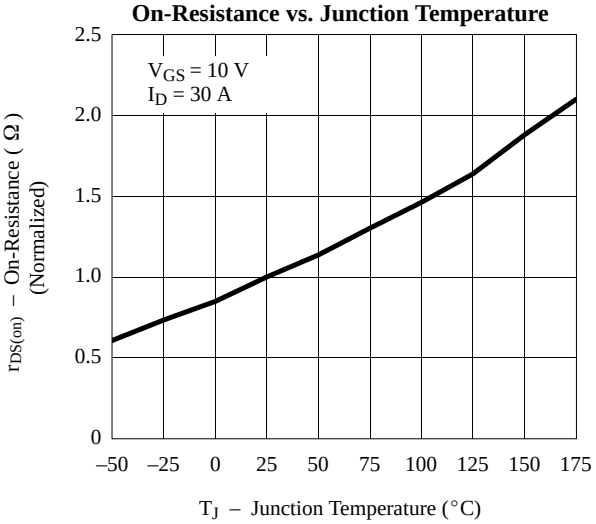


Gate Charge

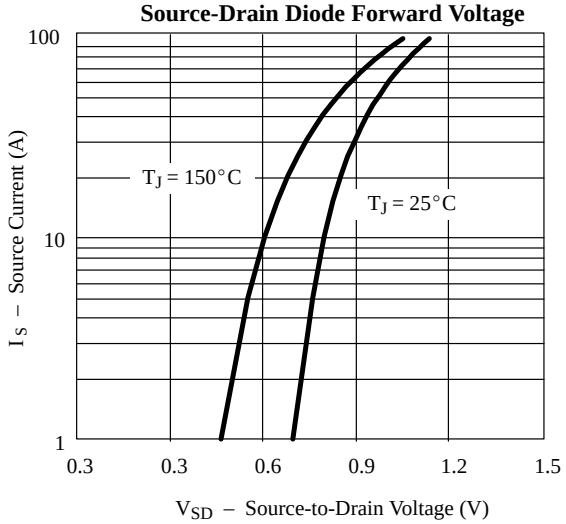


Typical Characteristics (25°C Unless Otherwise Noted)

On-Resistance vs. Junction Temperature

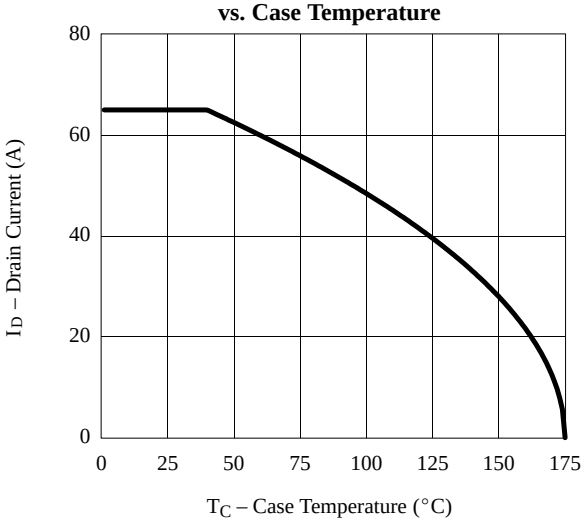


Source-Drain Diode Forward Voltage

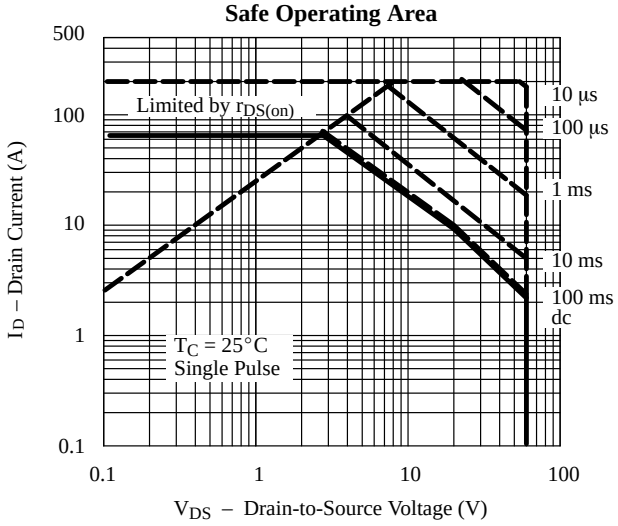


Thermal Ratings

Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case