



STS2DPF80

DUAL P-CHANNEL 80V - 0.21 Ω - 2.3A SO-8

STripFET™ POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STS2DPF80	80 V	<0.25 Ω	2.3 A

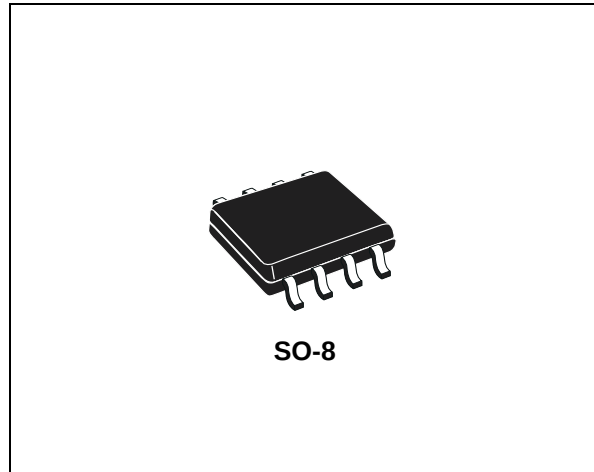
- TYPICAL R_{DS(on)} = 0.21 Ω
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY

DESCRIPTION

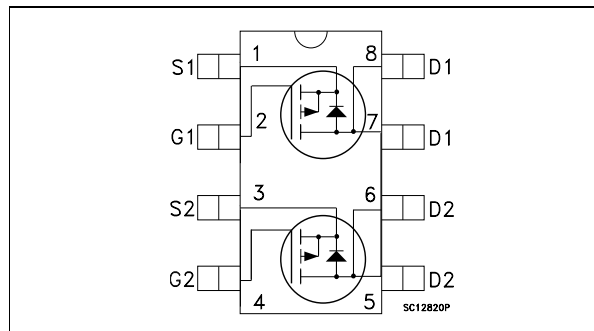
This application specific Power MOSFET is the second generation of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- DC/DC CONVERTERS
- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT
- POWER MANAGEMENT IN CELLULAR PHONES AND DISPLAY NEW GENERATION



INTERNAL SCHEMATIC DIAGRAM



Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STS2DPF80	S8DPF80	SO-8	TAPE & REEL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	80	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 k Ω)	80	V
V _{GS}	Gate- source Voltage	± 20	V
I _D	Drain Current (continuous) at T _C = 25°C Single Operation Drain Current (continuous) at T _C = 100°C Single Operation	2.0 1.3	A A
I _{DM} (●)	Drain Current (pulsed)	8	A
P _{tot}	Total Dissipation at T _C = 25°C	2.5	W
T _{stg}	Storage Temperature	-55 to 150	°C
T _j	Max. Operating Junction Temperature	150	°C

(●) Pulse width limited by safe operating area.

Note: For the P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed

STS2DPF80

TAB.1 THERMAL DATA

$R_{thj-PCB}^{(*)}$	Thermal Resistance Junction-PCB	62.5	°C/W
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(*) When Mounted on 1 inch² FR-4 board, 2 oz of Cu and t [10 sec.

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)

TAB.2 OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250 \mu A$, $V_{GS} = 0$	80			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_C = 125^\circ C$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20 V$			± 100	nA

TAB.3 ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250 \mu A$	2		4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10 V$ $I_D = 1 A$		0.21	0.25	Ω

TAB.4 DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(*)}$	Forward Transconductance	$V_{DS} = 10V$ $I_D = 1 A$		4		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V$, $f = 1 \text{ MHz}$, $V_{GS} = 0$		739 89.5 31		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

TAB.5 SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 40\text{ V}$ $I_D = 1\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 1)		13.5 18		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 64\text{ V}$ $I_D = 2\text{ A}$ $V_{GS} = 10\text{ V}$ (See test circuit, Figure 2)		20 2.5 4.9		nC nC nC

TAB.6 SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 40\text{ V}$ $I_D = 1\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 1)		32 13		ns ns

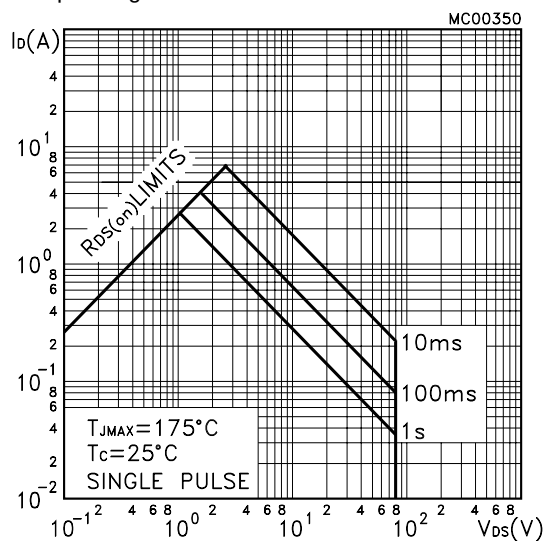
TAB.7 SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}(\bullet)$	Source-drain Current Source-drain Current (pulsed)				2.3 9.2	A A
V_{SD}^*	Forward On Voltage	$I_{SD} = 1\text{ A}$ $V_{GS} = 0$			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 2\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 40\text{ V}$ $T_j = 150^\circ\text{C}$ (See test circuit, Figure 3)		47 87 3.7		ns nC A

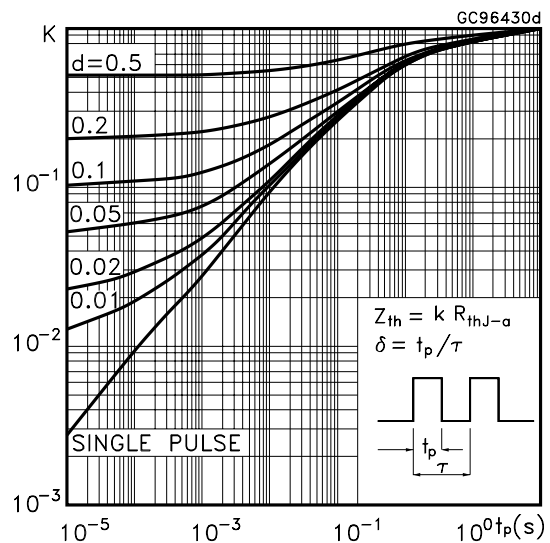
(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

(\bullet) Pulse width limited by safe operating area.

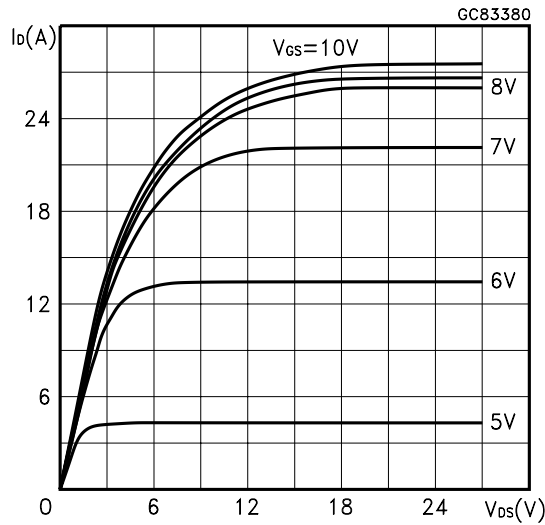
Safe Operating Area



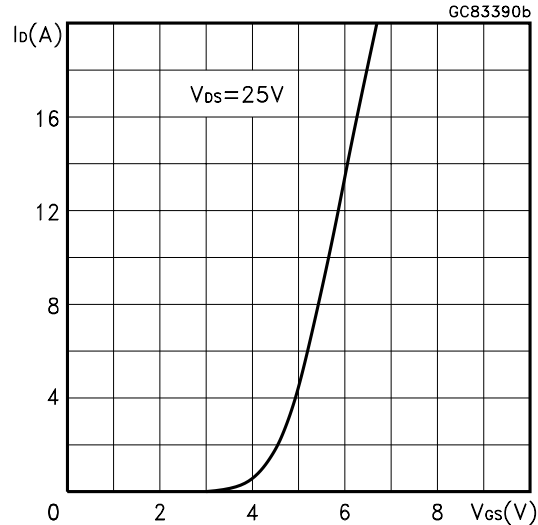
Thermal Impedance



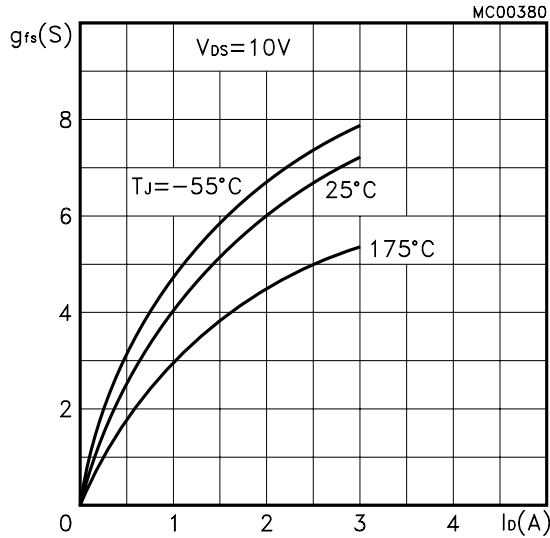
Output Characteristics



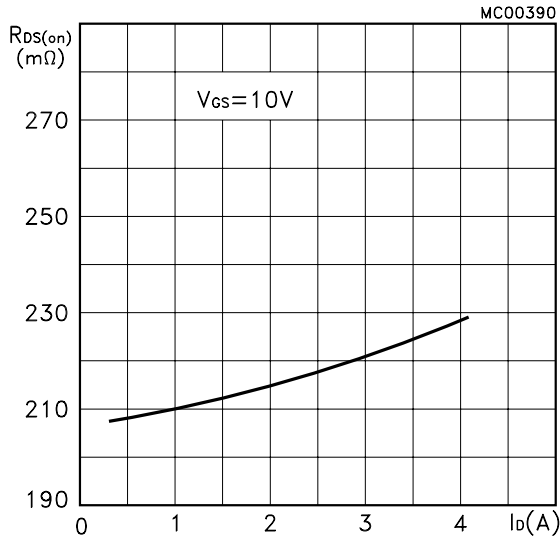
Transfer Characteristics



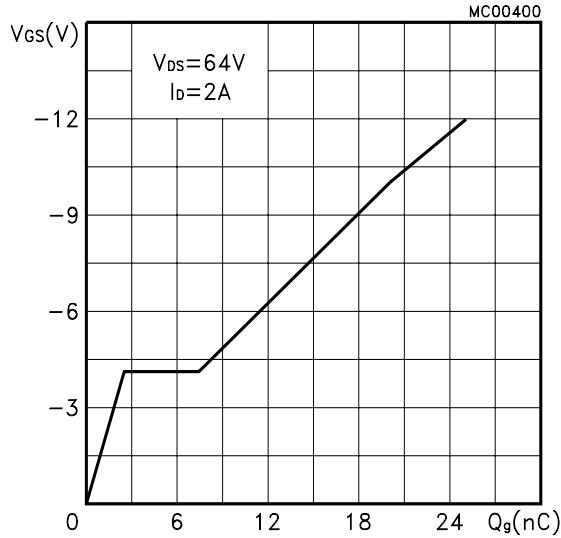
Transconductance



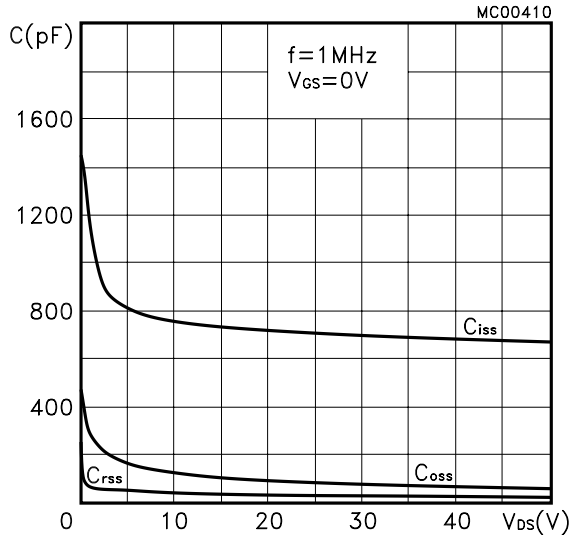
Static Drain-source On Resistance



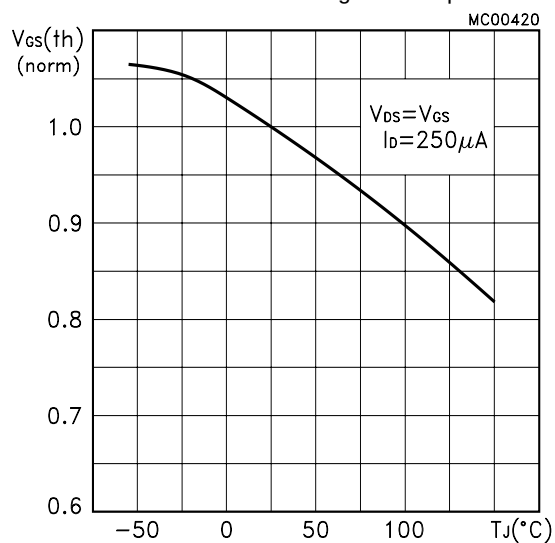
Gate Charge vs Gate-source Voltage



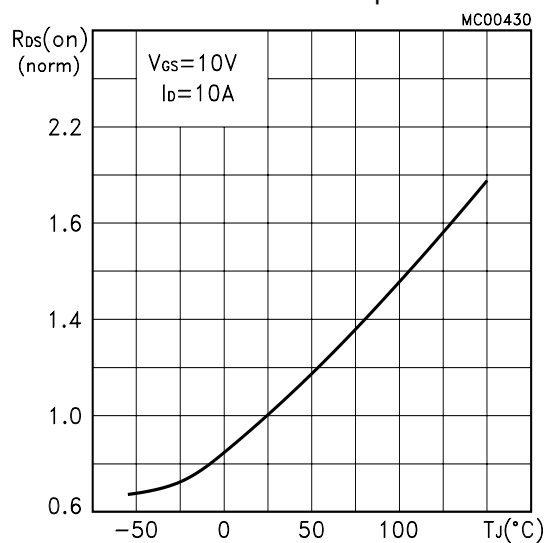
Capacitance Variations



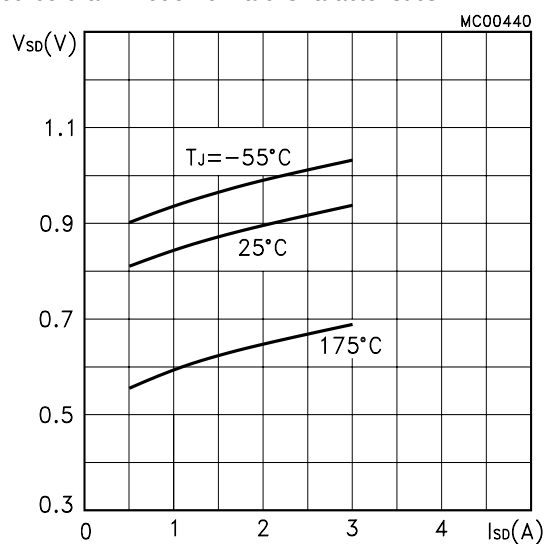
Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized Breakdown Voltage Temperature.

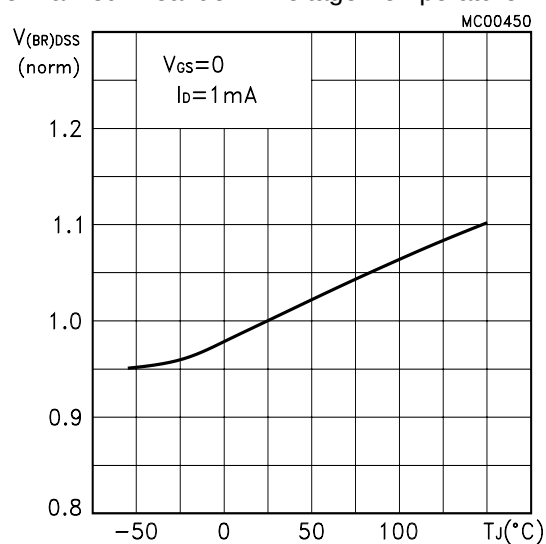


Fig. 1: Switching Times Test Circuits For Resistive Load

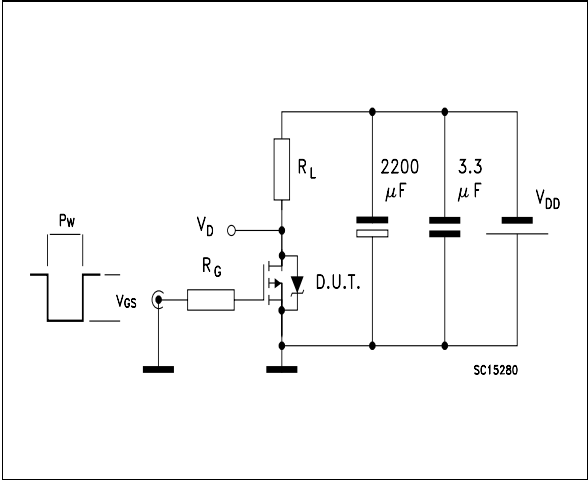


Fig. 2: Gate Charge test Circuit

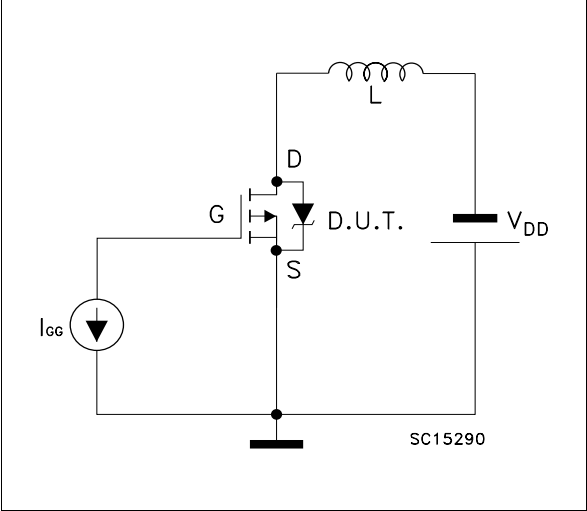
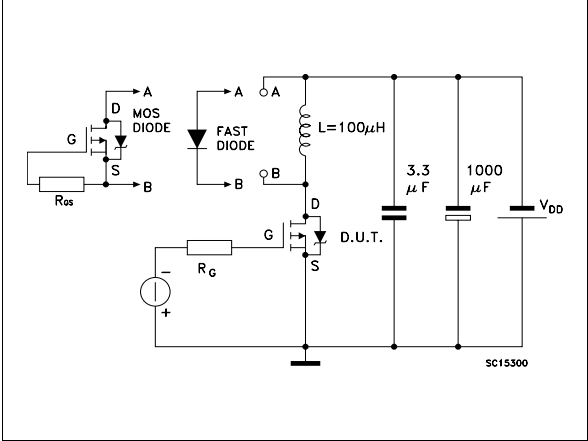
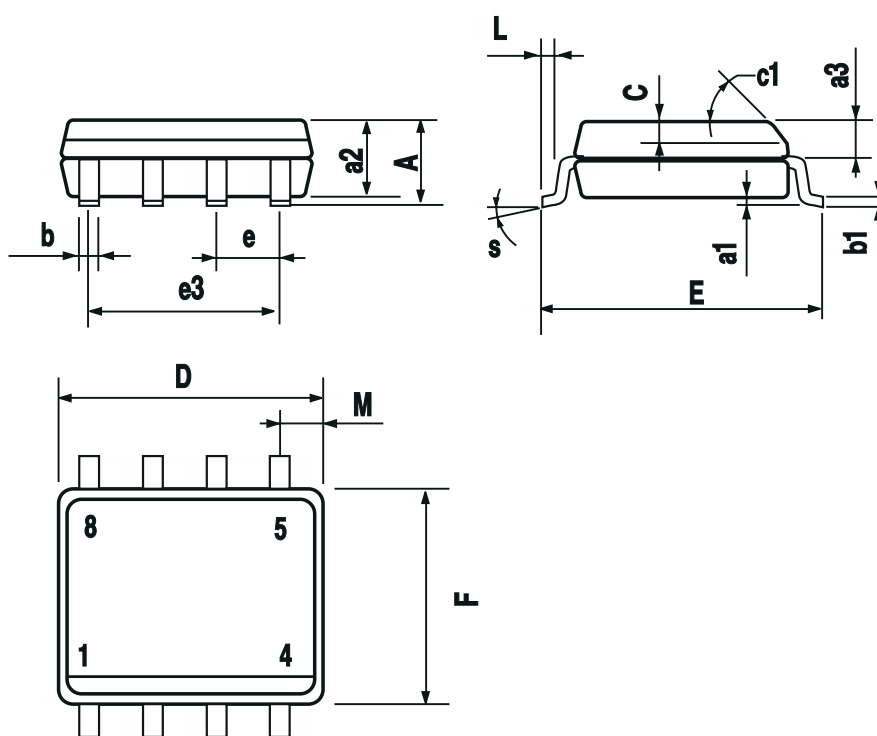


Fig. 3: Test Circuit For Diode Recovery Behaviour



SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



0016023

Revision History

Date	Revision	Description of Changes
Wednesday 16 June 2004	0.1	FIRST ISSUE

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