



STP21NM60N-STF21NM60N-STW21NM60N STB21NM60N - STB21NM60N-1

N-CHANNEL 600V - 0.19 Ω - 17 A TO-220/FP/D²/I²PAK/TO-247
SECOND GENERATION MDmesh™ MOSFET

Table 1: General Features

TYPE	V _{DSS}	R _{DS(on)}	I _D
STB21NM60N	660 V	< 0.24 Ω	17 A
STB21NM60N-1	660 V	< 0.24 Ω	17 A
STF21NM60N	660 V	< 0.24 Ω	17 A (*)
STP21NM60N	660 V	< 0.24 Ω	17 A
STW21NM60N	660 V	< 0.24 Ω	17 A

- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE

DESCRIPTION

The **STx21NM60N** is realized with the second generation of MDmesh Technology. This revolutionary MOSFET associates a new vertical structure to the Company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters

APPLICATIONS

The MDmesh™ II family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.

Figure 1: Package

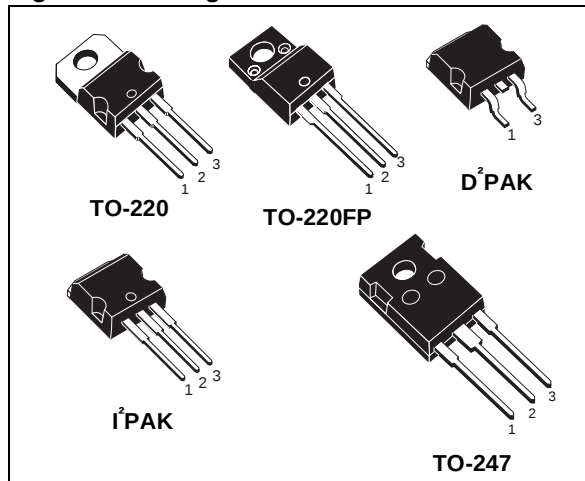


Figure 2: Internal Schematic Diagram

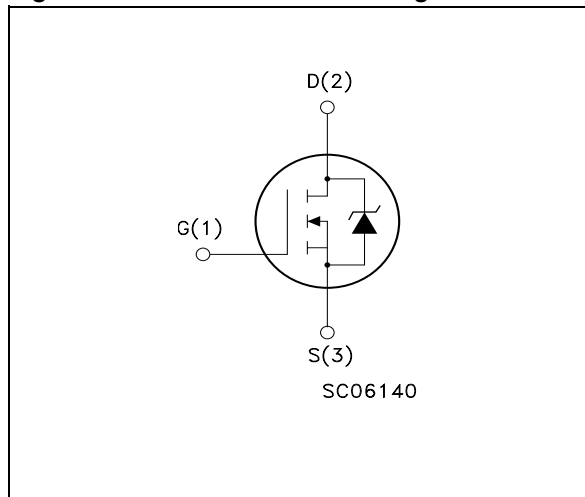


Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STB21NM60N	B21NM60N	D ² PAK	TAPE & REEL
STB21NM60N-1	B21NM60N	I ² PAK	TUBE
STF21NM60N	F21NM60N	TO-220FP	TUBE
STP21NM60N	P21NM60N	TO-220	TUBE
STW21NM60N	W21NM60N	TO-247	TUBE

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value		Unit
		TO-220 / D ² PAK / I ² PAK / TO-247	TO-220FP	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	600		V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	600		V
V _{GS}	Gate- source Voltage	±25		V
I _D	Drain Current (continuous) at T _C = 25°C	17	17 (*)	A
I _D	Drain Current (continuous) at T _C = 100°C	10	10 (*)	A
I _{DM} (●)	Drain Current (pulsed)	64	64 (*)	A
P _{TOT}	Total Dissipation at T _C = 25°C	140	30	W
	Derating Factor	1.12	0.23	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	15		V/ns
V _{iso}	Insulation Withstand Voltage (DC)	--	2500	V
T _{stg}	Storage Temperature	-55 to 150 150		°C
T _j	Max. Operating Junction Temperature			

(●) Pulse width limited by safe operating area

(*) Limited only by maximum temperature allowed

(1) I_{SD} ≤ 16 A, di/dt ≤ 400 A/μs, V_{DD}=80% V_{(BR)DSS}

Table 4: Thermal Data

		TO-220 / D ² PAK / I ² PAK / TO-247	TO-220FP	
R _{thj-case}	Thermal Resistance Junction-case Max	0.89	4.21	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient Max	62.5		°C/W
T _l	Maximum Lead Temperature For Soldering Purpose	300		°C

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I _{AS}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	8.5	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AS} , V _{DD} = 50 V)	610	mJ

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^{\circ}C$ UNLESS OTHERWISE SPECIFIED)**Table 6: On/Off**

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1mA, V_{GS} = 0$	600			V
$dv/dt(2)$	Drain Source Voltage Slope	$V_{DD}=480V, I_D=17A, V_{GS}=10V$	48			V/ns
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}, T_C = 125^{\circ}C$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V, I_D = 8.5 A$		0.190	0.24	Ω

(2) Characteristic value at turn off on inductive load

Table 7: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}(1)$	Forward Transconductance	$V_{DS} = 15 V, I_D = 8 A$		12		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		1950 508 38.4		pF pF pF
$C_{oss \text{ eq.}}(*)$	Equivalent Output Capacitance	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V$		282		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Off-voltage Rise Time Fall Time	$V_{DD} = 300 V, I_D = 8.5 A$ $R_G = 4.7\Omega, V_{GS} = 10 V$ (see Figure 20)		22 15 84 31		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 480V, I_D = 17 A,$ $V_{GS} = 10V,$ (see Figure 23)		66.6 9.9 33		nC nC nC
R_g	Gate Input Resistance	$f=1\text{MHz}$ Gate DC Bias=0 Test Signal Level=20mV Open Drain		2		Ω

(*) $C_{oss \text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} **Table 8: Source Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain Current Source-drain Current (pulsed)				16 64	A A
$V_{SD}(1)$	Forward On Voltage	$I_{SD} = 17 A, V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 17 A, di/dt = 100 A/\mu s$ $V_{DD} = 100 V, T_j = 25^{\circ}C$ (see Figure 21)		372 4.6 25		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 17A, di/dt = 100 A/\mu s$ $V_{DD} = 100 V, T_j = 150^{\circ}C$ (see Figure 21)		486 6.3 26		ns μC A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

Figure 3: Safe Operating Area For TO-220/
I²PAK/D²PAK

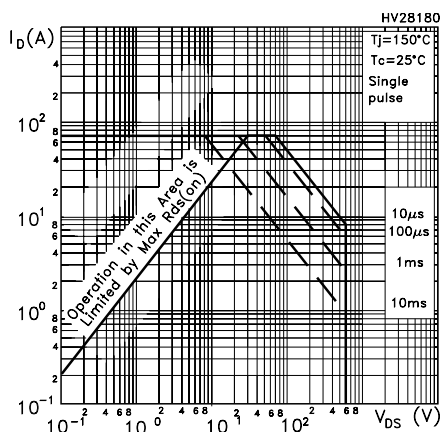


Figure 4: Safe Operating Area For TO-220FP

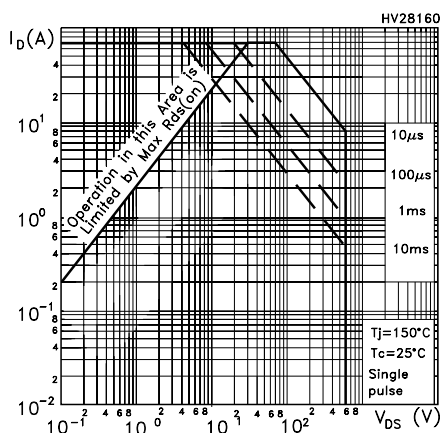


Figure 5: Safe Operating Area For TO-247

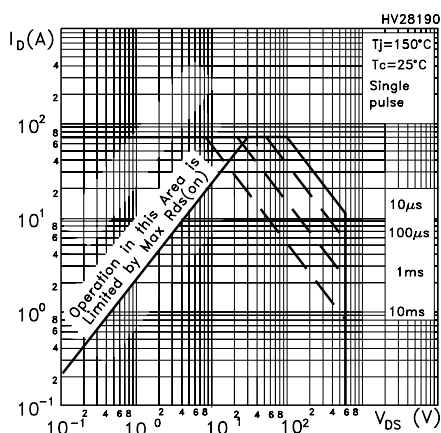


Figure 6: Thermal Impedance TO-220/I²PAK/
D²PAK

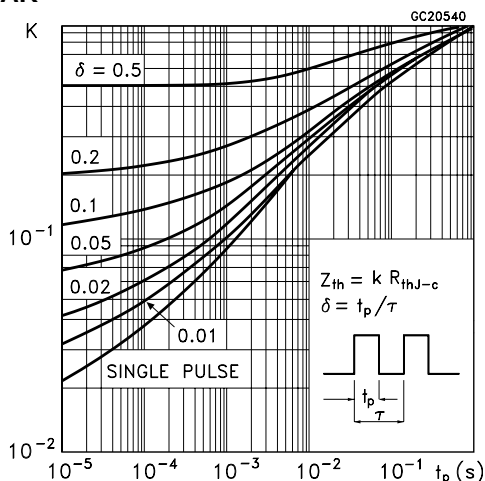


Figure 7: Thermal Impedance For TO-220FP

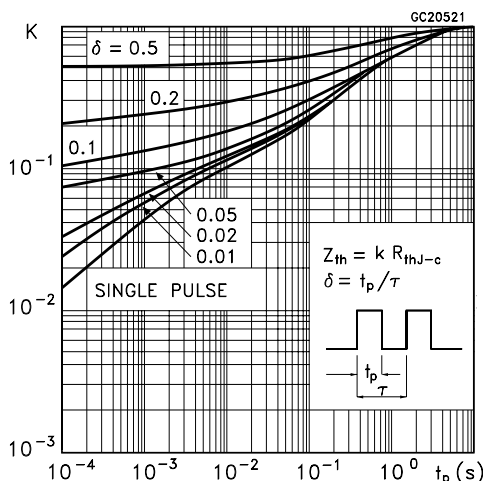


Figure 8: Thermal Impedance For TO-247

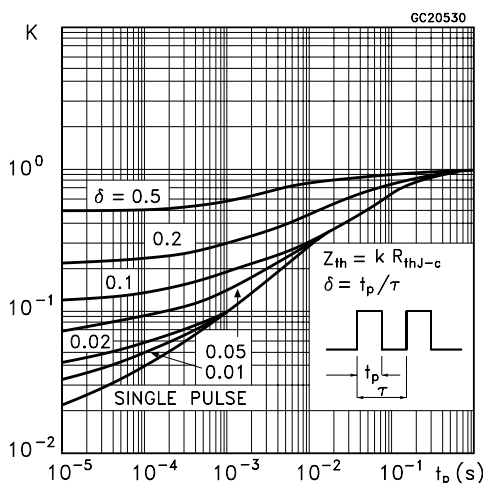


Figure 9: Output Characteristics
Output Characteristics

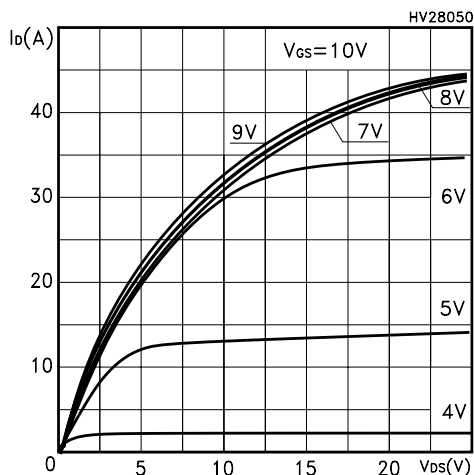


Figure 10: Transconductance

Figure 12: Transfer Characteristics

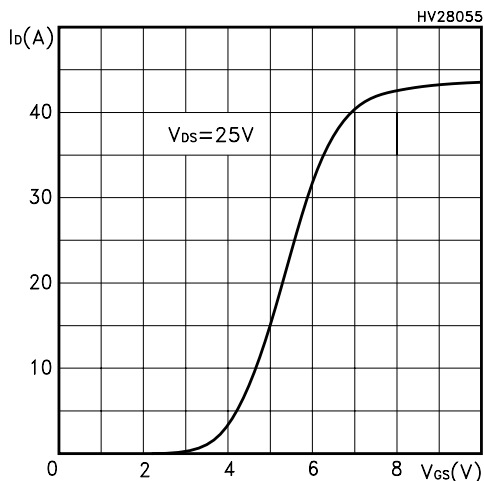


Figure 13: Static Drain-Source On Resistance

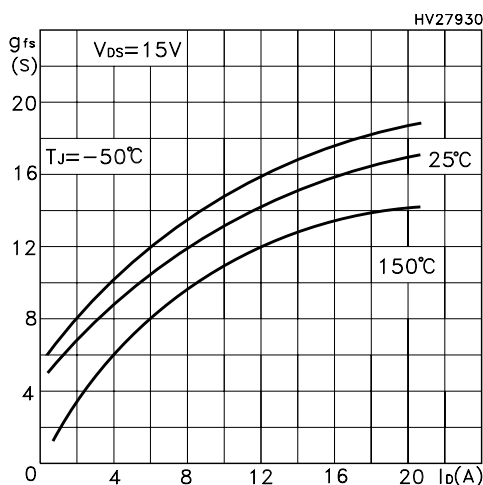


Figure 11: Gate Charge vs Gate-source Voltage

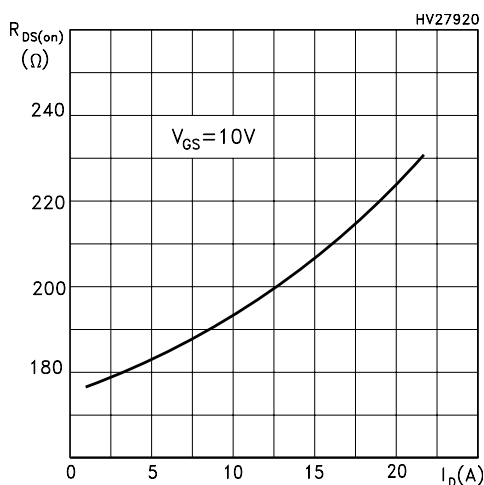


Figure 14: Capacitance Variations

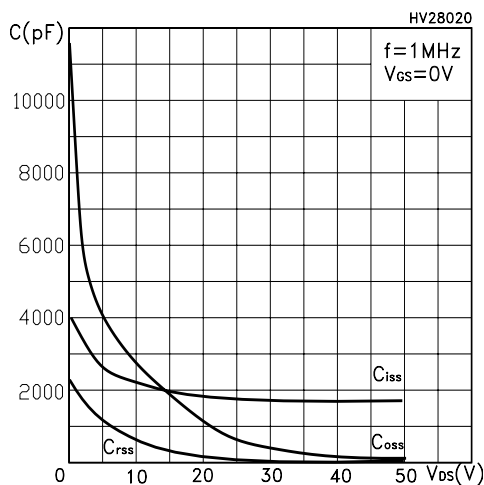
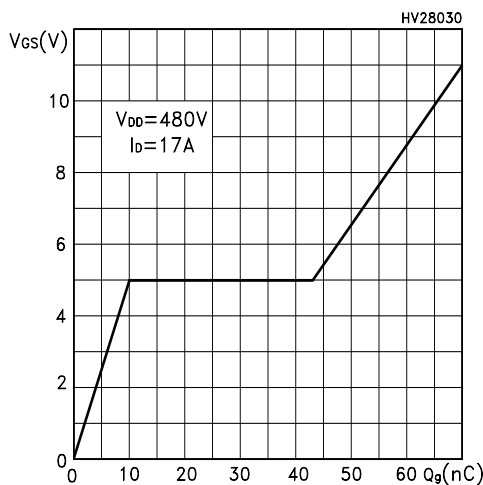


Figure 15: Normalized Gate Threshold Voltage vs Temperature

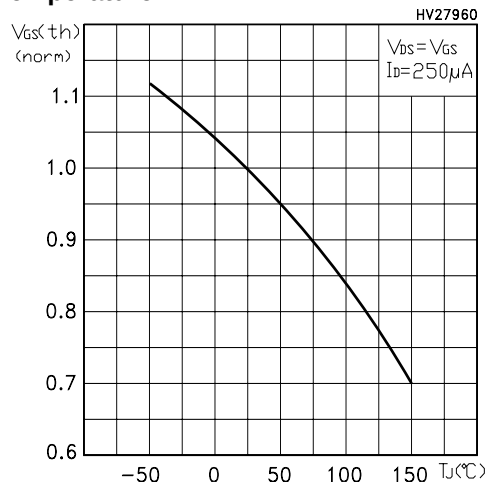


Figure 16: Source-Drain Forward Characteristics

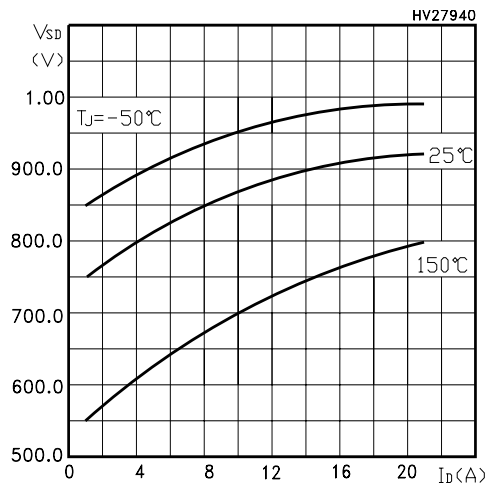


Figure 17: Normalized On Resistance vs Temperature

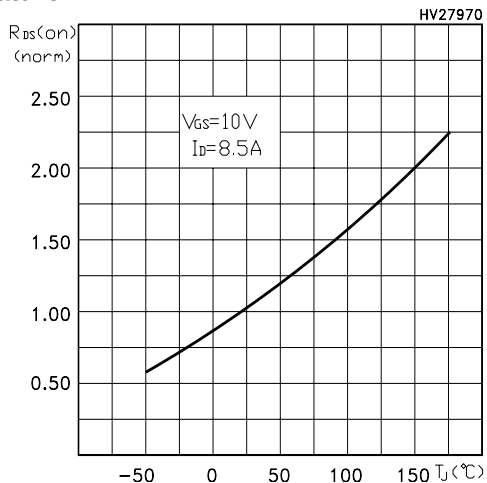


Figure 18: Normalized BV_{DSS} vs Temperature

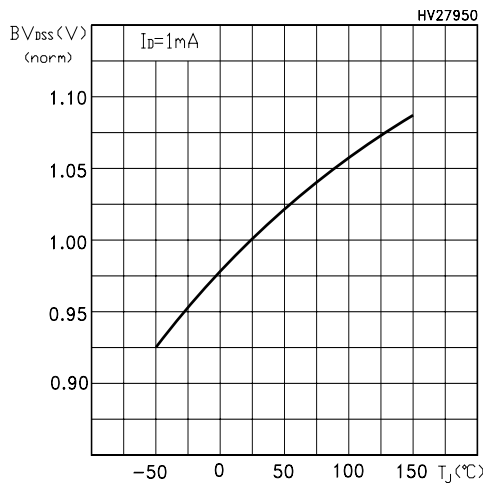


Figure 19: Unclamped Inductive Load Test Circuit

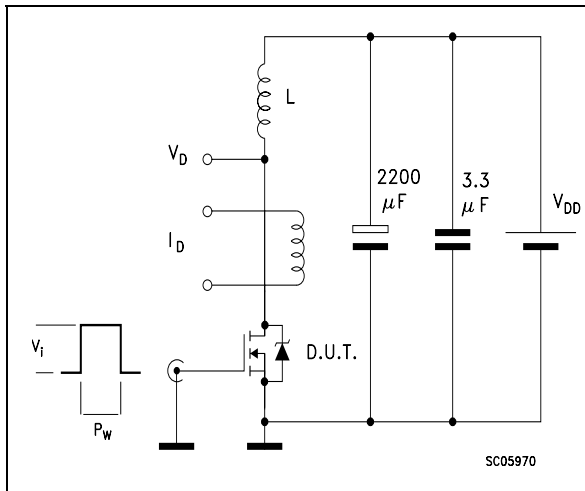


Figure 20: Switching Times Test Circuit For Resistive Load

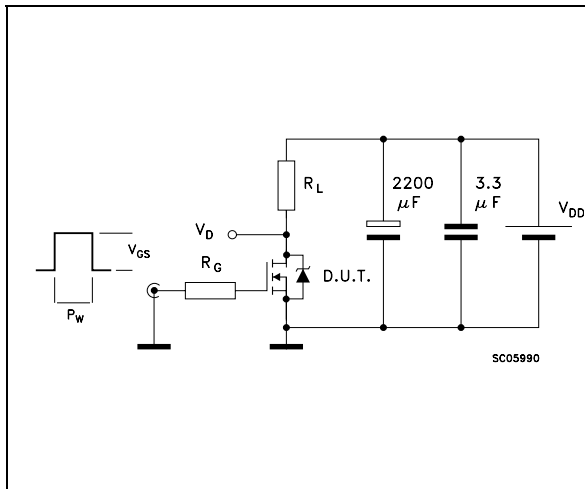


Figure 21: Test Circuit For Inductive Load Switching and Diode Recovery Times

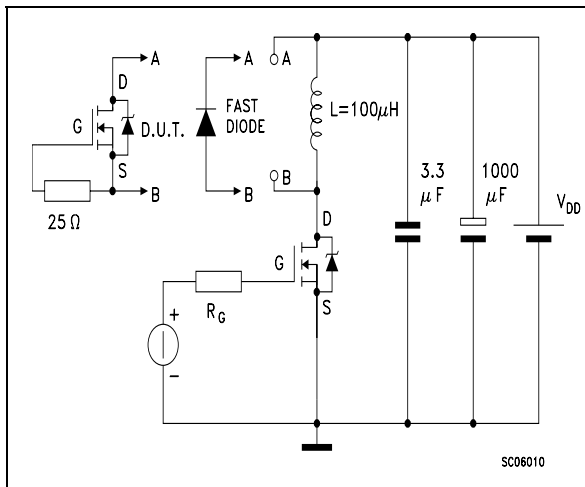


Figure 22: Unclamped Inductive Waform

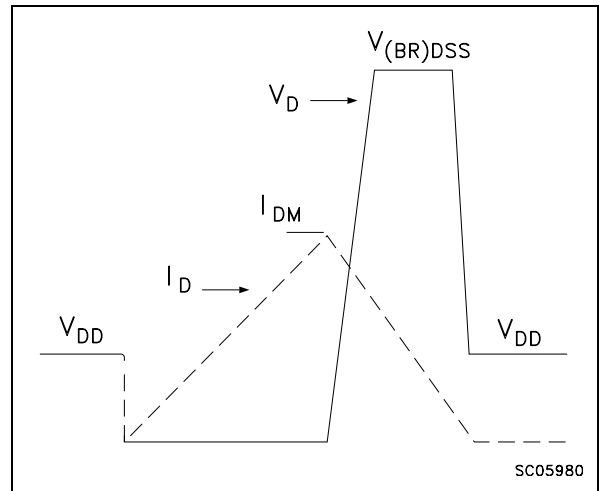
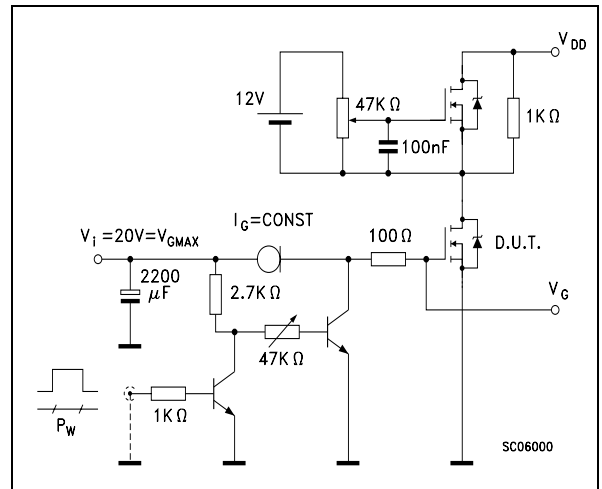
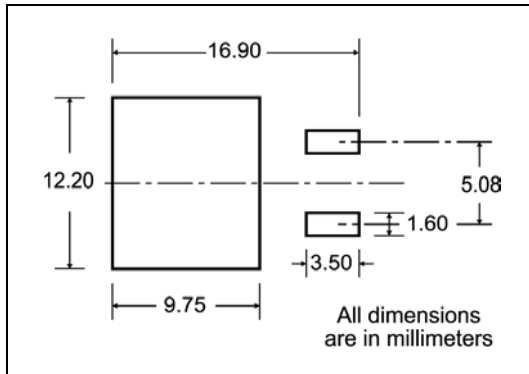


Figure 23: Gate Charge Test Circuit

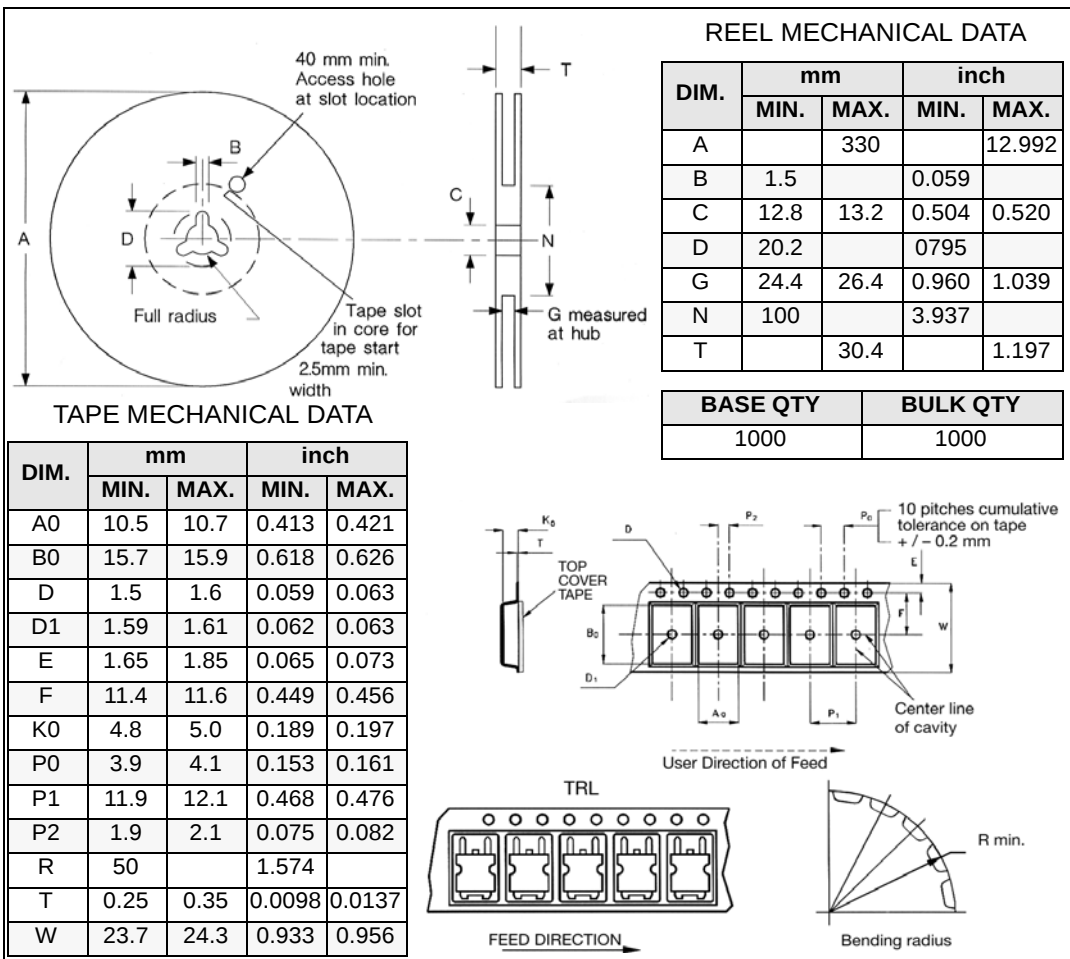


In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

D²PAK FOOTPRINT



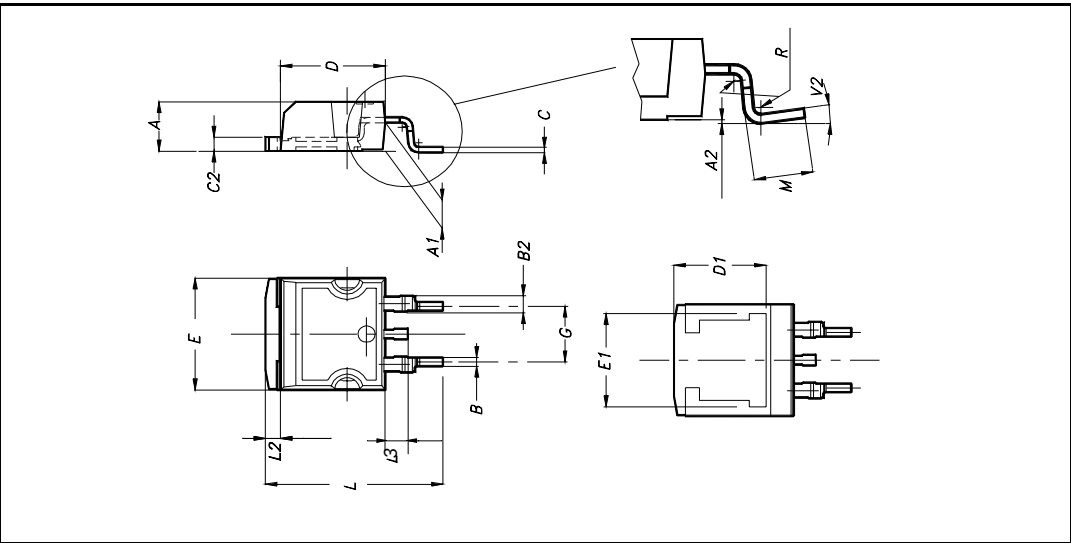
TAPE AND REEL SHIPMENT



* on sales type

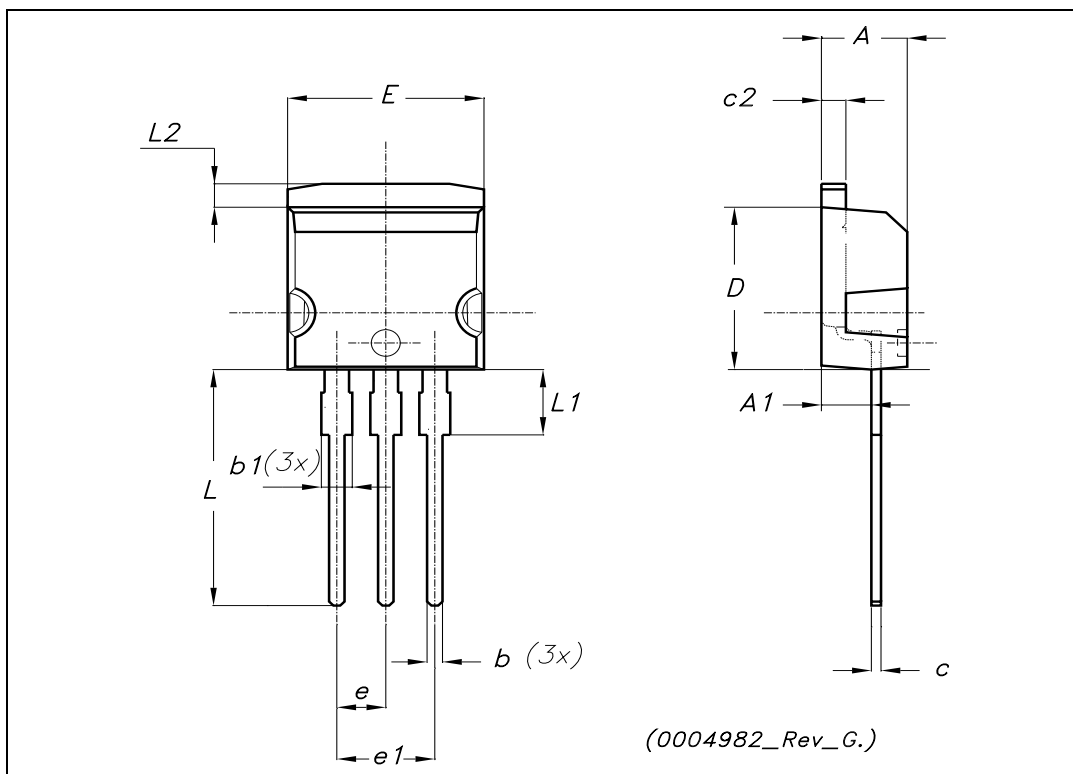
D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



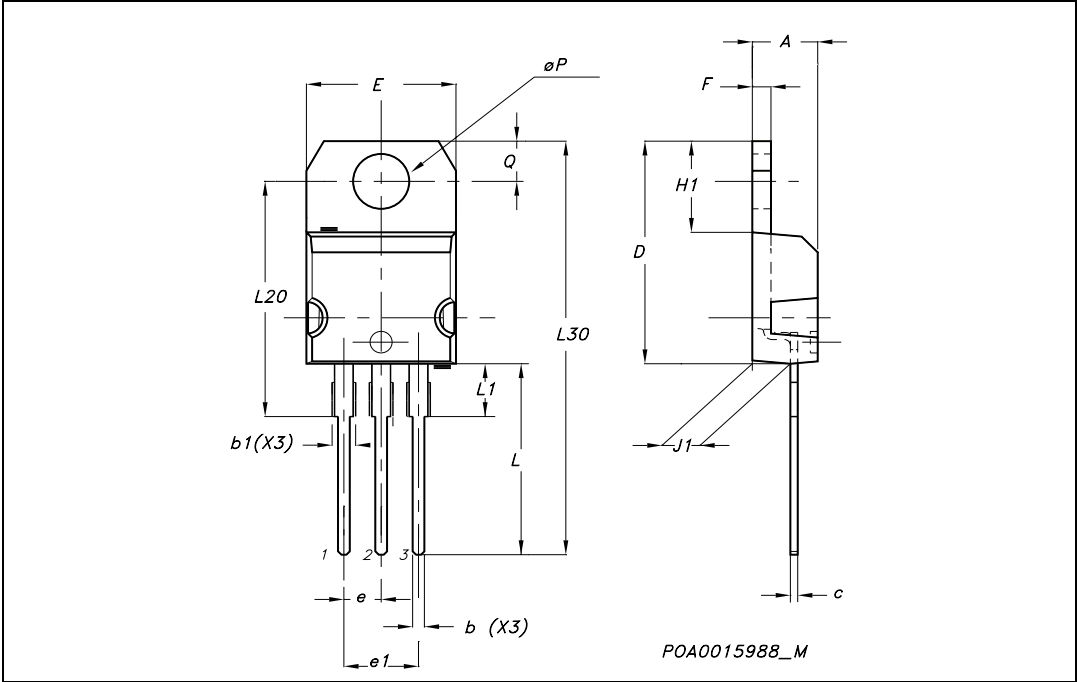
TO-262 (I²PAK) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
A1	2.40		2.72	0.094		0.107
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
c2	1.23		1.32	0.048		0.052
D	8.95		9.35	0.352		0.368
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
E	10		10.40	0.393		0.410
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L2	1.27		1.40	0.050		0.055



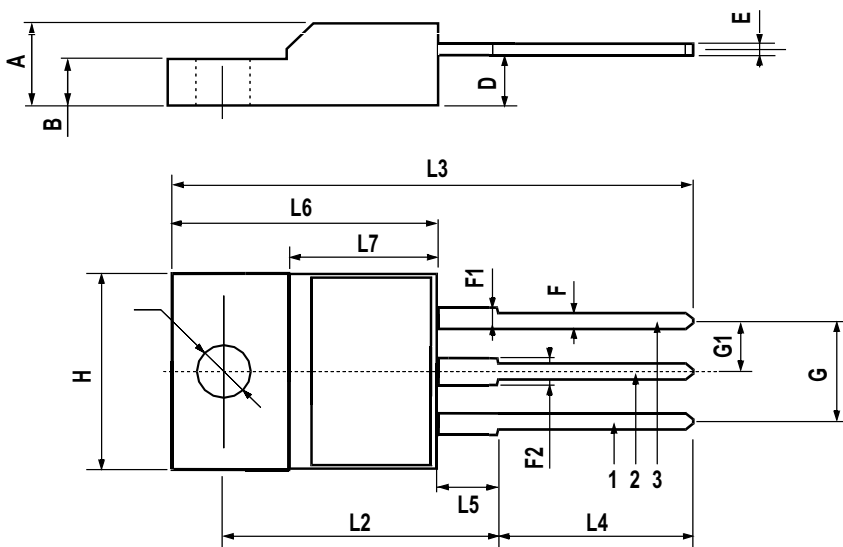
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	

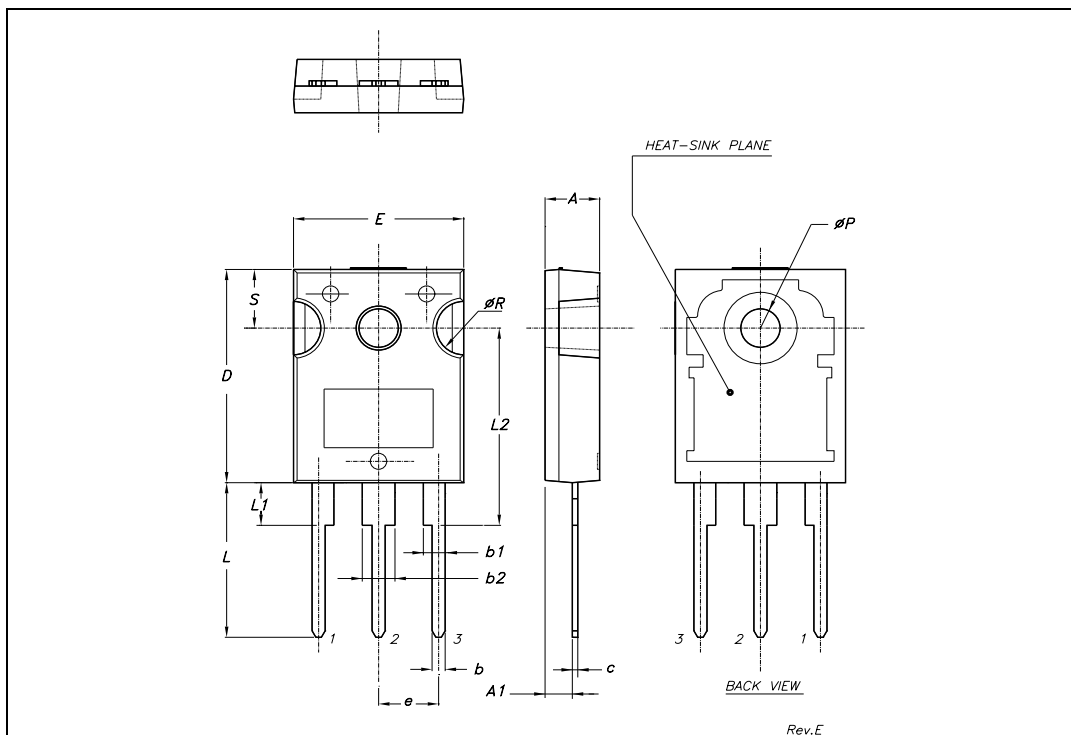


Table 9: Revision History

Date	Revision	Description of Changes
22-Sep-2005	1	First Release.
05-Oct-2005	2	Modified curves 9-12
26-Oct-2005	3	Complete version

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics

All other names are the property of their respective owners

© 2005 STMicroelectronics - All Rights Reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America