National Semiconductor

PRELIMINARY
April 9, 2008

LMH1982
Multi-Rate Video Clock Generator with Genlock

General Description

The LMH1982 is a multi-rate video clock generator ideal for use in a wide range of 3-Gbps (3G), high-definition (HD), and standard-definition (SD) video applications, such as video synchronization, serial digital interface (SDI) serializer and deserializer (SerDes), video conversion, video editing, and other broadcast and professional video systems.

The LMH1982 can generate two simultaneous SD and HD clocks and a Top of Frame (TOF) pulse. In genlock mode, the device's phase locked loops (PLLs) can synchronize the output signals to H sync and V sync input signals applied to either of the reference ports. The input reference can have analog timing from National's LMH1981 multi-format video sync separator or digital timing from an SDI deserializer and should conform to the major SD and HD standards. When a loss of reference occurs, the device can default to free run operation where the output timing accuracy will be determined by the external bias on the free run control voltage input.

The LMH1982 can replace discrete PLLs and field-programmable gate array (FPGA) PLLs with multiple voltage controlled crystal oscillators (VCXOs). Only one 27.0000 MHz VCXO and loop filter are externally required for genlock mode. The external loop filter as well as programmable PLL parameters can provide narrow loop bandwidths to minimize jitter transfer. HD clock output jitter as low as 40 ps peak-to-peak can help designers using FPGA serializers meet stringent SDI output jitter specifications.

The LMH1982 is offered in a space-saving 5 mm x 5 mm 32-pin LLP package and provides low total power dissipation of 250 mW (typical).

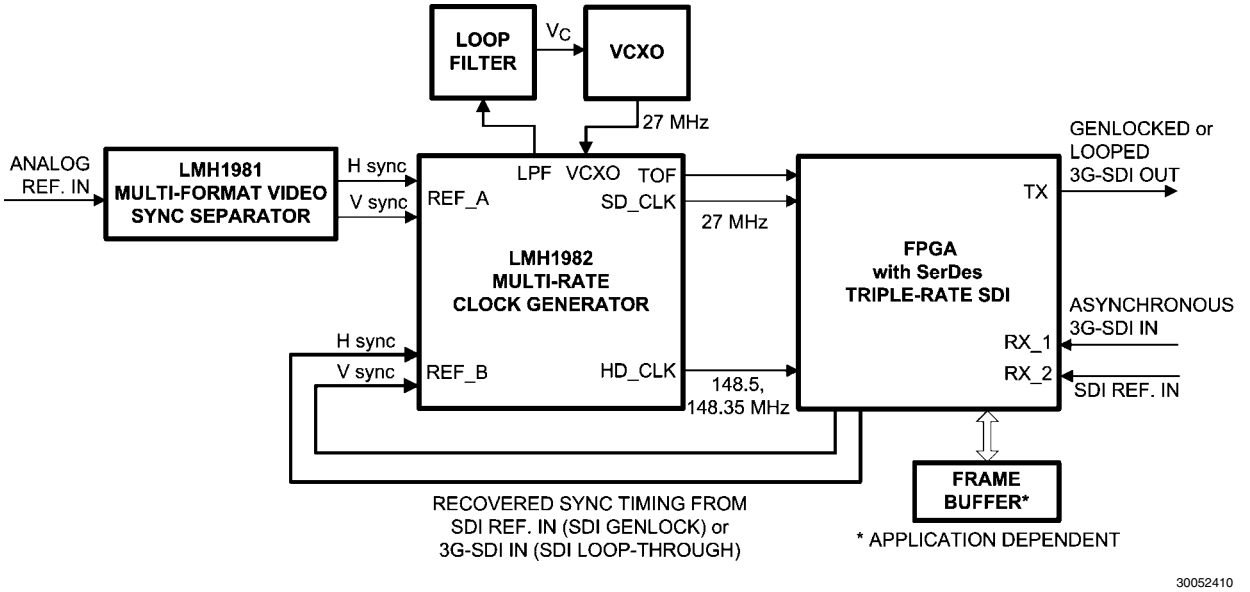
Features

- Two simultaneous LVDS output clocks with selectable frequencies and Hi-Z capability:
  - SD clock: 27 MHz or 67.5 MHz
  - HD clock: 74.25 MHz, 74.25/1.001 MHz, 148.5 MHz or 148.5/1.001 MHz
- Low-jitter output clocks may be directly connected to an FPGA serializer to meet SMPTE SDI jitter specifications
- Top of Frame (TOF) pulse with programmable output format timing and Hi-Z capability
- Two reference ports (A and B) with H and V sync inputs
- Supports cross-locking of input and output timing
- External loop filter allows control of loop bandwidth, jitter transfer, and lock time characteristics
- Free run or Holdover operation on loss of reference
- User-defined free run control voltage input
- I²C interface and control registers
- 3.3V and 2.5V supplies

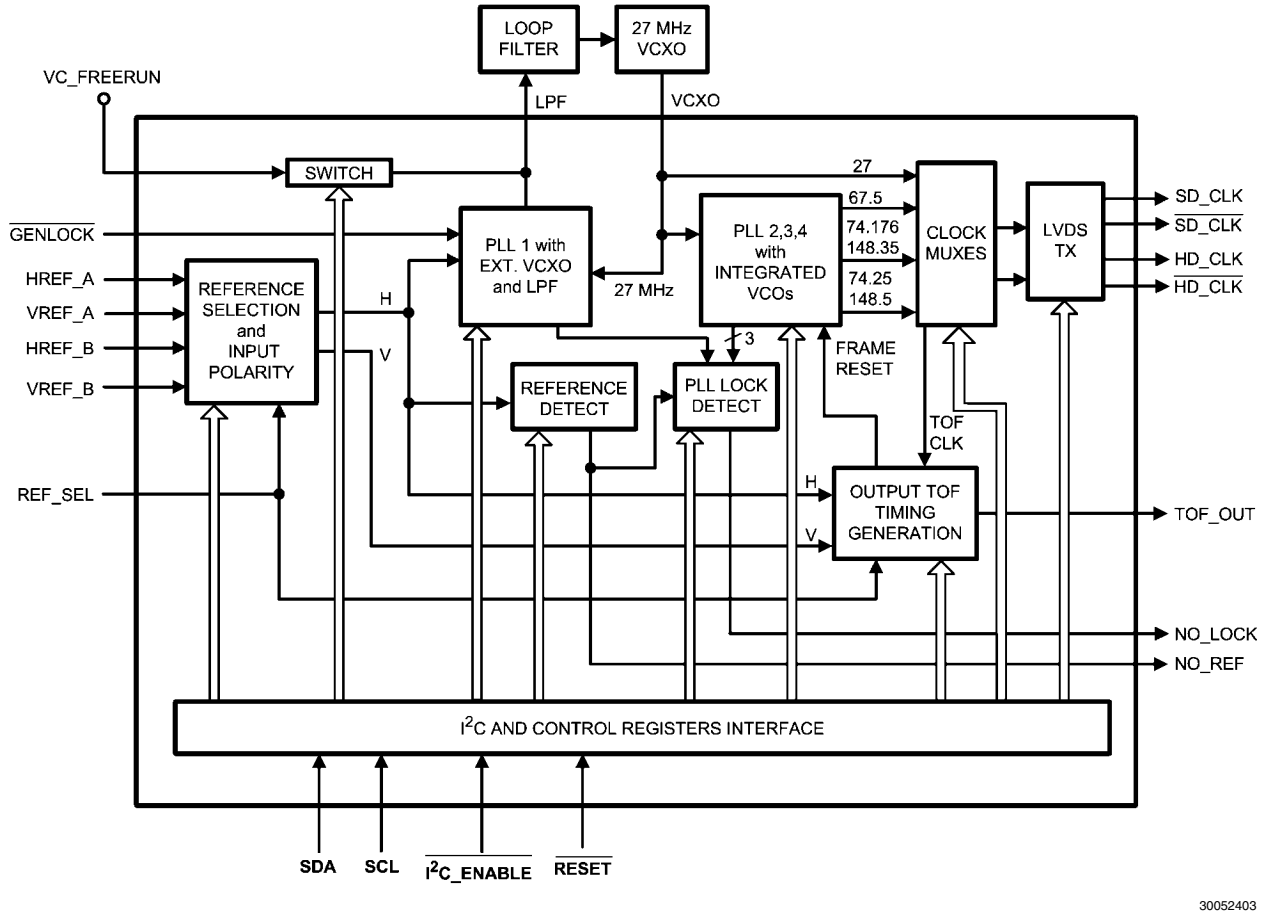
Applications

- Video genlock and synchronization
- Triple rate 3G/HD/SD-SDI SerDes
- Video capture, conversion, editing and distribution
- Video displays and projectors
- Broadcast and professional video equipment

Typical System Block Diagram



Functional Block Diagram



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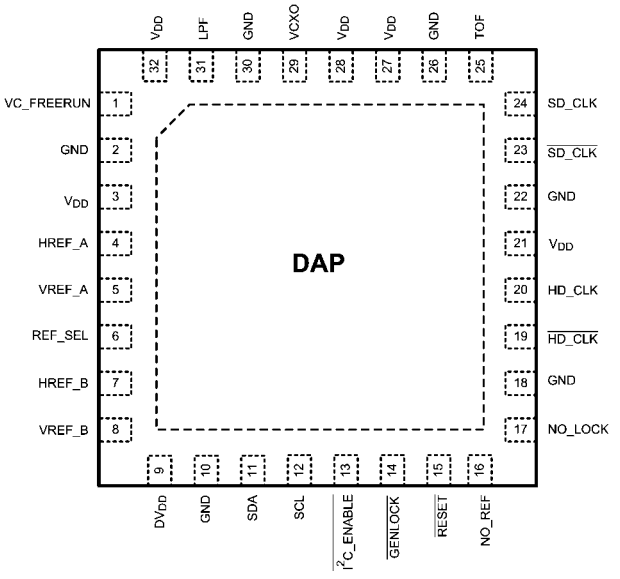
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
32-Pin LLP	LMH1982SQE	L1982SQ	250 Units Tape and Reel	SQA32A
	LMH1982SQ		1k Units Tape and Reel	
	LMH1982SQX		4.5k Units Tape and Reel	

Connection Diagram



Top View

Pin Descriptions

Pin No.	Pin Name	I/O	Signal Level	Pin Description
–	DAP	–	Supply	Die Attach Pad (Connect to GND)
1	VC_FREERUN	I	Analog	Free Run Control Voltage Input
2, 10, 18, 22, 26, 30	GND	–	Supply	Ground
3, 21, 27, 28, 32	V_{DD}	–	Supply	3.3V Supply
4	HREF_A	I	LVCMOS	H sync Input, Reference A
5	VREF_A	I	LVCMOS	V sync Input, Reference A
6	REF_SEL	I	LVCMOS	Reference Select [1, 2]
7	HREF_B	I	LVCMOS	H sync Input, Reference B
8	VREF_B	I	LVCMOS	V sync Input, Reference B
9	DV_{DD}	–	Supply	2.5V Supply
11	SDA	I/O	I²C	I²C Data [3]
12	SCL	I	I²C	I²C Clock [3]
13	$\overline{\text{I2C\_ENABLE}}$	I	LVCMOS	I²C Enable
14	$\overline{\text{GENLOCK}}$	I	LVCMOS	Mode Select [4]
15	$\overline{\text{RESET}}$	I	LVCMOS	Device Reset
16	NO_REF	O	LVCMOS	Reference Status Flag
17	NO_LOCK	O	LVCMOS	Lock Status Flag
19, 20	$\overline{\text{HD\_CLK}}$, HD_CLK	O	LVDS	HD Clock Output
23, 24	$\overline{\text{SD\_CLK}}$, SD_CLK	O	LVDS	SD Clock Output
25	TOF	O	LVCMOS	Top of Frame Pulse
29	VCXO	I	LVCMOS	VCXO Clock Input
31	LPF	O	Analog	VCXO PLL Loop Filter

Notes

1. To control reference selection via the REF_SEL input pin instead of the I²C interface (default), program I²C_RSEL = 0 (register 00h).
2. To override reference control via pin 6 and instead use pin 6 as an logic pulse input for output alignment initialization, program PIN6_OVRD = 1 (register 02h). Consequently, reference selection must be controlled via I²C, and the TOF_INIT bit (register 0Ah) will be ignored.
3. SDA and SCL pins each require a 4.7kΩ (typ.) pull-up resistor to the V_{DD} supply.
4. To control mode selection via the $\overline{\text{GENLOCK}}$ input pin instead of the I²C interface (default), program I²C_GNLK = 0 (register 00h).

Table of Contents

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	2000V
Machine Model	200V
Supply Voltage, V_{DD}	3.6V
Supply Voltage, DV_{DD}	2.75V
Input Voltage Range (any input)	−0.3V to V_{DD} +0.3V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10 sec.)	300°C
Junction Temperature, T_{JMAX}	150°C
Thermal Resistance (θ_{JA})	33°C/W

Operating Ratings

V_{DD}	3.3V ± 5%
DV_{DD}	2.5V ± 5%
Input Voltage	0V to V_{DD}
Temperature Range, T_A	0°C to 70°C

Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V_{DD} = 3.3V, DV_{DD} = 2.5V, **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{VDD}	V_{DD} Supply Current	Default Register Values		50		mA
I_{DVDD}	DV_{DD} Supply Current	Default Register Values		35		mA
Free Run Voltage Control Input (Pin 1)						
V_{IL}	Low Analog Input Voltage	(Note 3)		0		V
V_{IH}	High Analog Input Voltage	(Note 3)		V_{DD}		V
Reference Inputs (Pins 4, 5, 7, 8)						
V_{IL}	Low Input Voltage	I_{IN} = ±10 µA	0		0.8	V
V_{IH}	High Input Voltage	I_{IN} = ±10 µA	2.0		V_{DD}	V
ΔT_{HV}	H-V Timing Offset	(Note 4), Timing offset measured from H sync to V sync pulse leading edges			2.0	µs
Digital Control Inputs (Pins 6, 13, 14, 15)						
V_{IL}	Low Input Voltage	I_{IN} = ±10 µA	0		0.8	V
V_{IH}	High Input Voltage	I_{IN} = ±10 µA	2.0		V_{DD}	V
I²C Interface (Pins 11, 12)						
V_{IL}	Low Input Voltage		0		0.3 V_{DD}	V
V_{IH}	High Input Voltage		0.7 V_{DD}		V_{DD}	V
I_{IN}	Input Current	V_{IN} between 0.1 V_{DD} and 0.9 V_{DD}	−10		+10	µA
I_{OL}	Low Output Sink Current	V_{OL} = 0V or 0.4V		3		mA
Status Flag Outputs (Pin 16, 17)						
V_{OL}	Low Output Voltage	I_{OUT} = +10 mA			0.4	V
V_{OH}	High Output Voltage	I_{OUT} = −10 mA	V_{DD} −0.4V			V
Top of Frame Output (Pin 25)						
V_{OL}	Low Output Voltage	I_{OUT} = +10 mA			0.4	V
V_{OH}	High Output Voltage	I_{OUT} = −10 mA	V_{DD} −0.4V			V
I_{OZ}	Output Hi-Z Leakage Current	TOF = Hi-Z, V_{OUT} = V_{DD} or GND		0.4	10	|µA|
t_R	Rise Time	15 pF Load		1.5		ns
t_F	Fall Time	15 pF Load		1.5		ns
t_{OD}	Maximum delay time from 50% TOF_CLK active edge to 50% TOF leading edge	Output Alignment Mode Disabled (EN_TOF_RST = 0)		1		pixel period

Clock Outputs (Pins 19, 20, 23, 24)

$Jitter_{SD}$	27 MHz Time Interval Error (TIE) Peak-to-Peak Output Jitter (Note 5)	HD_CLK = Hi-Z		23		ps
	27 MHz TIE Peak-to-Peak Output Jitter(Note 5)	HD_CLK = 74.176 MHz		40		ps
	67.5 MHz TIE Peak-to-Peak Output Jitter (Note 5)	HD_CLK = 74.176 MHz		50		ps
$Jitter_{HD}$	74.176 MHz TIE Peak-to-Peak Output Jitter (Note 5)	SD_CLK = Hi-Z		55		ps
	74.25 MHz TIE Peak-to-Peak Output Jitter (Note 5)	SD_CLK = Hi-Z		40		ps
	148.35 MHz TIE Peak-to-Peak Output Jitter (Note 5)	SD_CLK = Hi-Z		60		ps
	148.5 MHz TIE Peak-to-Peak Output Jitter (Note 5)	SD_CLK = Hi-Z		45		ps
V_{OD}	Differential Signal Output Voltage	100Ω Differential Load	247	350	454	mV
V_{OS}	Common Signal Output Voltage	100Ω Differential Load	1.125	1.250	1.375	V
$\lvert\Delta V_{OD}\rvert$	|Change to V_{OD}| for Complementary Output States	100Ω Differential Load			50	|mV|
$\lvert\Delta V_{OS}\rvert$	|Change to V_{OS}| for Complementary Output States	100Ω Differential Load			50	|mV|
I_{OS}	Output Short Circuit Current	V_{CLK} and $\overline{V_{CLK}}$ = GND			24	|mA|
I_{OZ}	Output Hi-Z Leakage Current	CLK = Hi-Z, V_{CLK} = V_{DD} or GND		1	10	|µA|

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)

Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 3: The input voltage to VC_FREERUN (pin 1) should also be within the input range of the external VCXO. The input voltage should be clean from noise that may significantly modulate the VCXO control voltage and consequently produce output jitter during free run operation.

Note 4: ΔT_{HV} is required specification to allow for proper frame decoding and subsequent output alignment. For interlace formats, the H-V timing offset must be within ΔT_{HV} for all even fields and be outside ΔT_{HV} for odd fields. For progressive formats, the H-V timing offset must be within ΔT_{HV} for all frames. See sections *4.2 Internal Reference Frame Decoder* and *5.2.5 Output Frame Line Offset.*

Note 5: The SD and HD clock output jitter is based on VCXO clock with 20 ps TIE peak-to-peak jitter. The TIE peak-to-peak jitter (typical) was measured on the LMH1982 evaluation bench board using a Tektronix DSA70604 oscilloscope with TDSJIT3 jitter analysis software and 1 GHz differential probe.

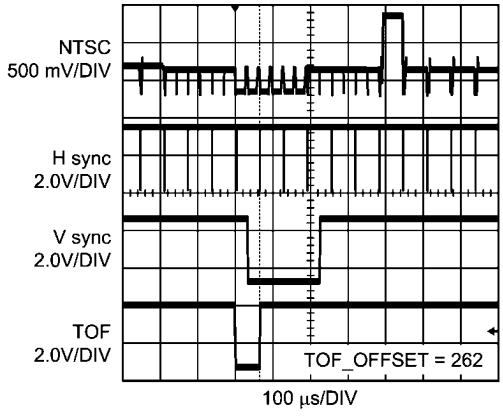
TIE Measurement Setup: 10^{-12} bit error rate (BER) and ≈1M samples recorded over multiple acquisitions. The number of acquisitions to record ≈1M samples varied with clock frequency.

Oscilloscope Setup: 20 mV/div vertical scale, 100 us/div horizontal scale, and 25 Gs/s sampling rate.

Typical Performance Characteristics

Note: Test conditions: V_{DD} = 3.3V, D_{VDD} = 2.5V, analog video reference from Tektronix TG700 AVG7 (SD video module) and AWVG7 (HD video module), H sync and V sync inputs from the LMH1981.

NTSC TOF Pulse



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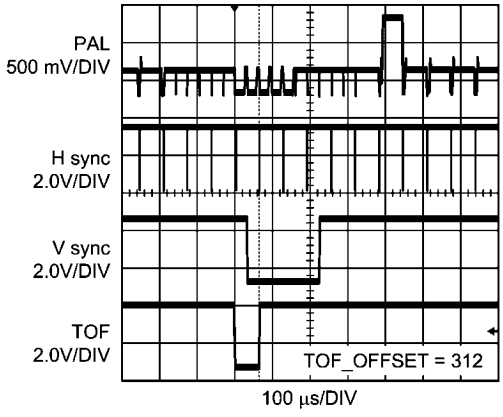
PAL TOF Pulse



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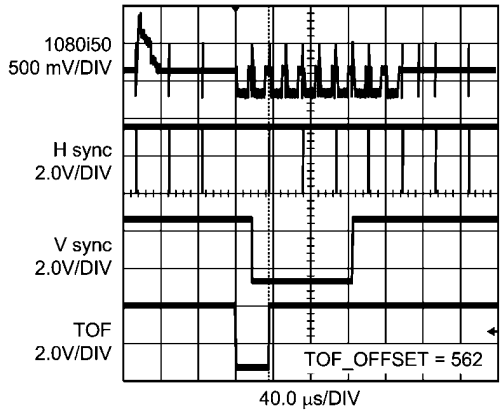
1080i50 TOF Pulse



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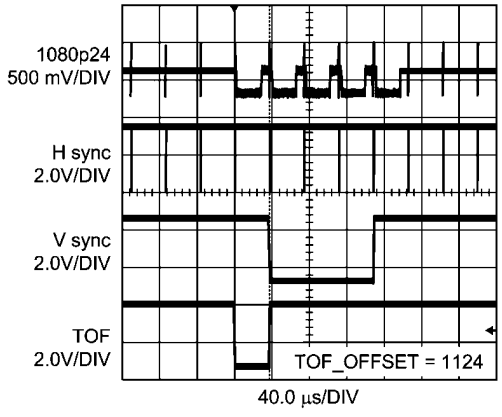
1080p24 TOF Pulse



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Application Information

1.0 FUNCTIONAL OVERVIEW

The LMH1982 is an analog phase locked loop (PLL) clock generator that can output simultaneous SD and HD video clocks synchronized or "genlocked" to H sync and V sync input reference timing. The LMH1982 features an output Top of Frame (TOF) pulse generator with programmable timing that can also be synchronized to the reference frame. Two reference ports are provided to allow a secondary input to be selected.

The clock generator uses a two-stage PLL architecture. The first stage is a VCXO-based PLL (PLL 1) that requires an external 27 MHz VCXO and loop filter. In Genlock mode, PLL 1 can phase lock the VCXO clock to the input reference after programming the PLL divider ratio. The use of a VCXO provides a low phase noise clock source even when the LMH1982 is configured with a low loop bandwidth, which is necessary to attenuate input timing jitter for minimum jitter transfer. The combination of the external VCXO, external loop filter, and programmable PLL parameters can provide flexibility for the system designer to optimize the loop bandwidth and loop response for the application.

The second stage consists of three PLLs (PLL 2, 3, 4) with integrated VCOs and loop filters. These PLLs will attempt to continually track the reference VCXO clock phase from PLL 1 regardless of the device mode. The second stage PLLs have pre-configured divider ratios to provide frequency multiplication or translation from the VCXO clock frequency. The VCO PLLs use a high loop bandwidth to assure PLL stability, so the VCXO must provide a stable low-jitter clock reference to ensure optimal output jitter performance.

Any unused clock output can be put in Hi-Z mode, which can be useful for reducing power dissipation as well as reducing jitter or phase noise on the active clock output.

The TOF pulse can be programmed to indicate the start (top) of frame and even provide format cross-locking. The output format registers should be programmed to specify the output timing format, the output timing offset relative to the reference, and the initial alignment of reference clock and TOF pulse to the reference frame. If unused, the TOF output can also be put in Hi-Z mode.

When a loss of reference occurs during genlock, PLL 1 can default to either Free run or Holdover operation. When free run is selected, the output frequency accuracy will be determined by the external bias on the free run control voltage input pin, VC_FREERUN. When Holdover is selected, the loop filter can hold the control voltage to maintain short-term output phase accuracy for a brief period in order to allow the application to select the secondary input reference and re-lock the outputs. These options in combination with proper PLL 1 loop response design can provide flexibility to manage output clock behavior during loss and re-acquisition of the reference.

The reference status and PLL lock status flags can provide real-time status indication to the application system. The loss of reference and lock detection thresholds can also be configured.

TABLE 1. LMH1982 PLL and Clock Summary

PLL	Input Reference	Divider Ratio (reduced)	Output Clock Frequency (MHz)	Output Port
PLL 1	H sync	Programmable	27	SD_CLK
PLL 2	VCXO clock	11/4 or 11/2	74.25 or 148.5	HD_CLK
PLL 3	VCXO clock	250/91 or 500/91	74.25/1.001 (74.176) or 148.5/1.001 (148.35)	HD_CLK
PLL 4	VCXO clock	5/2	67.5	SD_CLK

2.0 GENERAL PROGRAMMING INFORMATION

The LMH1982 can be configured by programming the control registers via the I²C interface. The $\overline{\text{I²C\_ENABLE}}$ pin must be set low or tied to GND to allow I²C communication; otherwise, the LMH1982 will not acknowledge communication. The I²C slave addresses are DCh for write sequences and DDh for read sequences. See section *8.0 I²C INTERFACE PROTOCOL* and *9.0 I²C INTERFACE CONTROL REGISTER DEFINITIONS*.

2.1 Recommended Start-Up Programming Sequence

The following programming sequence is necessary to ensure proper operation of the 148.35 MHz output clock following any power-up or reset condition. This sequence is also necessary after changing from any other HD clock frequency or Hi-Z mode.

1. Program HD_FREQ = 11b and HD_HIZ = 0 (register 08h) to select and enable the 148.35 MHz HD clock.
2. Program a value of 1 to the following register parameters:
   - FB_DIV = 1 (register 04h-05h)
   - TOF_RST = 1 (register 09h-0Ah)
   - REF_LPFM = 1 (register 0Dh-0Eh)
   - EN_TOF_RST = 1 (register 0Ah)
3. Wait at least 1 period of the 27 MHz VCXO clock.
4. Program EN_TOF_RST = 0.

Once this sequence is completed, the 148.35 MHz clock will operate correctly and normal device configuration can resume. Otherwise, the 148.35 MHz clock may have glitches or errors until the internal counters of PLL 3 are reset by the programming sequence above. All other output clocks do not require this reset sequence for proper operation.

2.2 Enabling Genlock Mode

Upon device power up or reset, the default mode of operation is Free Run mode. To enable Genlock mode, set GNLK = 1 (register 00h). Refer to section *3.2 Genlock Mode*.

2.3 Output Disturbance While Alignment Mode Enabled

While the output alignment mode is enabled (EN_TOF_RST = 1) and maintained beyond the initial alignment (initialization), the output signals can be abruptly phase-aligned to the reference on every output frame. Continual alignment can cause excessive phase "jumps" or jitter on the output clock edge coinciding with the TOF pulse; this effect is unavoidable and can be caused by slight differences in the internal counter reset timing for the TOF generation and large input jitter. The characteristic of the output jitter can also vary in severity from process variation, part variation, and the selected clock reference frequency. . This output jitter can only be inhibited by

setting EN_TOF_RST = 0 after the output alignment and before the subsequent output frame.

3.0 MODES OF OPERATION

The mode of operation describes the operation of the VCXO PLL, which can operate in either Free Run mode or Genlock mode depending on the GNLK bit setting. If desired, the $\overline{\text{GENLOCK}}$ input pin can be instead used to control the mode of operation by initially setting I²C_GNLK = 0 (register 00h).

3.1 Free Run Mode

The LMH1982 will enter Free Run mode when GNLK is set to 0. In Free Run mode, the VCXO will be free-running and independent of the input reference, and the output clocks will maintain phase lock to the VCXO clock reference. Therefore, the output clocks will have the same accuracy as the VCXO clock reference.

The LMH1982 provides the designer with the option to define the VCXO's free run control voltage by external biasing of the VC_FREERUN input (pin 1). The analog bias voltage applied to the VC_FREERUN input will be internally connected to the LPF output (pin 31) though a low impedance switch, as shown in section *Functional Block Diagram*. The resultant voltage at the LPF output will drive the control input of the VCXO to set its free run output frequency. Thus, the pull range of the VCXO imparts the same pull range on the free run output clocks.

If VC_FREERUN is left floating, the VCXO control voltage will be pulled to GND potential as the residual charge stored across the loop filter will discharge through any existing leakage path.

3.2 Genlock Mode

The LMH1982 will enter Genlock mode when GNLK is set to 1. In Genlock mode, the VCXO PLL can be phase locked to the reference H sync input of the selected port; once the VCXO PLL clock reference is locked and stable, the output clocks and TOF pulse can be aligned and phase locked to the reference. The LMH1982 supports cross-locking, which allows the outputs to be frame-locked to a reference format that is different from the output format.

To genlock the outputs, the following programming sequence is suggested:

1. Program the output clock frequency for the desired output format. Refer to section *4.1 Programming The VCXO PLL Dividers*.
2. Program the output TOF timing for the desired output format. Refer to section *5.2 Programming The Output Timing Format*. It is necessary to complete this step for proper output clock alignment even when the TOF pulse is not required.
3. Program the VCXO PLL divider registers for the input reference format. Refer to section *4.1 Programming The VCXO PLL Dividers*.
4. Program GNLK = 1 to enable Genlock mode. See the note below.
5. Program the output alignment to the desired reference frame. Refer to section *5.3 Programming The Output Alignment Sequence*.

Note: When Genlock mode is enabled, the LMH1982 will attempt to phase lock the PLLs to the input reference regardless of input timing stability. Timing errors or instability on the inputs will cause the PLLs and outputs to also have instability. If output stability is a consideration during periods of input uncertainty, it is suggested to gate off the input signals from the LMH1982 until they are completely stable. Input signal gating can be achieved externally using a discrete or FPGA logic buffer with Hi-Z (tri-state) output and a pull-up or pull-down resistor, depending on the input pulse signal polarity.

3.2.1 Genlock Mode State Diagram

Figure 1 shows the Genlock mode state diagram for different input reference and PLL lock conditions. It also includes Free Run and Holdover states for the loss of reference operation, specified by the HOLDOVER bit (register 00h). Each state indicates the NO_REF and NO_LOCK status flag output conditions.

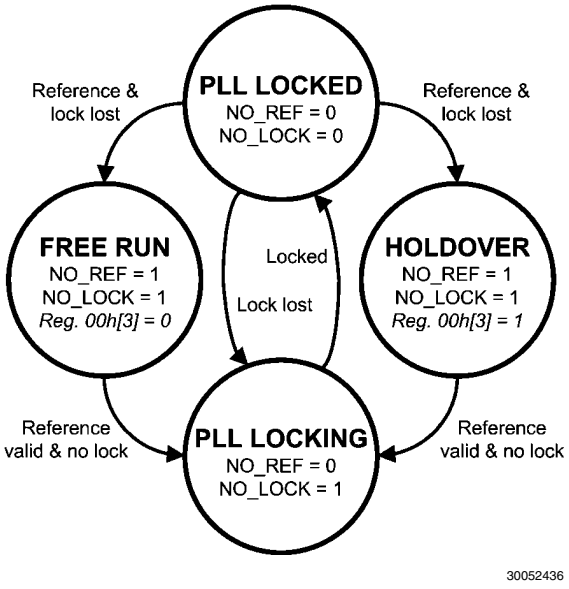


FIGURE 1. Genlock Mode State Diagram

3.2.2 Loss of Reference (LOR)

By configuring the HOLDOVER bit, the LMH1982 can default to either Free Run or Holdover operation when a loss of reference (LOR) occurs in Genlock mode.

If HOLDOVER = 0 when a LOR occurs, the LMH1982 will default to Free run operation (section *3.2.2.1 Free Run during LOR*) until a reference is reapplied.

If HOLDOVER = 1 when a LOR occurs, the LMH1982 will default to Holdover operation (section *3.2.2.2 Holdover during LOR*) until a reference is reapplied.

When the input reference is reapplied, the LMH1982 will immediately attempt to phase lock the output clocks to the reference.

3.2.2.1 Free Run during LOR

Free Run mode (GNLK = 0) differs from Free Run operation due to LOR in Genlock mode (GNLK = 1) in the following way. In Free Run mode, the outputs will free run regardless of the presence or loss of reference. In Genlock mode, the outputs will free run only during LOR; once a reference is present, free run operation will cease as the PLLs will immediately attempt to phase lock the output clocks to the reference.

3.2.2.2 Holdover during LOR

In Holdover operation, the LPF output is put into high impedance mode, which allows the loop filter to temporarily hold the residual charge stored across it (i.e. the control voltage) immediately after LOR is indicated by the NO_REF status flag. Holdover operation can help to temporarily sustain the output clock accuracy upon LOR. The duration that the residual control voltage level can be sustained within a toler-

able level depends primarily on the charge leakage on the loop filter. A typical VCXO has an input impedance of several tens of kΩ, which will be the dominant leakage path seen by the loop filter. As the leakage current discharges the residual control voltage to GND, the output frequencies of the VCXO and LMH1982 will drift accordingly. If a longer time constant is required, a precision op amp with low input bias current and rail-to-rail input and output (e.g. LMP7701) can be used to buffer the control voltage. The buffer will isolate the relatively low input impedance of the VCXO and reduce the charge leakage on the loop filter during Holdover.

The output frequency accuracy will degrade as the VCXO accuracy drifts with the decaying control voltage. Moreover, because the H_ERROR setting (register 00h) affects the reference error threshold for LOR indication, a higher setting for H_ERROR may result in reduced output accuracy upon LOR indication compared to when H_ERROR = 0. For more information on programming H_ERROR, see section *6.1.1 Programming the Loss of Reference (LOR) Threshold*.

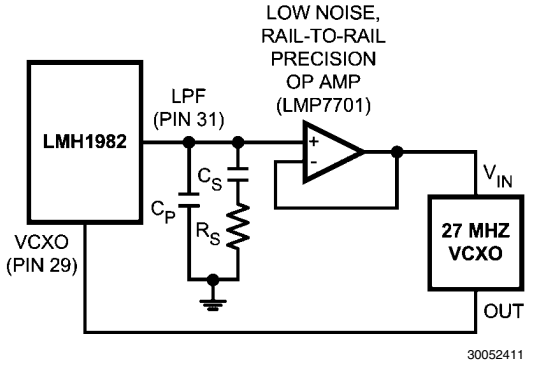


FIGURE 2. Optional Buffer to Isolate VCXO Input Impedance from the Loop Filter

3.3 Recognized Video Timing Formats And Standards

Table 2 lists the supported video timing standard formats and various timing parameter values that can be used to program the device registers related to the input reference and output formats.

TABLE 2. Supported Video Timing Formats and Timing Parameter Values

Video Standard	Video Format	Pixel Clock Frequency (MHz)	Total Pixels per Line	Total Lines per Frame	Frame Rate (Hz)	H Freq (kHz)	REF_DIV[1] Register 03h	FB_DIV[1] Register 04h-05h
SMPTE 125M/ 267M	NTSC/525I	27	1716	525	29.97	15.734	1	1716
ITU-R BT.601-5	PAL/625I	27	1728	625	25	15.625	1	1728
SMPTE 293M	525P/59.94	27	858	525	59.94	31.469	1	858
ITU-R BT.1358	625P/50	27	864	625	50	31.250	1	864
SMPTE 296M	1280x720/60/P	74.25	1650	750	60	45.000	1	600
	1280x720/59.94/P	74.176	1650	750	59.94	44.955	2	3003
	1280x720/50/P	74.25	1980	750	50	37.500	1	720
	1280x720/30/P	74.25	3300	750	30	22.500	1	1200
	1280x720/29.97/P	74.176	3300	750	29.97	22.478	2	6006
	1280x720/25/P	74.25	3960	750	25	18.750	1	1440
	1280x720/24/P	74.25	4125	750	24	18.000	1	1500
	1280x720/23.98/P	74.176	4125	750	23.98	17.982	0	3003
SMPTE 274M	1920x1080/60/P	148.5	2200	1125	60	67.500	1	400
	1920x1080/59.94/P	148.35	2200	1125	59.94	67.433	2	2002
	1920x1080/50/P	148.5	2640	1125	50	56.250	1	480
	1920x1080/30/P	74.25	2200	1125	30	33.750	1	800
	1920x1080/29.97/P	74.176	2200	1125	29.97	33.716	2	4004
	1920x1080/25/P	74.25	2640	1125	25	28.125	1	960
	1920x1080/24/P	74.25	2750	1125	24	27.000	1	1000
	1920x1080/23.98/P	74.176	2750	1125	23.98	26.973	1	1001
SMPTE 274M	1920x1080/60/I	74.25	2200	1125	30	33.750	1	800
	1920x1080/59.94/I	74.176	2200	1125	29.97	33.716	2	4004
	1920x1080/50/I	74.25	2640	1125	25	28.125	1	960

Notes
1. Other PLL divider values may be compatible as described in section *4.1 Programming The VCXO PLL Dividers.*

4.0 INPUT REFERENCE

The LMH1982 features two reference ports (A and B) with H sync and V sync inputs which are used for phase locking the outputs in Genlock mode. The reference port can be selected by programming RSEL (register 00h). If desired, REF_SEL input can be used instead to select the reference port by initially setting I²C_RSEL = 0 (register 00h).

The reference signals should be 3.3V LVCMOS signals within the input voltage range specified in the Electrical Characteristics table. The H sync and V sync input signals may have analog timing, such as from the LMH1981 multi-format analog video sync separator, or digital timing, such as from an FPGA SDI deserializer.

4.1 Programming The VCXO PLL Dividers

To genlock the outputs to the reference, it is necessary to phase lock the VCXO PLL clock to the H sync input signal by programming its dividers. The PLL divider values are determined by the following ratio:

f_{VCXO} / f_{HSYNC} = Feedback Divider / Reference Divider

Where:

f_{VCXO} = 27 MHz VCXO frequency

f_{HSYNC} = H sync input frequency

Feedback Divider = 1 to 8191

Reference Divider = 1, 2 or 5

The reference divider value can be selected from *Table 3* and programmed to REF_DIV (register 03h). The feedback divider value can be selected from *Table 4* and programmed to FB_DIV (register 04h-05h).

TABLE 3. VCXO PLL Reference Divider Selection

REF_DIV Register 03h	Reference Divider Value
00b	2
01b	1
10b	5

TABLE 4. VCXO PLL Feedback Divider Selection

FB_DIV Register 04h-05h	Feedback Divider Value
0...00	Invalid
0...01	1
:	:
1...10	8190
1...11	8191

Table 2 shows the recognized input formats with the corresponding reference and feedback divider values, which are based on the ratio reduced to its lowest factors. Some reference formats can have up to three sets of compatible divider values with the same reduced ratio. For example, a 1080p60 input reference has three sets of compatible divider values of 400/1 (reduced), 800/2 and 2000/5. Because the divider values can directly influence the loop response of the VCXO PLL, the programmability of these registers can be used advantageously by the designer. Refer to section *7.0 VCXO PLL LOOP RESPONSE* for more information.

4.2 Internal Reference Frame Decoder

The LMH1982 features an internal frame decoder to monitor the input H sync and V sync pulses and decode the reference frame timing, which eliminates the need for an odd/even field timing input pin. The reference frame timing is required to allow for proper frame alignment between the output clock and TOF pulse and the reference.

To allow for proper frame decoding and subsequent output alignment, the H sync and V sync input signals must comply with the H-V timing offset specification, ΔT_{HV}, as described here. For interlace formats, the H-V timing offset must be within ΔT_{HV} for even fields and be outside ΔT_{HV} for odd fields. Compliance with this specification will ensure the internal frame counters are reset only once per frame instead of twice. For progressive formats, the H-V timing offset must be within ΔT_{HV} for all frames.

For analog timing from the LMH1981 sync separator, the H and V pulses will comply with the ΔT_{HV} specification for any input reference format.

For digital timing from an FPGA SDI deserializer, the recovered H and V pulses may be co-timed and within ΔT_{HV} for **both** odd and even fields. This will cause the internal frame counters to reset twice per frame and thus preclude proper frame decoding and output alignment. As a simple workaround, the designer may choose to configure the FPGA to gate the V sync signal, allowing only the even field V pulses and gating off the odd field V pulses.

5.0 OUTPUT CLOCKS AND TOF

The LMH1982 has simultaneous LVDS output SD and HD clocks and an output TOF pulse. The output timing characteristics must be specified by register programming outlined in the following section.

5.1 Programming The Output Clock Frequencies

The SD clock frequency can be selected from *Table 5* and programmed to SD_FREQ (register 08h). PLL 1 and PLL 4 are used to generate the two SD clock rates but only one SD clock can be selected at a time. If the SD_CLK output is not needed, it can be put in Hi-Z mode by setting SD_HIZ = 1 (register 08h).

If 27 MHz is selected, the VCXO clock is directly converted from a 3.3V single-ended clock the VCXO input (pin 29) to an LVDS clock at the SD_CLK output port (pins 23 and 24). If 67.5 MHz is selected, the VCXO clock is used as an input reference for PLL 4 to generate this SD clock frequency. A 67.5 MHz clock is required instead of 27 MHz as an SD reference clock in some FPGA SD-SDI SerDes applications.

TABLE 5. SD Clock Frequency Selection

SD_CLK (MHz)	SD_FREQ Register 08h	PLL#
27	0b	1
67.5	1b	4

The HD clock frequency can be selected from *Table 6* and programmed to HD_FREQ (register 08h). PLL 2 and PLL 3 are used to generate the four different HD clock rates but only one HD clock can be selected at a time. If the HD_CLK output is not needed, it can be put in Hi-Z mode by setting HD_HIZ = 1 (register 08h).

Note: If 148.35 MHz is selected, it is recommended to follow the initial programming sequence described in section *2.1 Recommended Start-Up Programming Sequence*.

TABLE 6. HD Clock Frequency Selection

HD_CLK (MHz)	HD_FREQ Register 08h	PLL#
74.25	00b	2
74.25/1.001	01b	3
148.5	10b	2
148.5/1.001	11b	3

5.2 Programming The Output Timing Format

When the VCXO PLL is stable and locked to the input reference, the output clock and TOF pulse can be programmed to be aligned to the desired reference frame. Before implementing the output alignment sequence, the desired output timing format (i.e. output clock and TOF pulse) needs to be specified first. The reference and output timing formats must be fully and correctly specified by programming the output format registers 09h-12h. The output format registers define the following parameters:

- Output Clock Reference
- Output Frame Rate
- Reference Frame Timing
- Input-Output Frame Rate Ratio
- Output Frame Line Offset

Once the output format registers are programmed according to sections 5.2.1 to 5.2.5, the output alignment procedure can then be implemented as described in section 5.3.

5.2.1 Output Clock Reference

The TOF pulse is derived from internal pixel, line, and frame counters and can be made synchronous to either the SD_CLK or HD_CLK, depending on the desired output format. The output clock reference for timing the TOF pulse should be selected by setting TOF_CLK (register 0Ch).

The TOF pulse output delay time (t_{OD}) relative to the selected clock will be deterministic and is specified in the Electrical Characteristics table. For example, *Figure 3* and *Figure 4* show the typical t_{OD} for 525i and 1080i50 output timing, respectively. The width of the TOF pulse will be approximately one line period of the programmed output format.

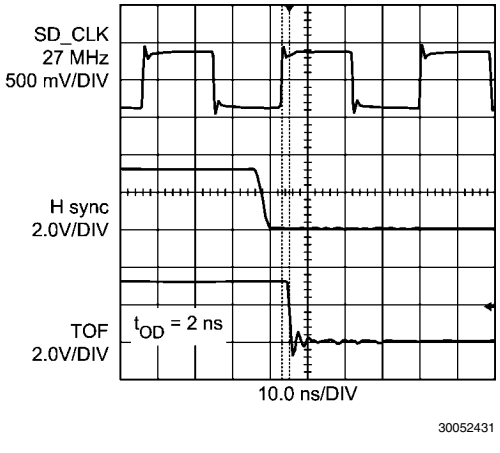


FIGURE 3. 525i TOF Output Delay Time Relative to 27 MHz

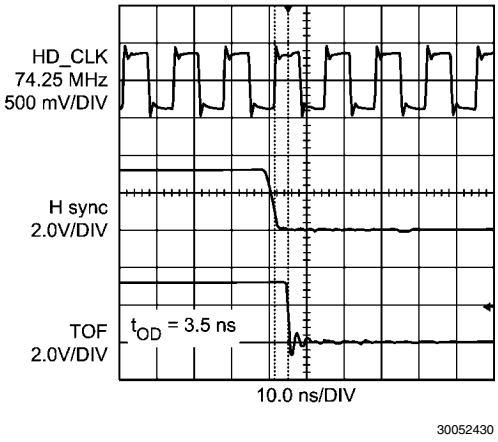


FIGURE 4. 1080i50 TOF Output Delay Time Relative to 74.25 MHz

5.2.2 Output Frame Rate

The output format frame rate (TOF pulse rate) can be calculated as:

TOF rate = f_{TOF_CLK} / (TOF_PPL x TOF_LPFM)

Where:

f_{TOF_CLK} = Clock reference frequency
TOF_PPL = Total pixels per output line
TOF_LPFM = Total lines per output frame

The output frame rate should be specified by programming TOF_CLK, TOF_PPL (register 0Bh-0Ch) and TOF_LPFM (0Dh-0Eh) based on the desired output format.

For example, if the output format is 625i, then:

TOF rate = 27 MHz / (1728 x 625) = 25 Hz frame rate

Where:

f_{TOF_CLK} = 27 MHz (SD_FREQ = 0)
TOF_PPL = 1728
TOF_LPFM = 625

5.2.3 Reference Frame Rate

The reference frame timing is generated internally and used for resetting the internal counters for output TOF generation. The reference frame rate should be specified by programming the total reference lines per frame to REF_LPFM (register 0Fh-10h).

5.2.4 Input-Output Frame Rate Ratio

The input-output frame rate ratio is also used for resetting the internal counters for output TOF generation. The ratio is the Input frame rate / Output frame rate, in which the numerator and denominator values are reduced to lowest integer factors. The numerator value of this reduced ratio should be programmed to TOF_RST (register 09h-0Ah), and the denominator value is discarded.

For example, if the input reference is 525i with a frame rate of 30/1.001 Hz, and the output format is 625i with a frame rate of 25 Hz, then TOF_RST = 1200:

Frame rate ratio = (30 / 1.001) / 25 = **1200** / 1001

5.2.5 Output Frame Line Offset

The output clock and TOF pulse can be aligned to any line of the reference frame by specifying TOF_OFFSET (register 11h-12h) and subsequently programming the output align-

ment sequence. The line offset value programmed to TOF_OFFSET can delay or advance the output alignment relative to the reference line where the input H and V pulse are within ΔT_{HV} (see section *4.2 Internal Reference Frame Decoder*).

TOF_OFFSET must be greater than zero but less than or equal to the total lines per reference frame. If no line offset is required, then set TOF_OFFSET equal to REF_LPFM instead of zero (invalid).

TABLE 7. TOF Line Offset Selection

Register 11h-12h TOF_OFFSET	Line Offset Value for Output Alignment
0...00	Invalid
0...01	1
:	:
1...10	4094
1...11	4095

For example, if an input reference with PAL timing comes from the LMH1981, the H and V pulses will be aligned to within ΔT_{HV} for the even field V pulses which occur on line 313 of the reference. In this case, TOF_OFFSET can be set to 312d so the output frame will align to Line 1 of the PAL reference (start of frame) after the output alignment is subsequently implemented. This example is illustrated in *Figure 5*.

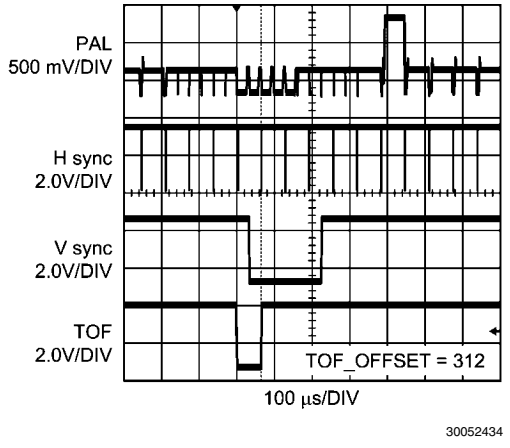


FIGURE 5. PAL Reference and Output TOF Pulse (TOF_OFFSET = 312)

5.3 Programming The Output Alignment Sequence

Before implementing the output alignment sequence, the following prerequisites must be met as described:

1. The VCXO PLL must be stable and locked to the input reference.
2. The desired output clock and TOF pulse timing must be fully specified to the output format registers.

To ensure that the output clock and TOF pulse are properly aligned and subsequently phas locked to the reference frame, the output alignment sequence should be programmed accordingly.

During the output frame immediately prior to the frame the alignment is to occur:

1. Set EN_TOF_RST = 1(register 0Ah) to enable output alignment mode.
2. Toggle TOF_INIT (register 0Ah) from 0 to 1 to initialize the internal counters. On the next frame, the output clock and TOF pulse will be aligned to the reference frame and relative line offset based on TOF_OFFSET.
3. Immediately after the alignment and before the next output frame occurs, clear EN_TOF_RST and TOF_INIT to 0. Otherwise, the output clock will be continually aligned every output frame, which may cause excessive jitter on the output clock due to slight differences in the reset timing of the internal counters. This occurrence of excessive clock jitter can be avoided by disabling output alignment mode (EN_TOF_RST = 0) immediately after the alignment.

Note: Due to the following conditions, the TOF pulse may be delayed or offset by more than one pixel clock (t_{OD} > 1 pixel clock) even after the output alignment sequence:

1. The H sync and/or V sync input pulses have excessive jitter equal to or larger than half of a pixel period of the selected output clock. Input sync jitter less than 3 ns peak-to-peak is recommended.
2. The VCXO PLL is not completely phase locked nor stable when the output alignment is performed.

5.3.1 Output Clock Alignment without TOF

For applications that do not require the TOF pulse, it is still necessary to program all output format registers prior to the output alignment sequence. This is because the output alignment circuitry relies on the full and correct specification of the output format. If the TOF output is not needed, it can be put in Hi-Z mode by setting TOF_HIZ = 1 (register 08h).

5.4 Output Behavior Upon Loss Of Reference

After loss of reference (LOR), the LMH1982 will maintain the TOF pulse without the input reference according to the terminal counts of the reference clock; however, output frequency accuracy will be determined by the VCXO, which may be in Free Run or Holdover operation.

To disable output alignment to an arbitrary reference frame when the reference is reapplied, set EN_TOF_RST = 0 before the reference returns. After the VCXO PLL has re-locked to the reference, the outputs can be initialized to the desired reference frame.

6.0 REFERENCE AND PLL LOCK STATUS

TABLE 8. Summary of Genlock Status Bits and Flag Outputs

	Mode Control Bits Register 00h		Status Flag Outputs		Status Bits Register 01h		
Conditions	GNLK	HOLD-OVER	NO_REF [1] (pin 16)	NO_LOCK [2] (pin 17)	HD_LOCK bit 2	SD_LOCK bit 1	REF_VALID bit 0
Genlock mode, Reference valid, PLLs locking	1	X	0	1	0	0	1
Genlock mode, Reference valid, PLLs locked	1	X	0	0	1	1	1
Genlock mode, Reference lost, Free Run operation	1	0	1	1	1	0	0
Genlock mode, Reference lost, Holdover operation	1	1	1	1	1	0	0

Notes
1. NO_REF output = $\overline{\text{REF\_VALID}}$
2. NO_LOCK output = $\overline{\text{(REF\_VALID) (SD\_LOCK) (HD\_LOCK)}}$

The LMH1982 features a reference detector and PLL lock detector that can be used to indicate genlock status of the input reference and device PLLs. Genlock status can be sampled via the NO_REF and NO_LOCK output status pins and the REF_VALID, SD_LOCK, and HD_LOCK status bits (register 01h). Both the reference and PLL lock detectors may be programmed for their respective detection thresholds according to the needs of the application system.

6.1 Reference Detection

In Genlock mode, a valid reference will be indicated by NO_REF = 0 when all the criteria below are met. Otherwise, a loss of reference (LOR) will be indicated by NO_REF = 1.

The NO_REF output is the logical NOT of the REF_VALID status bit.

- An H sync signal is applied to the input reference and conforms to one of the standard formats in *Table 2*. A V sync signal is not used in reference detection.
- The PLL divide registers are programmed according to the input reference format.
- The control voltage of the VCXO is not within about 500 mV of the GND or V_{DD} supplies.

6.1.1 Programming the Loss of Reference (LOR) Threshold

The reference detector's error threshold can be programmed to H_ERROR (register 00h), which determines the maximum number of missing H sync pulses before indicating an LOR. The LOR threshold will be the H_ERROR value multiplied by the PLL reference divider value, as shown in *Table 9*.

TABLE 9. LOR Threshold Selection

REF_DIV Register 03h	Reference Divider Value	LOR Threshold
00b	2	2 x H_ERROR
01b	1	1 x H_ERROR
10b	5	5 x H_ERROR

If H_ERROR = 0, then the device will react after the first missing pulse. When the LOR threshold is exceeded, the NO_REF output will indicate LOR, and the device will default to either Free Run or Holdover operation for as long as the reference is lost. As the LOR threshold value is increased, the accuracy for counting the actual number of missing H pulses may diminish due to frequency drifting by the VCXO PLL.

Note: If the input reference is missing H pulses periodically, e.g. every vertical interval period, the PLL may not indicate a valid reference nor achieve lock regardless of the H_ERROR value programmed. This is because periodically missing pulses will translate to a lower average frequency than expected. When the average input frequency falls outside of the absolute pull range (APR) of the VCXO, the PLL will not be able to frequency lock to the input reference.

6.2 PLL Lock Detection

In Genlock mode, PLL lock will be indicated by NO_LOCK = 0 when all the criteria below are met. Otherwise, a loss of lock will be indicated by NO_LOCK = 1.

The NO_LOCK output is the logical NAND of the REF_VALID, SD_LOCK, and HD_LOCK status bits.

- A valid reference is indicated (REF_VALID = 1).
- The VCXO PLL is phase locked to the input reference (SD_LOCK = 1).
- The relevant HD clock VCO PLL is phase locked to the VCXO clock reference (HD_LOCK = 1).

The VCO PLLs have high loop bandwidths, which allow them to achieve lock quickly and concurrently while the VCXO PLL achieves lock. Because the VCXO PLL has a much lower loop bandwidth, it will dictate the overall lock indication time.

6.2.1 Programming the PLL Lock Threshold

The VCXO PLL lock detector threshold can be programmed to LOCK_CTRL (register 01h), which determines the maximum phase error between PLL 1's phase detector (PD) inputs before indicating an unlock or lock condition. The PD inputs are the reference signal (H sync input / reference divider) and the feedback signal (VCXO clock / feedback divider).

The lock detector will indicate loss of lock when the phase error between the PD inputs is greater than the lock threshold for three consecutive phase comparison periods. Conversely, it will indicate valid lock when the phase error is less than the lock threshold for three consecutive phase comparison periods.

A larger value for LOCK_CTRL will yield shorter lock indication time (although not actual lock time) at the expense of higher output phase error when lock is initially indicated, whereas a smaller value will yield the opposite effect.

6.2.2 PLL Lock Status Instability

It is possible for excessive jitter on the H input to indicate lock instability through the NO_LOCK output, even if VCXO PLL and output clocks are properly phase locked and no system-level errors are occurring (e.g. bit errors). To reduce the probability of false loss of lock indication or lock status instability, LOCK_CTRL can be increased to improve the lock detector's ability to tolerate a larger amount of input phase jitter or phase error. This can help to ensure the NO_LOCK output and SD_LOCK bit are stable when the reference signal has large input jitter.

7.0 VCXO PLL LOOP RESPONSE

The overall jitter performance of the LMH1982 is determined by the design of the VCXO PLL's loop response. Because the integrated VCO PLLs use the VCXO clock as the input reference to phase lock the output clocks, the ability of the VCXO PLL to attenuate the input jitter is critical. The loop response can be characterized by its loop bandwidth and damping factor. A lower loop bandwidth will provide higher input jitter attenuation (reduced jitter transfer) for improved output jitter characteristics. Increased lock time (or settling time) and larger external component values are a couple trade-offs to having a lower loop bandwidth.

The loop response is primarily determined by the loop filter components and the loop gain. A passive second-order loop filter consisting of R_S, C_S, and C_P components can provide sufficient input jitter attenuation for most applications, although a higher order passive filter or active filter may also be used. The loop gain is a function of the VCXO gain and programmable PLL parameters.

7.1 Loop Response Design Equations

The following equations can be used to design the loop response of the VCXO PLL.

The -3 dB loop bandwidth, BW, can be approximated by:

$$BW = I_{CP1} * R_S * K_{VCO} / FB\_DIV$$

Where:

I_{CP1} = Nominal VCXO PLL charge pump current (in amps)
programmed by setting ICP1 (register 13h).
For example:
I_{CP1} = 250 µA: ICP1 = 08h (default value)
I_{CP1} = 0 µA: ICP1 = 00h (min)
I_{CP1} = 62.5 µA; ICP1 = 02h (practical min)
I_{CP1} = 968.75 µA; ICP1 = 1Fh (max)
I_{CP1} step size = 31.25 µA

R_S = Nominal value of series resistor (in ohms)

K_{VCO} = Nominal 27 MHz VCXO gain (in Hz/V)
K_{VCO} = Pull_range * 27 MHz/Vin_range
For the recommended VCXO (CTS 357LB3I027M0000): K_{VCO} = 100 ppm * 27 MHz/ (3.0V- 0.3V) = 1000 Hz/V

FB_DIV = Feedback Divider value
For example:
FB_DIV =1716 for NTSC Hsync input

Note that this BW approximation does not take into account the effects of the damping factor or the second pole introduced by Cp.

At frequencies far above the –3 dB loop bandwidth, the closed-loop frequency response of the VCXO PLL will roll off at about –40 dB/decade, which is useful attenuating input jitter at frequencies above the loop bandwidth. Near the –3 dB corner frequency, the roll-off will depend on other factors, such as damping factor and filter order.

To prevent output jitter due to the modulation of the VCXO by the PLL's phase comparison frequency:

$$BW \leq (27\ MHz / FB\_DIV) / 20$$

The VCXO PLL damping factor, DF, can be approximated by:

$$DF = (R_S / 2) * \text{sqrt}\ (I_{CP1} * C_S * K_{VCO} / FB\_DIV)$$

Where:

C_S = Nominal value of the series capacitor (in farads)

A typical design target for DF is between 0.707 to 1, which can often yield a good trade-off between reference spur attenuation and lock time. DF is related to the phase margin, which is a measure of the PLL stability.

A secondary parallel capacitor, C_P, is needed to filter the reference spurs introduced by the PLL which may modulate the VCXO input voltage and also cause output jitter. The following relationship should be used to determine C_P:

$$C_P = C_S / 20$$

The PLL loop gain, K, can be calculated as:

$$K = I_{CP1} * K_{VCO} / FB\_DIV$$

Therefore, the BW and DF can be expressed in terms of K:

$$BW = R_S * K$$

$$DF = (R_S/2) * \text{sqrt}\ (C_S * K)$$

7.1.1 Loop Response Optimization Tips

To design and optimize the PLL response for a given loop filter across all input reference formats, it is suggested to maintain a relatively constant loop gain, K, across all expected values for FB_DIV. It is desirable to maintain a narrow range for K because the term K affects both BW and DF equations. To maintain a relatively constant K, I_{CP1} can be adjusted in proportion to the change in FB_DIV.

It is suggested to design for the loop filter component values using the BW and DF equations and initially assuming FB_DIV = 1716 (NTSC) and I_{CP1} = 250 µA (default setting). Once reasonable component values are achieved under these initial assumptions, it is necessary to check that K can be maintained over the expected range of FB_DIV by adjusting I_{CP1}. The usable current range of I_{CP1} is limited to a practical minimum of 62 µA (ICP1 = 2) to a maximum of 969 µA (ICP1 = 31), so it should provide adequate adjustment range to maintain a relatively constant value for K assuming the suggested starting values for FB_DIV and I_{CP1} were followed. If a narrow range for K cannot be maintained within the usable range of I_{CP1}, then the loop filter design may need to be modified.

In some loop response design, the calculated I_{CP1} current that is required for a target K value can be near or below the practical minimum of the I_{CP1} current range. In these situations, it may be possible to leverage the programmable VCXO PLL reference and feedback dividers by scaling up the values in proportion (i.e. same reduced divider ratio); this would allow I_{CP1} to be scaled up by the same factor to be within the usable current range. This technique of scaling FB_DIV and I_{CP1} assumes that the reference format has more than one combination of compatible divider values as explained in the latter part of section *4.1 Programming The VCXO PLL Dividers*.

7.2 Lock Time Considerations

The LMH1982 lock time or settling time is determined by the loop response of the VCXO PLL, which has a much lower loop bandwidth compared to the integrated PLLs used to derive the other output clock frequencies. Generally, the lock time is inversely proportional to the loop bandwidth; however, if the loop response is not designed or programmed for sufficient PLL stability, the lock time may not be predicted from the loop bandwidth alone. Therefore, any parameter that affects the loop response can also affect the overall lock time.

7.3 VCXO Considerations

The recommended VCXO manufacturer part number is CTS 357LB3C27M0000, which has an absolute pull range (APR) of ±50 ppm and operating temperature range of -20°C to +70° C. A VCXO with a tighter APR can provide better output frequency accuracy in Free Run operation; however, the APR must be wider than the worst-case input frequency error in order to achieve phase lock.

7.4 Free Run Output Jitter

The input voltage to VC_FREERUN (pin 1) should have sufficient filtering to minimize noise over the frequency bands of interest (i.e. SMPTE SDI jitter frequency bands) which can cause VCXO input voltage modulation and thus free run output clock jitter.

8.0 I²C INTERFACE PROTOCOL

The protocol of the I²C interface begins with the start pulse followed by a byte comprised of a seven-bit slave device address and a read/write bit as the LSB. Therefore, the address of the LMH1982 for write sequences is DCh (1101 1100) and the address for read sequences is DDh (1101 1101). *Figure 6*, *Figure 7*, and *Figure 8* show a write and read sequence across the I²C interface.

8.1 Write Sequence

The write sequence begins with a start condition, which consists of the master pulling SDA low while SCL is held high. The slave device address is sent next. The address byte is made up of an address of seven bits (7:1) and the read/write bit (0). Bit 0 is low to indicate a write operation. Each byte that is sent is followed by an acknowledge (ACK) bit. When SCL is high the master will release the SDA line. The slave must pull SDA low to acknowledge. The address of the register to be written to is sent next. Following the register address and the ACK bit, the data byte for the register is sent. When more than one data byte is sent, it is automatically incremented into the next address location. See *Figure 6*. Note that each data byte is followed by an ACK bit.

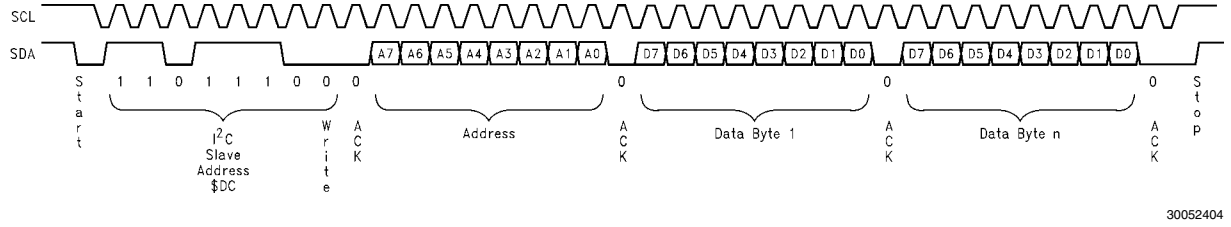


FIGURE 6. LMH1982 Write Sequence

8.2 Read Sequence

Read sequences are comprised of two I_2C transfers. The first is the address access transfer, which consists of a write sequence that transfers only the address to be accessed. The second is the data read transfer, which starts at the address accessed in the first transfer and increments to the next address per data byte read until a stop condition is encountered.

The address access transfer shown in *Figure 7* consists of a start pulse, the slave device address including the read/write bit (a zero, indicating a write), then its ACK bit. The next byte is the address to be accessed, followed by the ACK bit and the stop bit to indicate the end of the address access transfer.

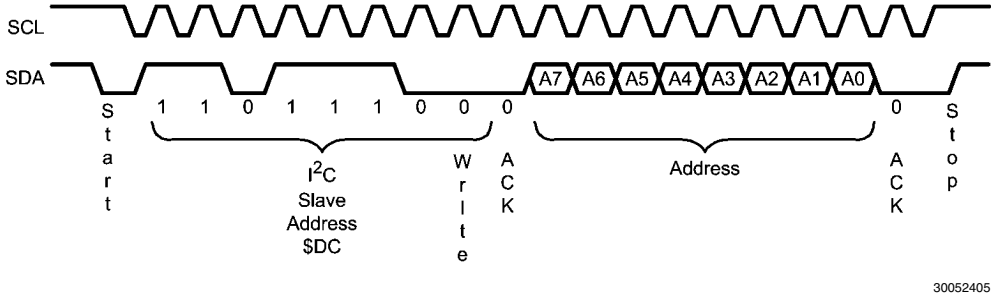


FIGURE 7. LMH1982 Read Sequence – Address Access Transfer

The subsequent read data transfer shown in *Figure 8* consists of a start pulse, the slave device address including the read/write bit (a one, indicating a read) and the ACK bit. The next byte is the data read from the initial access address. Subsequent read data bytes will correspond to the next increment address locations. Each data byte is separated from the other data bytes by an ACK bit.

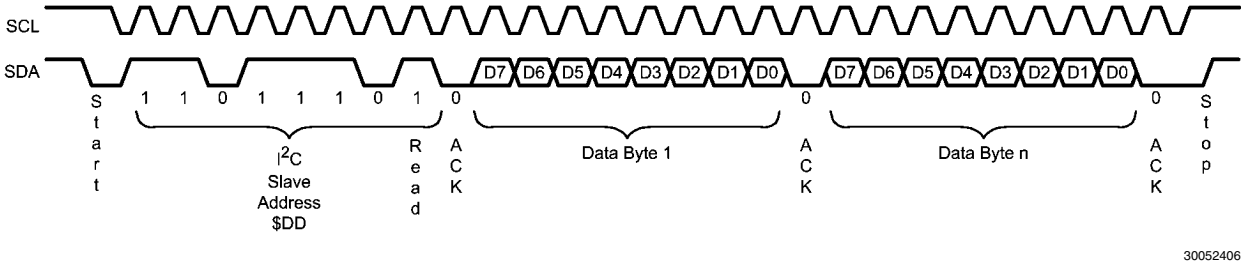


FIGURE 8. LMH1982 Read Sequence – Data Read Transfer

8.3 I²C Enable Control Pin

When the active low input $\overline{\text{I2C\_ENABLE}}$ = 0, the LMH1982 will enable I²C communication via its fixed slave address; otherwise, the LMH1982 will not respond. For applications with multiple LMH1982 devices on the same I²C bus, the I²C enable function can be useful for writing data to a specific device(s) and for reading data from an individual device to prevent bus contention. For single chip applications, the $\overline{\text{I2C\_ENABLE}}$ input can be tied to GND to keep the I²C interface enabled.

9.0 I²C INTERFACE CONTROL REGISTER DEFINITIONS

TABLE 10. I²C Interface Control Register Map

Register Address	Default Data	D7	D6	D5	D4	D3	D2	D1	D0
00h	A3h	GNLK_I²C	GNLK	RSEL_I²C	RSEL	HOLD-OVER	H_ERROR [2:0]		
01h	86h	LOCK_CTRL [7:3]					HD_LOCK	SD_LOCK	REF_VALID
02h	00h	RSV	RSV	PIN6_OVRD	REF_27	POL_HA	POL_VA	POL_HB	POL_VB
03h	01h	RSV	RSV	RSV	RSV	RSV	RSV	REF_DIV [1:0]	
04h	B4h	FB_DIV [7:0]							
05h	06h	0	0	0	FB_DIV [12:8]				
06h	00h	RSV	RSV	RSV	RSV	ICP4 [3:0]			
07h	00h	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
08h	04h	RSV	RSV	TOF_HIZ	HD_HIZ	HD_FREQ [3:2]		SD_HIZ	SD_FREQ
09h	01h	TOF_RST [7:0]							
0Ah	00h	EN_TOF_RST	POL_TOF	TOF_INIT	TOF_RST [12:8]				
0Bh	B4h	TOF_PPL [7:0]							
0Ch	06h	0	0	TOF_CLK	TOF_PPL [12:8]				
0Dh	0Dh	TOF_LPFM [7-0]							
0Eh	02h	0	0	0	0	TOF_LPFM [11:8			
0Fh	0Dh	REF_LPFM [7-0]							
10h	02h	0	0	0	0	REF_LPFM [11:8]			
11h	00h	TOF_OFFSET [7-0]							
12h	00h	0	0	0	0	TOF_OFFSET [11:8]			
13h	88h	RSV	RSV	RSV	ICP1 [4:0]				
14h	88h	ICP2 [7:4]				ICP3 [3:0]			

9.1 Genlock And Input Reference Control Registers

REGISTER 00h

Bits 2-0: H Input Error Max Count (H_ERROR)

The H_ERROR bits control the reference detector's error threshold, which determines the maximum number of missing H sync pulses before indicating a LOR. See section *6.1.1 Programming the Loss of Reference (LOR) Threshold*.

Bit 3: Holdover on Loss of Reference (HOLDOVER)

The HOLDOVER bit controls the operating mode when a loss of reference occurs. See section *3.2.2 Loss of Reference (LOR)*.

Bit 4: Reference Select (RSEL)

The RSEL bit selects either REF_A or REF_B inputs as the reference to genlock the outputs when I²C_RSEL = 1.

RSEL = 0: Select REF_A inputs.

RSEL = 1: Select REF_B inputs.

If PIN6_OVRD = 1 (register 02h), then reference selection must be controlled by programming RSEL, regardless of I²C_RSEL. When PIN6_OVRD = 0 and I²C_RSEL = 0, then reference selection is controlled using the REF_SEL input pin and the RSEL bit is ignored.

Bit 5: Reference Select Control via I²C (I²C_RSEL)

By programming I²C_RSEL, reference selection can be controlled either via I²C or the REF_SEL input pin.

I_2C_RSEL = 1: Control reference selection by programming RSEL.

I²C_RSEL = 0: Control reference selection via the REF_SEL input pin.

Note: If PIN6_OVRD = 1, then reference selection must be controlled by programming RSEL regardless of I²C_RSEL.

Bit 6: Mode Select (GNLK)

The GNLK bit selects the operating mode when I²C_GNLK = 1. See section *3.0 MODES OF OPERATION*.

GNLK = 0: Selects Free Run mode.

GNLK = 1: Selects Genlock mode.

If I²C_GNLK = 0, then the operating mode will be controlled using the $\overline{\text{GENLOCK}}$ input pin and the GNLK bit will be ignored.

Bit 7: Mode Select via I²C (I²C_GNLK)

By programming I²C_GNLK, mode selection can be controlled either via I²C or the $\overline{\text{GENLOCK}}$ input pin.

I²C_GNLK = 1: Control mode selection by programming GNLK.

I²C_GNLK = 0: Control mode selection via the $\overline{\text{GENLOCK}}$ input pin.

9.2 Genlock Status And Lock Control Register

REGISTER 01h

Bit 0: Reference Status (REF_VALID)

REF_VALID is a read-only bit and indicates the presence or loss of reference on the selected reference port in Genlock mode. The NO_REF output flag is an inverted copy of REF_VALID. See section *6.1 Reference Detection*.

REF_VALID = 0: Indicates loss of reference (LOR).

REF_VALID = 1: Indicates valid reference.

In Free Run mode, REF_VALID will be set to 0 to indicate the absence of any input pulses at the selected HREF port.

Bit 1: SD Clock PLL Lock Status (SD_LOCK)

SD_LOCK is a read-only bit and indicates PLL lock status of the selected SD clock. See section *6.2 PLL Lock Detection*.

SD_LOCK = 0: Indicates loss of lock.

SD_LOCK = 1: Indicates valid lock.

Bit 2: HD Clock PLL Lock Status (HD_LOCK)

HD_LOCK is a read-only bit and indicates PLL lock status of the selected HD clock. See section *6.2 PLL Lock Detection*.

HD_LOCK = 0: Indicates loss of lock.

HD_LOCK = 1: Indicates valid lock.

Bits 7-3: Lock Control (LOCK_CTRL)

LOCK_CTRL controls the phase error threshold of the VCXO PLL lock detector. A larger value for LOCK_CTRL will yield shorter lock indication time (although not actual lock time) at the expense of higher output phase error when lock is initially indicated, whereas a smaller value will yield the opposite effect. See section *6.2.1 Programming the PLL Lock Threshold*.

9.3 Input Control Register

REGISTER 02h

Bit 0: VREF_B Input Signal Polarity (POL_VB)

This bit should be programmed to match the input signal polarity at the VREF_B input pin.

POL_VB = 0: Negative polarity or active low signal.

POL_VB = 1: Positive polarity or active high signal.

Bit 1: HREF_B Input Signal Polarity (POL_HB)

This bit should be programmed to match the input signal polarity at the HREF_B input pin. The rising edge of the output clock will be phase locked to the active edge of the H sync input signal.

POL_HB = 0: Negative polarity or active low signal.

POL_HB = 1: Positive polarity or active high signal.

Bit 2: VREF_A Input Signal Polarity (POL_VA)

This bit should be programmed to match the input signal polarity at the VREF_A input pin.

POL_VA = 0: Negative polarity or active low signal.

POL_VA = 1: Positive polarity or active high signal.

Bit 3: HREF_A Input Signal Polarity (POL_HA)

This bit should be programmed to match with the input signal polarity at HREF_A input pin. The rising edge of the output clock will be phase locked to the active edge of the H sync input signal.

POL_HA = 0: Negative polarity or active low signal.

POL_HA = 1: Positive polarity or active high signal.

Bit 4: 27 MHz Reference Control (27M_REF)

Instead of an H sync signal, a 27 MHz clock signal can be applied to the selected HREF input to phase lock the output clocks. If a 27 MHz clock is used as a reference, then a value of 1 should be programmed to 27M_REF, REF_DIV, and FB_DIV.

27M_REF = 0: H sync input signal.

27M_REF = 1: 27 MHz clock input signal.

Note: The VCXO PLL loop parameters are different between an H sync signal and a 27 MHz clock signal; therefore, they

will require different external loop filter components for optimal PLL response.

Bit 5: Pin 6 Override (PIN6_OVRD)

The PIN6_OVRD bit can be programmed to override the default reference selection capability on pin 6 and instead use pin 6 as an logic pulse input for output alignment initialization, which initializes or resets the frame counter programmed to TOF_RST.

PIN6_OVRD = 0: Allows a logic level input to be applied to pin 6 for reference selection if RSEL_I²C = 0 (register 00h). If RSEL_I²C = 1, then pin 6 is ignored and reference selection is controlled via I²C; additionally, output alignment must be initialized via I²C by programming TOF_INIT and EN_TOF_RST (register 0Ah).

PIN6_OVRD = 1: Allows an TOF Init pulse to be applied to pin 6 for output alignment initialization if EN_TOF_RST = 1. If EN_TOF_RST = 0, then any TOF Init pulse received at pin 6 will be ignored. Additionally, reference selection must be controlled via I²C, regardless of I²C_RSEL.

Bits 7-6: Reserved (RSV)

9.4 PLL 1 Divider Register

REGISTER 03h

Bits 1-0: Reference Divider Value (REF_DIV)

REF_DIV selects the reference divider value according to *Table 3*. See section *4.1 Programming The VCXO PLL Dividers*.

The reference divide value is the denominator of the VCXO PLL divider ratio:

Feedback divider value / Reference divider value = 27 MHz / Hsync input frequency

The numerator and denominator values of the divider ratio must be reduced to their lowest factors before programming REF_DIV and FB_DIV. These registers must be programmed correctly for the input timing format in order to phase lock the 27 MHz VCXO PLL and output clocks to the HREF input.

Bits 7-3: Reserved (RSV)

REGISTER 04h

Bits 7-0: Feedback Divide Value (FB_DIV)

This register contains the 8 LSBs of FB_DIV. The feedback divider value is the numerator of the VCXO PLL divider ratio. FB_DIV should be programmed using the exact feedback divider value after the divide ratio has been reduced to its lowest factors. See the description for REF_DIV.

REGISTER 05h

Bits 4-0: Feedback Divide Value (FB_DIV)

This register contains the 5 MSBs of FB_DIV. See the description for register 04h.

Bits 7-5: These non-programmable bits contain zeros.

9.5 PLL 4 Charge Pump Current Control Registers

REGISTER 06h

Bits 3-0: Charge Pump Current Control for PLL 4 (ICP4)

ICP4 can be programmed to specify the charge pump current for PLL 4, which generates the 67.5 MHz SD clock.

Note: Bit 3 is inverted internally, so the default value of 0000b (0h) actually yields an effective value of 1000b (8h).

Reducing the effective value of the charge pump current will lower its loop bandwidth at the expense of reduced PLL stability. An effective value of 0 should not be programmed since this corresponds to 0 µA nominal current and will cause PLL 4 to lose phase lock.

Bits 7-4: Reserved (RSV)

REGISTER 07h

Bits 7-0: Reserved (RSV)

9.6 Output Clock And TOF Control Register

REGISTER 08h

Bit 0: SD Clock Output Frequency Select (SD_FREQ)

This bit sets the clock frequency of the SD_CLK output pair. See section *5.1 Programming The Output Clock Frequencies*.

SD_FREQ = 0: Selects 27 MHz from PLL 1.

SD_FREQ = 1: Selects 67.5 MHz from PLL 4.

Bit 1: SD Clock Output Mode (SD_HIZ)

Set the SD_HIZ bit to 1 to put the SD_CLK output pair in high-impedance (Hi-Z) mode; otherwise, the SD_CLK output will be enabled.

Bit 3-2: HD Clock Output Frequency Select (HD_FREQ)

These bits set the clock frequency of the HD_CLK output pair.

HD_FREQ = 00b: Selects 74.25 MHz from PLL 2.

HD_FREQ = 01b: Selects 74.176 MHz from PLL 3.

HD_FREQ = 10b: Selects 148.5 MHz from PLL 2.

HD_FREQ = 11b: Selects 148.35 MHz from PLL 3.

Bit 4: HD Clock Output Mode (HD_HIZ)

Set the HD_HIZ bit to 1 to put the HD_CLK output pair in high-impedance (Hi-Z) mode; otherwise, the HD_CLK output will be enabled.

Bit 5: Top of Frame Output Mode (TOF_HIZ)

Set the TOF_HIZ bit to 1 to put the TOF output pin in high-impedance (Hi-Z) mode; otherwise, the output will be enabled.

Bits 7-6: Reserved (RSV)

9.7 TOF Configuration Registers

REGISTER 09h

Bits 7-0: TOF Reset (TOF_RST)

This register contains the 8 LSBs of TOF_RST. When the VCXO PLL is phase locked to the reference, both H sync and V sync inputs are used to reset the frame-based counters used for output TOF generation. The numerator value of the reduced frame rate ratio should be programmed to TOF_RST. See section *5.2.4 Input-Output Frame Rate Ratio*.

For example, if the input timing is NTSC and the desired output timing is PAL, then a value of 1200 (decimal) should be programmed to TOF_RST (30/1.001 Hz / 25 Hz = **1200** / 1001).

Once TOF_RST is programmed, it must be properly initialized by either programming TOF_INIT or otherwise using an external TOF Init pulse (when PIN6_OVRD = 1).

REGISTER 0Ah

Bits 4-0: TOF Reset (TOF_RST)

This register contains the 5 MSBs of TOF_RST. See the description for register 09h.

Bit 5: Output Alignment Initialization (TOF_INIT)

After enabling output alignment mode (EN_TOF_RST = 1), the TOF_INIT bit should be programmed to initially align the outputs to the desired input reference frame. The initialization is triggered by programming a positive bit transition (0 to 1) to TOF_INIT, which will reset the frame counters programmed to TOF_RST. See section *5.3 Programming The Output Alignment Sequence*.

Bit 6: TOF Pulse Output Polarity (POL_TOF)

This bit should be programmed to the desired TOF pulse polarity at the TOF output.

POL_TOF = 0: Negative polarity or active low signal.

POL_TOF = 1: Positive polarity or active high signal.

Bit 7: Output Alignment Mode (EN_TOF_RST)

This bit must be set (EN_TOF_RST = 1) to enable output alignment mode prior to initialization per section *5.3 Programming The Output Alignment Sequence*. It is recommended to clear this bit (EN_TOF_RST = 0) immediately after the output alignment sequence has been programmed to prevent excessive output jitter, as described in section *2.3 Output Disturbance While Alignment Mode Enabled*.

REGISTER 0Bh

Bits 7-0: Total Pixels per Line for the Output Format (TOF_PPL)

This register contains the 8 LSBs of TOF_PPL. TOF_PPL should be programmed with total pixels per line for the desired output format. TOF_PPL is used in specifying the output frame rate. This should be specified prior to programming the output alignment sequence. See section *5.2.2 Output Frame Rate*.

REGISTER 0Ch

Bits 4-0: MSBs of Total Pixels per Line for the Output Format (TOF_PPL)

This register contains the 5 MSBs of TOF_PPL. See the description for register 0Bh.

Bit 5: Reference Clock Select for Output Top of Frame (TOF_CLK)

This bit should be programmed to select the output clock reference according to the desired output format. The selected clock frequency is used in specifying the output frame rate. See sections *5.2.1 Output Clock Reference* and *5.2.2 Output Frame Rate*.

TOF_CLK = 0: Selects the SD_CLK output as the output clock reference.

TOF_CLK = 1: Selects the HD_CLK output as the output clock reference.

Bit 7-6: These non-programmable bits contain zeros.

REGISTER 0Dh

Bits 7-0: LSBs of Total Lines per Frame for the Output Format (TOF_LPFM)

This register contains the 8 LSBs of TOF_LPFM. TOF_LPFM should be programmed with the total lines per frame for the desired output format. TOF_LPFM is used in specifying the output frame rate. This should be specified prior to programming the output alignment sequence. See section *5.2.2 Output Frame Rate*.

REGISTER 0Eh

Bits 3-0: MSBs of Total Lines per Frame for the Output Format (TOF_LPFM)

This register contains the 4 MSBs of TOF_LPFM. See the description for register 0Dh.

Bit 7-5: These non-programmable bits contain zeros.

REGISTER 0Fh

Bits 7-0: LSBs of Total Lines per Frame for the Input Reference Format (REF_LPFM)

This register contains the 8 LSBs of REF_LPFM. REF_LPFM should be programmed with the total lines per frame for the input reference format. REF_LPFM is used in specifying the reference frame rate. This should be specified prior to programming the output alignment sequence (section *5.2.3 Reference Frame Rate*).

REGISTER 10h

Bits 3-0: MSBs of Total Lines per Frame for the Input Reference Format (REF_LPFM)

This register contains the 4 MSBs of REF_LPFM. See the description for register 0Fh.

Bit 7-4: These non-programmable bits contain zeros.

REGISTER 11h

Bits 7-0: LSBs of Output Frame Offset (TOF_OFFSET)

This register contains the 8 LSBs of TOF_OFFSET. TOF_OFFSET should be programmed with the desired line offset to delay or advance the output timing relative to the reference frame. This should be specified prior to programming the output alignment sequence. See section *5.2.5 Output Frame Line Offset*.

REGISTER 12h

Bits 3-0: MSBs of Line Offset for the Output Top of Frame (TOF_OFFSET)

This register contains the 4 MSBs of TOF_OFFSET. See the description for register 11h.

Bit 7-4: These bits contain zeros (non-programmable)

9.8 PLL 1 Charge Pump Current Control Register

REGISTER 13h

Bits 4-0: Charge Pump Current Control for PLL 1 (ICP1)

ICP1 can be programmed to specify the charge pump current for PLL 1. ICP1 is one of the loop gain parameters can be programmed to optimize the VCXO PLL loop response.

For example, ICP1 can be adjusted in proportion to a change in FB_DIV to maintain a constant loop gain and a thus consistent loop response across different input formats for the same loop filter circuit. Also, when phase lock has been achieved, lowering ICP1 can reduce the PLL1 charge pump current to lower the loop bandwidth for additional input jitter rejection; this can be helpful to minimize low-frequency input jitter from propagating to the output clocks.

Note: ICP1 values of 0 to 2 correspond to PLL 1 charge pump currents of less than about 60 µA. These low currents may cause reduced PLL performance (e.g. loss of lock, clock wander) due to loop filter charge leakage and other secondary factors. Therefore, it is not recommended to use ICP1 less than 3.

ICP1 = 0: 0 µA (not recommended)

ICP1 = 8: 250 µA nominal (default)

ICP1 = 31: 1000 µA nominal

ICP1 step: 31.25 µA nominal current step

Bits 7-5: Reserved (RSV)

9.9 PLL 2 and PLL 3 Charge Pump Current Control Register

REGISTER 14h

Bits 3-0: Charge Pump Current Control for PLL 3 (ICP3)

ICP3 can be programmed to specify the charge pump current for PLL 3, which generates the 74.176 and 148.35 MHz HD clock outputs. Reducing the value of ICP3 will reduce the PLL 3 charge pump current and lower its loop bandwidth at the expense of reduced PLL stability. An value of 0 should not be programmed since this corresponds to 0 µA nominal current and will cause PLL 3 to lose phase lock.

Bit 7-4: Charge Pump Current Control for PLL 2 (ICP2)

ICP2 can be programmed to specify the charge pump current for PLL 2, which generates the 74.25 and 148.5 MHz HD clock outputs. Reducing the value of ICP2 will reduce the PLL 2 charge pump current and lower its loop bandwidth at the expense of reduced PLL stability. An value of 0 should not be programmed since this corresponds to 0 µA nominal current and will cause PLL 2 to lose phase lock.

9.10 Reserved Registers

REGISTER 07h

REGISTER 15h-1Fh

Do not program any data to these registers.

10.0 TYPICAL SYSTEM BLOCK DIAGRAMS

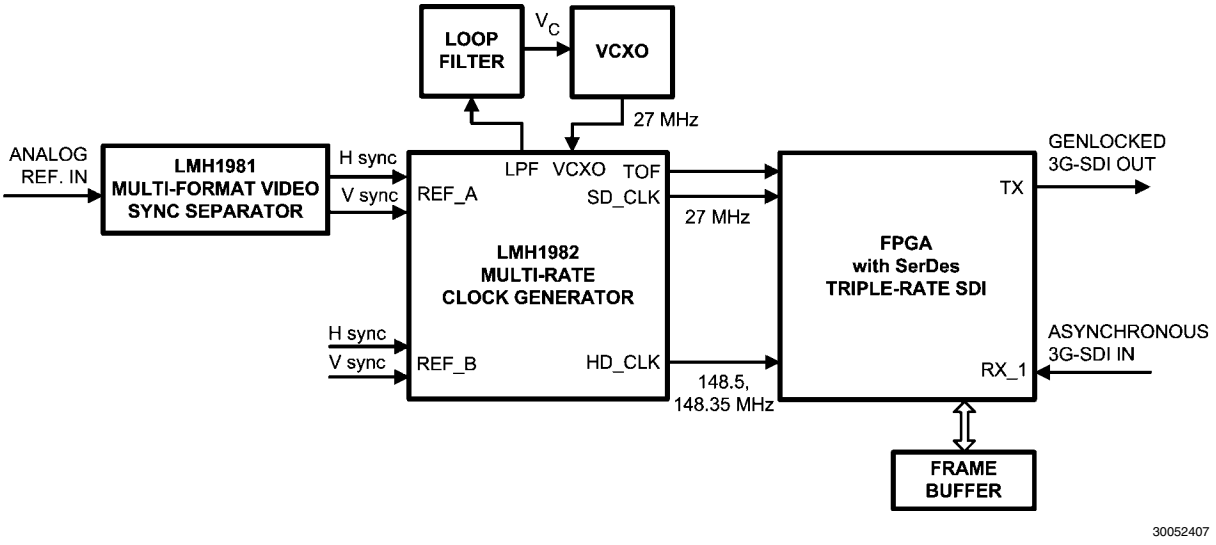


FIGURE 9. Analog Reference Genlock for Triple-rate SDI Video

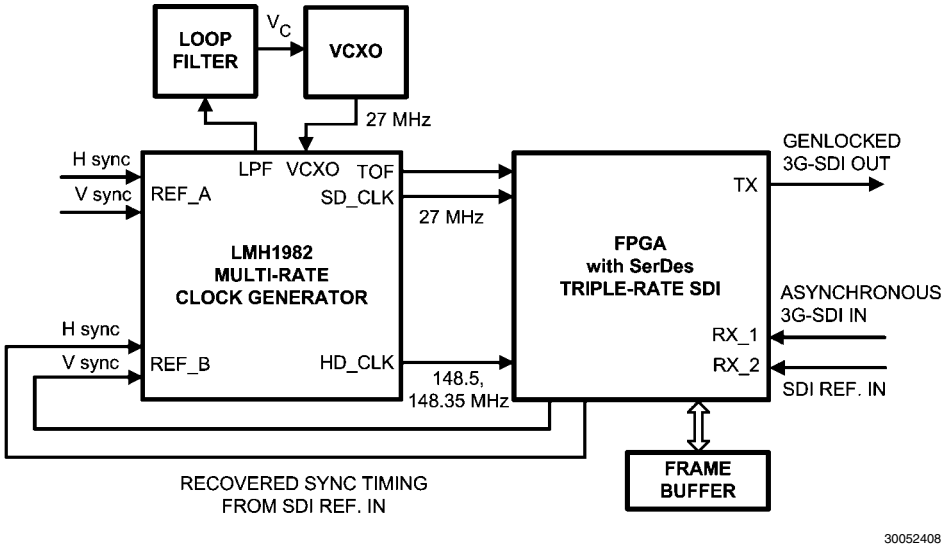


FIGURE 10. SDI Reference Genlock for Triple-rate SDI Video

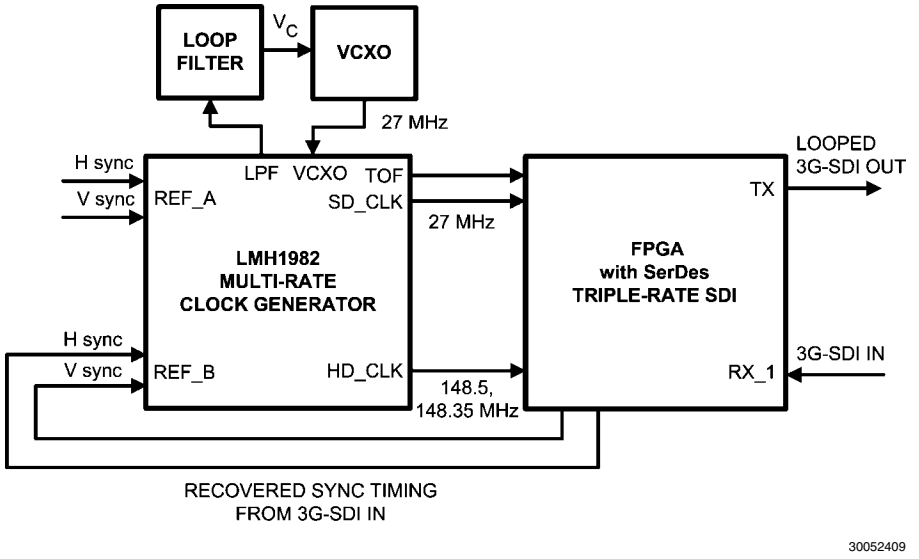


FIGURE 11. Triple-rate SDI Loop-through

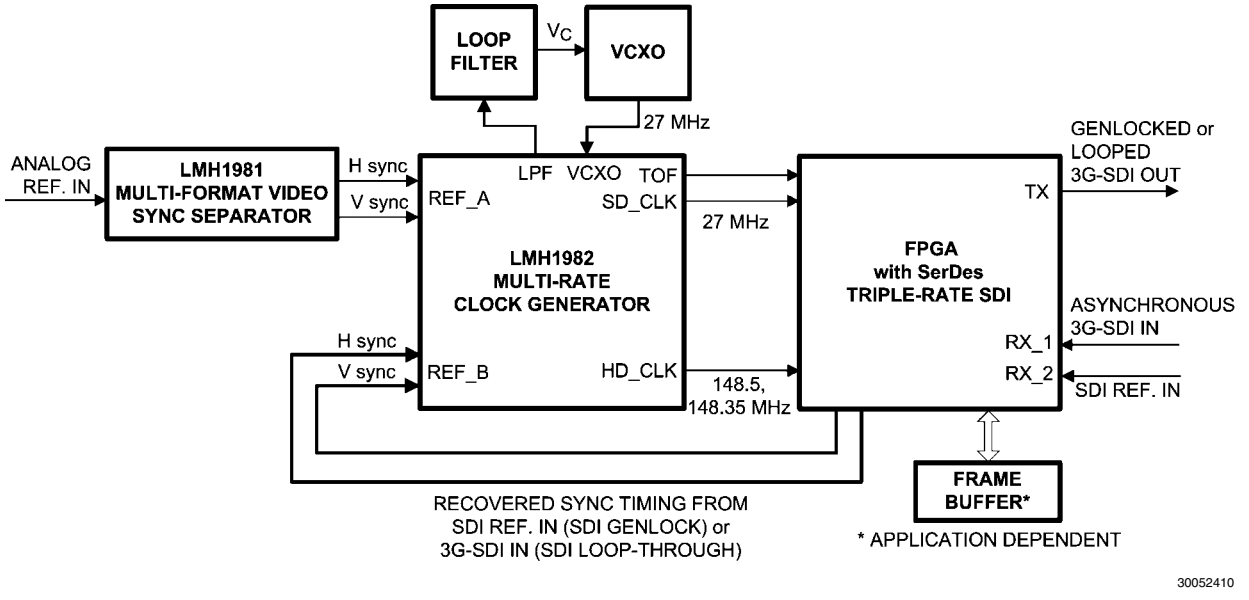
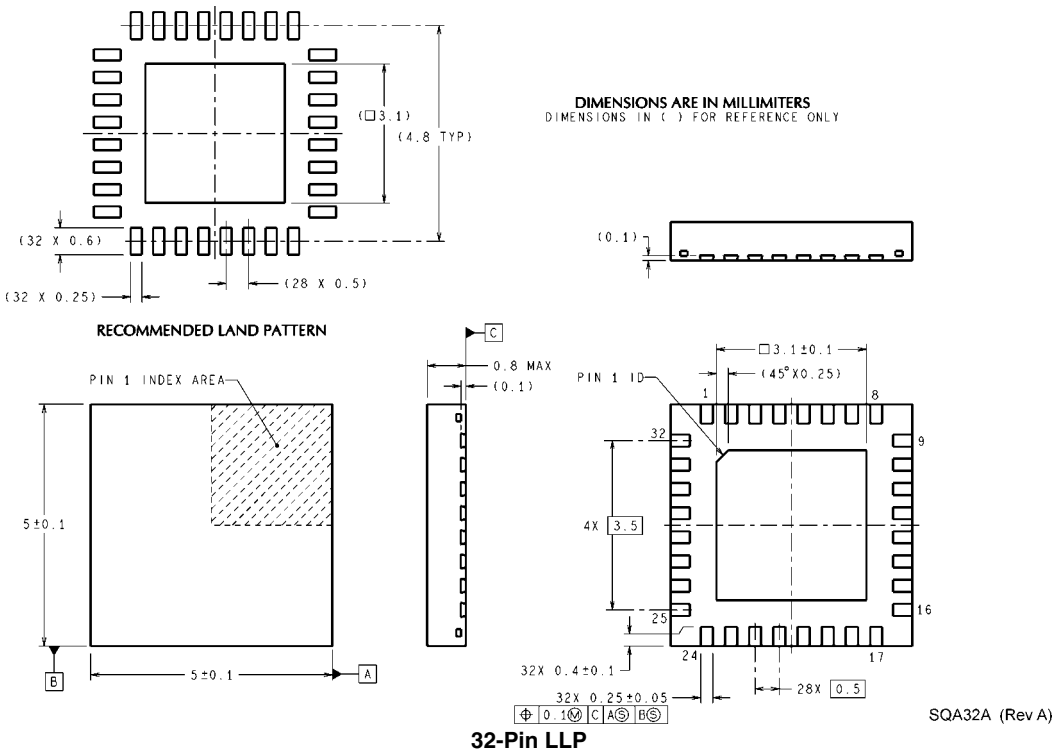


FIGURE 12. Combined Genlock or Loop-through for Triple-rate SDI Video

Physical Dimensions inches (millimeters) unless otherwise noted



32-Pin LLP
NS Package Number SQA32A

Notes

Notes

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Ethernet	www.national.com/ethernet	Packaging	www.national.com/packaging
Interface	www.national.com/interface	Quality and Reliability	www.national.com/quality
LVDS	www.national.com/lvds	Reference Designs	www.national.com/refdesigns
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PowerWise	www.national.com/powerwise		
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