



SPP2303

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP2303 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

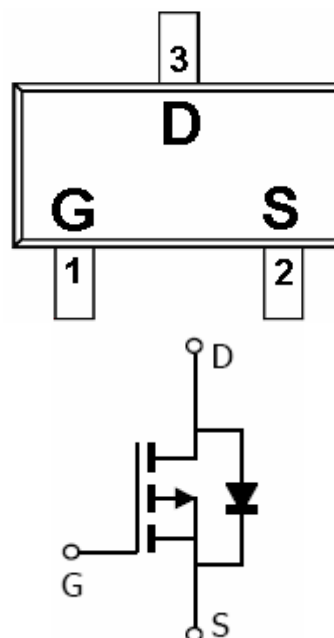
FEATURES

- ◆ $-30V/-2.6A, R_{DS(ON)}=130m\Omega @ V_{GS}=-10V$
- ◆ $-30V/-2.0A, R_{DS(ON)}=180m\Omega @ V_{GS}=-4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-23-3L package design

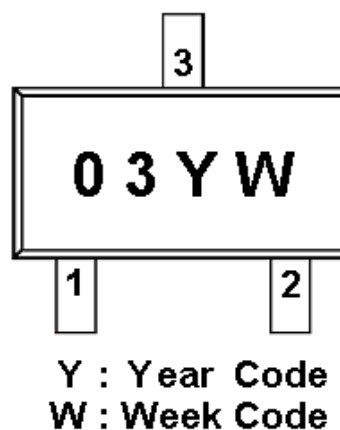
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(SOT-23-3L)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP2303S23RG	SOT-23-3L	03YW

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)

※ SPP2303S23RG : Tape Reel ; Pb – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	-30	V
Gate –Source Voltage		V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	T _A =25°C	I _D	-3.0	A
	T _A =70°C		-2.0	
Pulsed Drain Current		I _{DM}	-10	A
Continuous Source Current(Diode Conduction)		I _S	-1.25	A
Power Dissipation	T _A =25°C	P _D	1.25	W
	T _A =70°C		0.8	
Operating Junction Temperature		T _J	150	°C
Storage Temperature Range		T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient		R _{θJA}	100	°C/W



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ELECTRICAL CHARACTERISTICS

(T_A=25°C Unless otherwise noted)

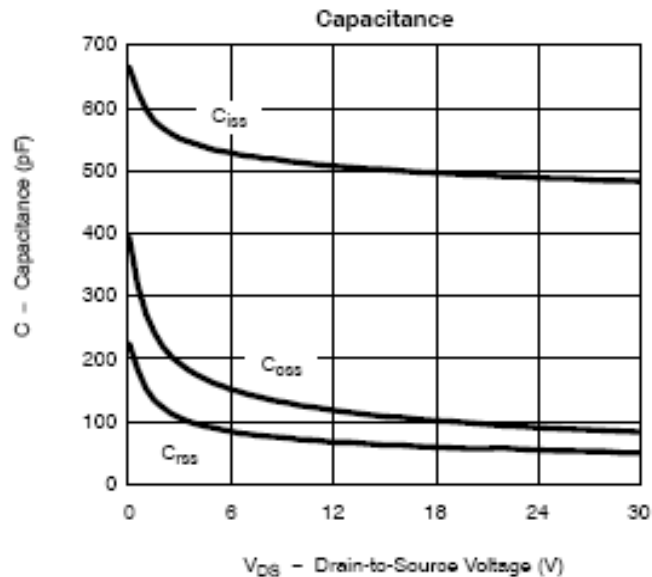
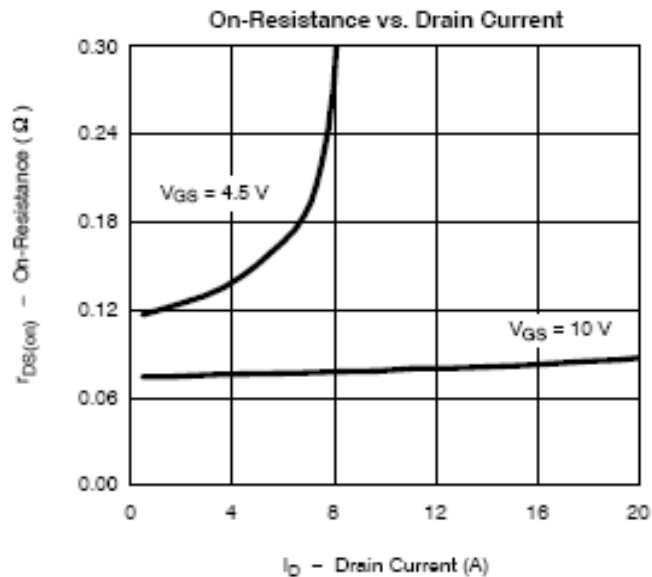
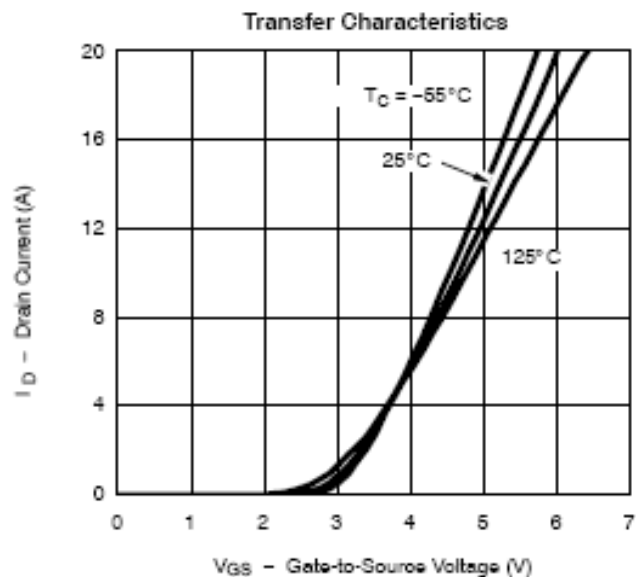
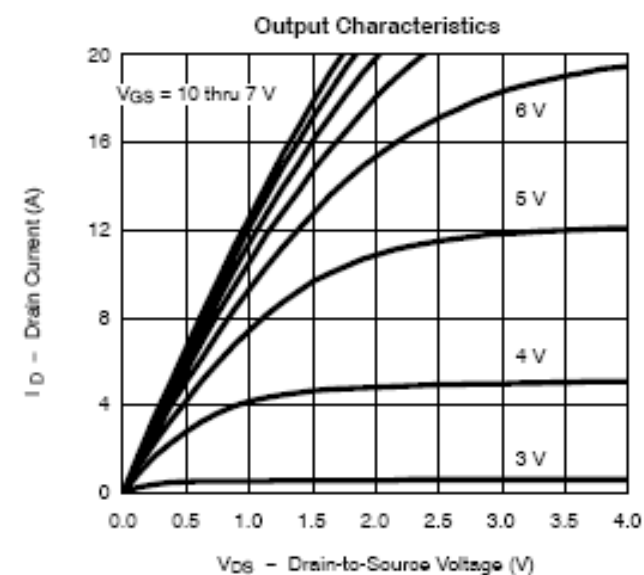
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =-10uA	-30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-1.0		-3.0	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-30V, V _{GS} =0V			-1	uA
		V _{DS} =-30V, V _{GS} =0V T _J =55°C			-10	
On-State Drain Current	I _{D(on)}	V _{DS} ≤ -5V, V _{GS} =-10V	-6			A
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-2.6A		0.095	0.130	Ω
		V _{GS} =-4.5V, I _D =-2.0A		0.125	0.180	
Forward Transconductance	g _{fs}	V _{DS} =-10V, I _D =-1.7A		2.4		S
Diode Forward Voltage	V _{SD}	I _S =-1.25A, V _{GS} =0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =-15V, V _{GS} =-10V I _D =-1.7A		5.8	10	nC
Gate-Source Charge	Q _{gs}			0.8		
Gate-Drain Charge	Q _{gd}			1.5		
Input Capacitance	C _{iss}	V _{DS} =-15V, V _{GS} =0V f=1MHz		226		pF
Output Capacitance	C _{oss}			87		
Reverse Transfer Capacitance	C _{rss}			19		
Turn-On Time	t _{d(on)}	V _{DD} =-15V, R _L =15Ω I _D =-1.0A, V _{GEN} =-10V R _G =6Ω		9	20	ns
	t _r			9	20	
Turn-Off Time	t _{d(off)}			18	35	
	t _f			6	20	



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TYPICAL CHARACTERISTICS

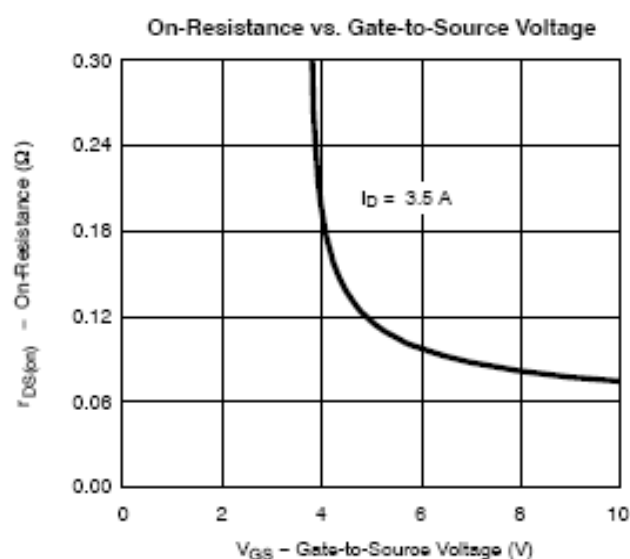
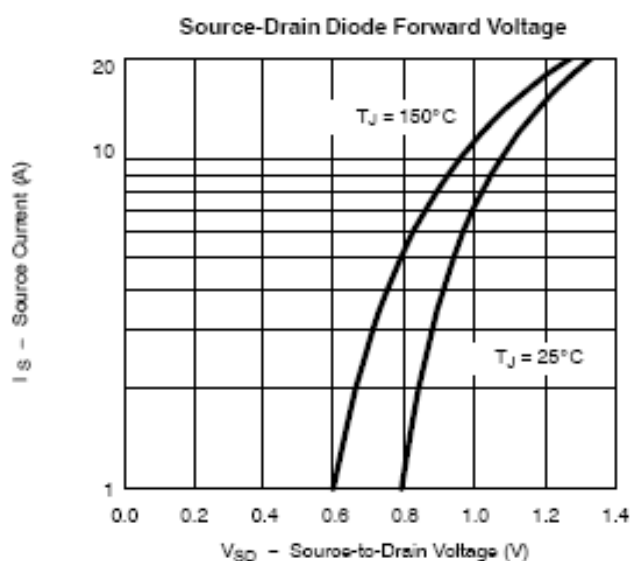
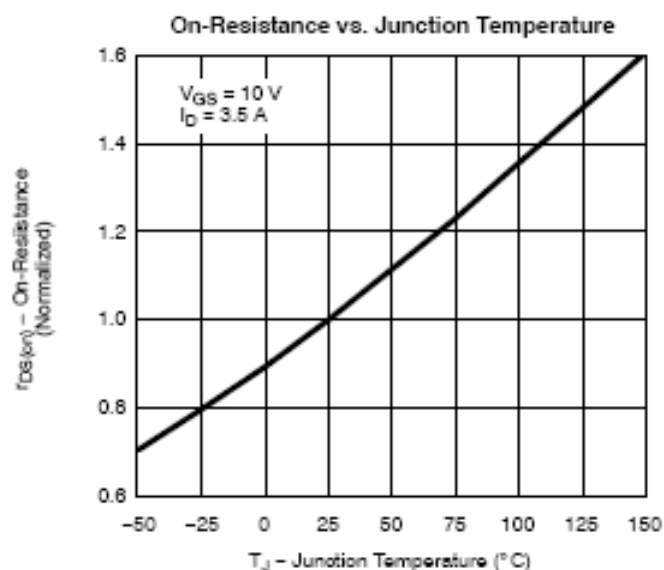
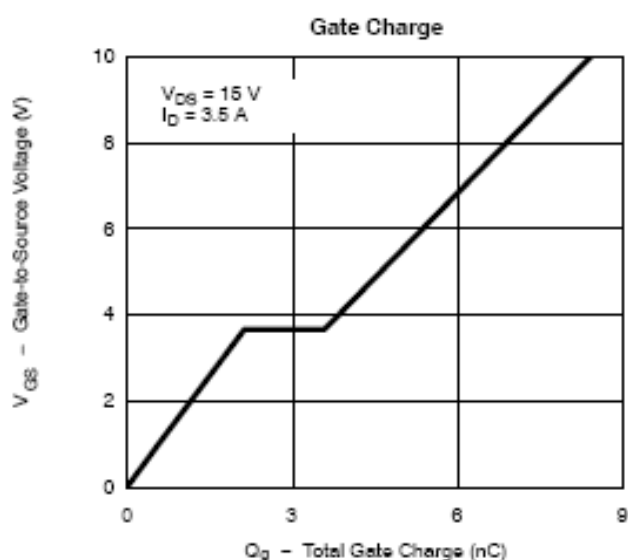




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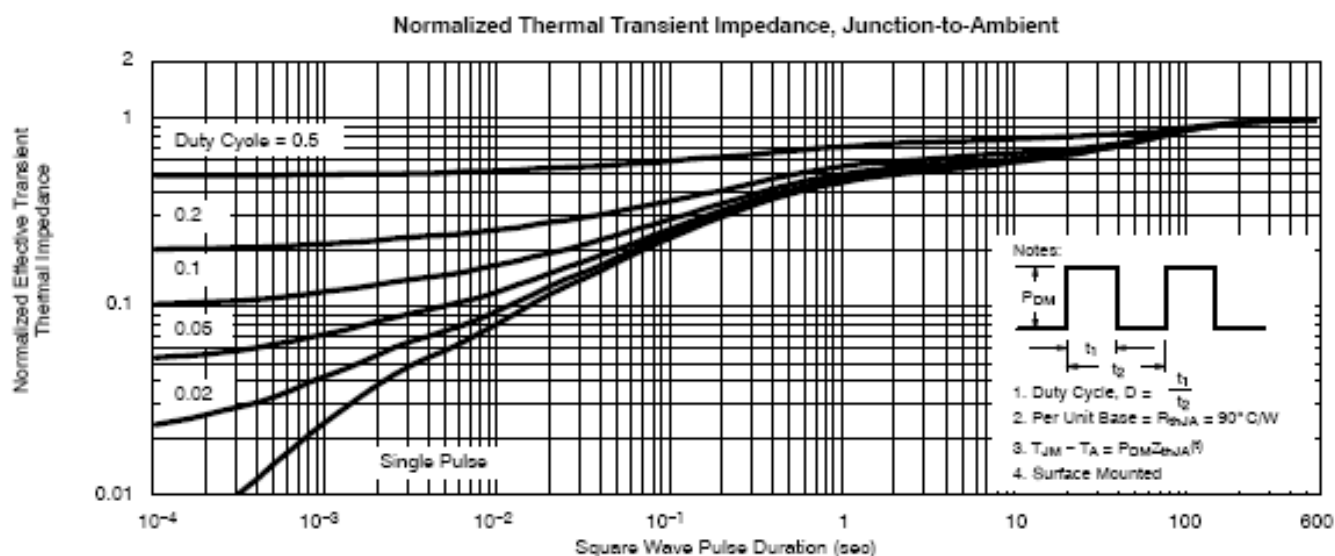
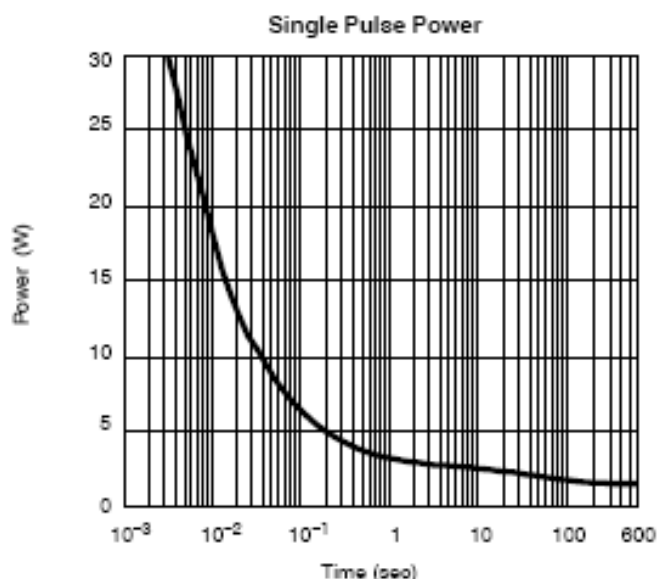
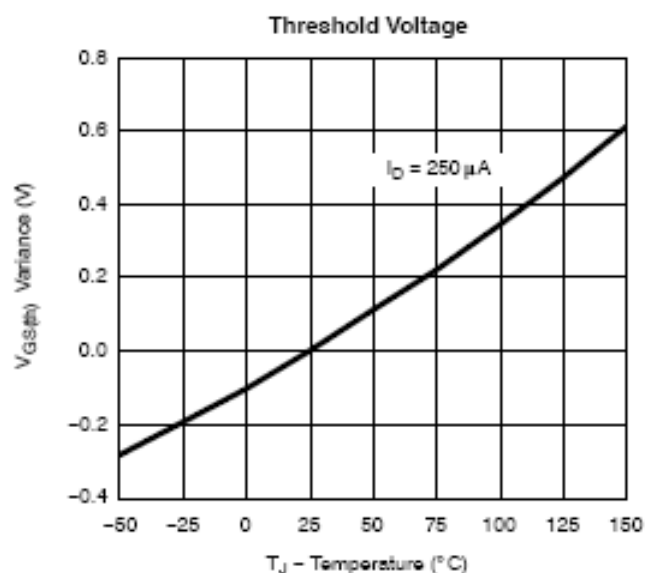




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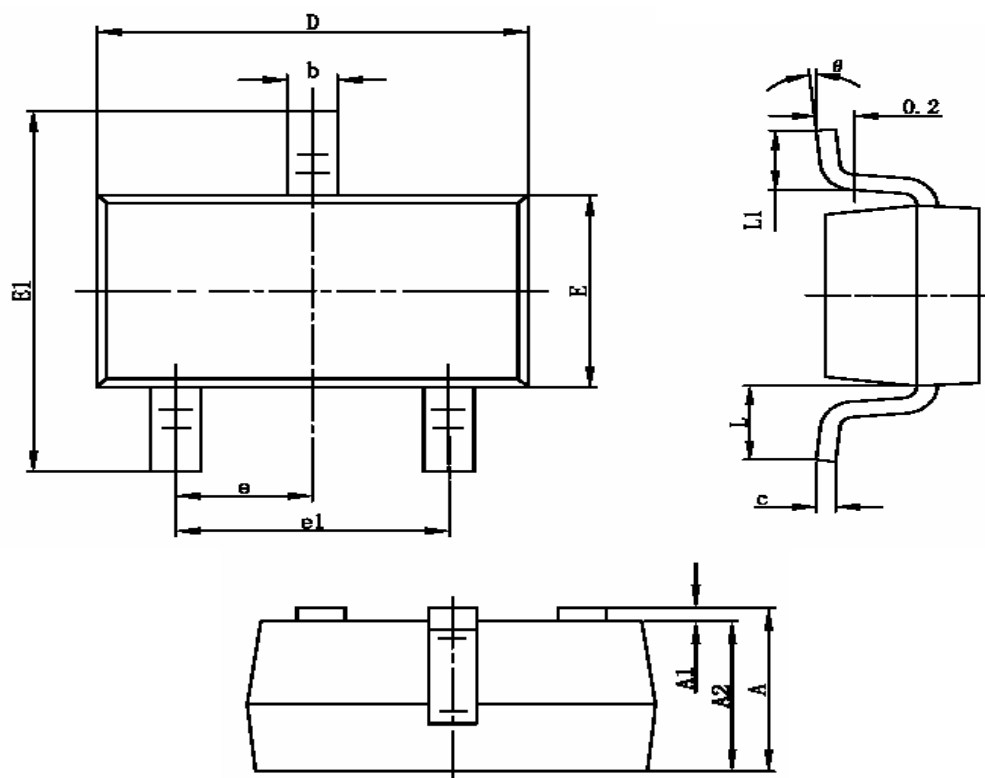




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SOT-23-3L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°



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SYNC Power Corporation

9F-5, No.3-2, Park Street

NanKang District (NKSP), Taipei, Taiwan, 115, R.O.C

Phone: 886-2-2655-8178

Fax: 886-2-2655-8468

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