

Linear Systems Monolithic Dual PNP Transistor

The LS352 is a monolithic pair of PNP transistors mounted in a single P-DIP package. The monolithic dual chip design reduces parasitics and gives better performance while ensuring extremely tight matching.

The 8 Pin P-DIP provides ease of manufacturing, and the symmetrical pinout prevents improper orientation.

(See Packaging Information).

LS352 Features:

- Very high gain
- Tight matching
- Low Output Capacitance

FEATURES

HIGH GAIN	$h_{FE} \geq 200$ @ 10 μ A-1mA
TIGHT V_{BE} MATCHING	$ V_{BE1} - V_{BE2} = 0.2\text{mV TYP.}$
HIGH f_t	275MHz TYP. @ 1mA

ABSOLUTE MAXIMUM RATINGS¹ @ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	-65°C to +200°C
Operating Junction Temperature	-55°C to +150°C

Maximum Power Dissipation

Continuous Power Dissipation (One side)	250mW
Continuous Power Dissipation (Both sides)	500mW
Linear Derating factor (One side)	2.3mW/°C
Linear Derating factor (Both sides)	4.3mW/°C

Maximum Currents

Collector Current	10mA
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MATCHING CHARACTERISTICS @ 25°C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$ V_{BE1} - V_{BE2} $	Base Emitter Voltage Differential	--	0.2	0.5	mV	$I_C = 10\mu\text{A}, V_{CE} = 5\text{V}$
$\Delta V_{BE1} - V_{BE2} / \Delta T$	Base Emitter Voltage Differential Change with Temperature	--	0.5	2	$\mu\text{V}/^\circ\text{C}$	$I_C = 10\mu\text{A}, V_{CE} = 5\text{V}$ $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$
$ I_{B1} - I_{B2} $	Base Current Differential	--	--	5	nA	$I_C = 10\mu\text{A}, V_{CE} = 5\text{V}$
$ \Delta (I_{B1} - I_{B2}) / ^\circ\text{C}$	Base Current Differential Change with Temperature	--	--	0.3	$\text{nA}/^\circ\text{C}$	$I_C = 10\mu\text{A}, V_{CE} = 5\text{V}$ $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$
h_{FE1} / h_{FE2}	DC Current Gain Differential	--	5	--	%	$I_C = 10\mu\text{A}, V_{CE} = 5\text{V}$

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{CBO}	Collector to Base Voltage	60	--	--	V	$I_C = 10\mu\text{A}, I_E = 0$
BV_{CEO}	Collector to Emitter Voltage	60	--	--	V	$I_C = 10\mu\text{A}, I_B = 0$
BV_{EBO}	Emitter-Base Breakdown Voltage	6.2	--	--	V	$I_E = 10\mu\text{A}, I_C = 0^2$
BV_{CCO}	Collector to Collector Voltage	100	--	--	V	$I_C = 10\mu\text{A}, I_E = 0$
h_{FE}	DC Current Gain	200	--	600		$I_C = 10\mu\text{A}, V_{CE} = 5\text{V}$
		200	--	600		$I_C = 100\mu\text{A}, V_{CE} = 5\text{V}$
		200	--	--		$I_C = 1\text{mA}, V_{CE} = 5\text{V}$
$V_{CE(SAT)}$	Collector Saturation Voltage	--	--	0.5	V	$I_C = 1\text{mA}, I_B = 0.1\text{mA}$
I_{EBO}	Emitter Cutoff Current	--	--	0.2	nA	$I_E = 0, V_{CB} = 3\text{V}$
I_{CBO}	Collector Cutoff Current	--	--	0.2	nA	$I_E = 0, V_{CB} = 20\text{V}$
C_{OBO}	Output Capacitance	--	--	2	pF	$I_E = 0, V_{CB} = 5\text{V}$
C_{C1C2}	Collector to Collector Capacitance	--	--	2	pF	$V_{CC} = 0\text{V}$
I_{C1C2}	Collector to Collector Leakage Current	--	--	0.5	nA	$V_{CC} = \pm 45\text{V}$
f_T	Current Gain Bandwidth Product	200	--	--	MHz	$I_C = 1\text{mA}, V_{CE} = 5\text{V}$
NF	Narrow Band Noise Figure	--	--	3	dB	$I_C = 100\mu\text{A}, V_{CE} = 5\text{V}, BW = 200\text{Hz}, R_G = 10\text{K}\Omega, f = 1\text{KHz}$

Notes:

- Absolute Maximum ratings are limiting values above which serviceability may be impaired
- The reverse base-to-emitter voltage must never exceed 6.2 volts; the reverse base-to-emitter current must never exceed 10 μ A.



Available Packages:

LS352 in P-DIP
LS352 available as bare die

Please contact Micross for full package and die dimensions:

Email: chipcomponents@micross.com
Web: www.micross.com/distribution.aspx

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P-DIP (Top View)

