numonyx

M39P0R9080E0

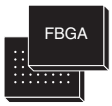
512 Mbit (x16, Multiple Bank, Multi-Level, Burst) Flash Memory 256 Mbit Low Power SDRAM, 1.8V Supply, Multi-Chip Package

Feature summary

- Multi-Chip Package
  - 1 die of 512 Mbit (32Mb x 16, Multiple Bank, Multi-Level, Burst) Flash memory
  - 1 die of 256 Mbit (4 Banks of 4Mb x16) Low Power Synchronous Dynamic RAM
- Supply voltage
  - $V_{DDF} = V_{CCP} = V_{DDQ} = 1.7$ to 1.95V
  - $V_{PPF} = 9V$ for fast program
- Electronic signature
  - Manufacturer Code: 20h
  - Device Code: 8819
- ECOPACK® package available

Flash memory

- Synchronous / asynchronous read
  - Synchronous Burst Read mode: 108MHz, 66MHz
  - Asynchronous Page Read mode
  - Random Access: 96ns
- Programming time
  - 4.2µs typical Word program time using Buffer Enhanced Factory Program command
- Memory organization
  - Multiple Bank Memory Array: 64 Mbit Banks
  - Four Extended Flash Array (EFA) Blocks of 64 Kbits
- Dual operations
  - program/erase in one Bank while read in others
  - No delay between read and write operations
- Security
  - 64-bit unique device number
  - 2112-bit user programmable OTP Cells



TFBGA105 (ZAD)
9 x 11mm

- 100,000 program/erase cycles per block
- Block locking
  - All Blocks locked at power-up
  - Any combination of Blocks can be locked with zero latency
  - $\overline{WP}_F$ for Block Lock-Down
  - Absolute Write Protection with $V_{PPF} = V_{SS}$
- Common Flash Interface (CFI)

LPSDRAM

- 256 Mbit synchronous dynamic RAM
  - Organized as 4 Banks of 4 MWords, each 16 bits wide
- Synchronous burst read and write
  - Fixed Burst Lengths: 1, 2, 4, 8 words or Full Page
  - Burst Types: Sequential and Interleaved.
  - Clock Frequency: 133 MHz (7.5ns speed class)
  - Clock Valid to Output Delay ($\overline{CAS}$ Latency): 3 at 133 MHz
- Automatic and controlled precharge
- Low-power features:
  - Partial Array Self Refresh (PASR),
  - Automatic Temperature Compensated Self Refresh (TCSR)
  - Driver Strength (DS)
  - Deep Power-Down Mode
- Auto Refresh and Self Refresh

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1 Summary description

The M39P0R9080E0 combines two memory devices in one Multi-Chip Package:

- 512-Mbit Multiple Bank Flash memory (the M58PR512J)
- 256-Mbit Low Power Synchronous DRAM (the M65KA256AF)

The purpose of this document is to describe how the two memory components operate with respect to each other. It must be read in conjunction with the M58PR512J and M65KA256AF datasheets, where all specifications required to operate the Flash memory and SDRAM components are fully detailed. These datasheets are available from the Numonyx website *www.numonyx.com*.

Recommended operating conditions do not allow more than one memory to be active at the same time.

The memory is delivered in a Stacked TFBGA105 package. In order to meet environmental requirements, Numonyx offers the M39P0R9080E0 in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label.

The M39P0R9080E0 is supplied with all the bits erased (set to ‘1’).

Figure 1. Logic diagram

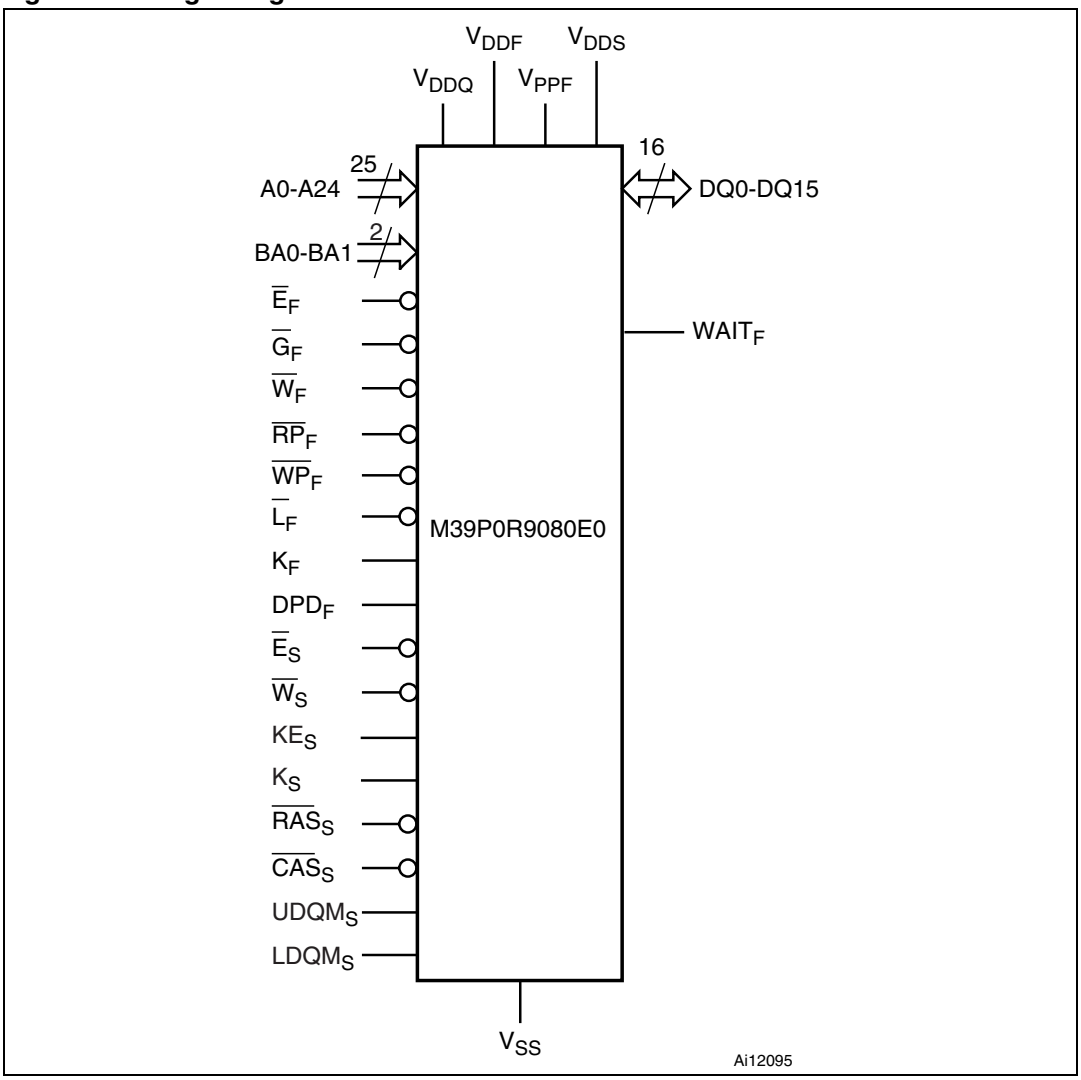
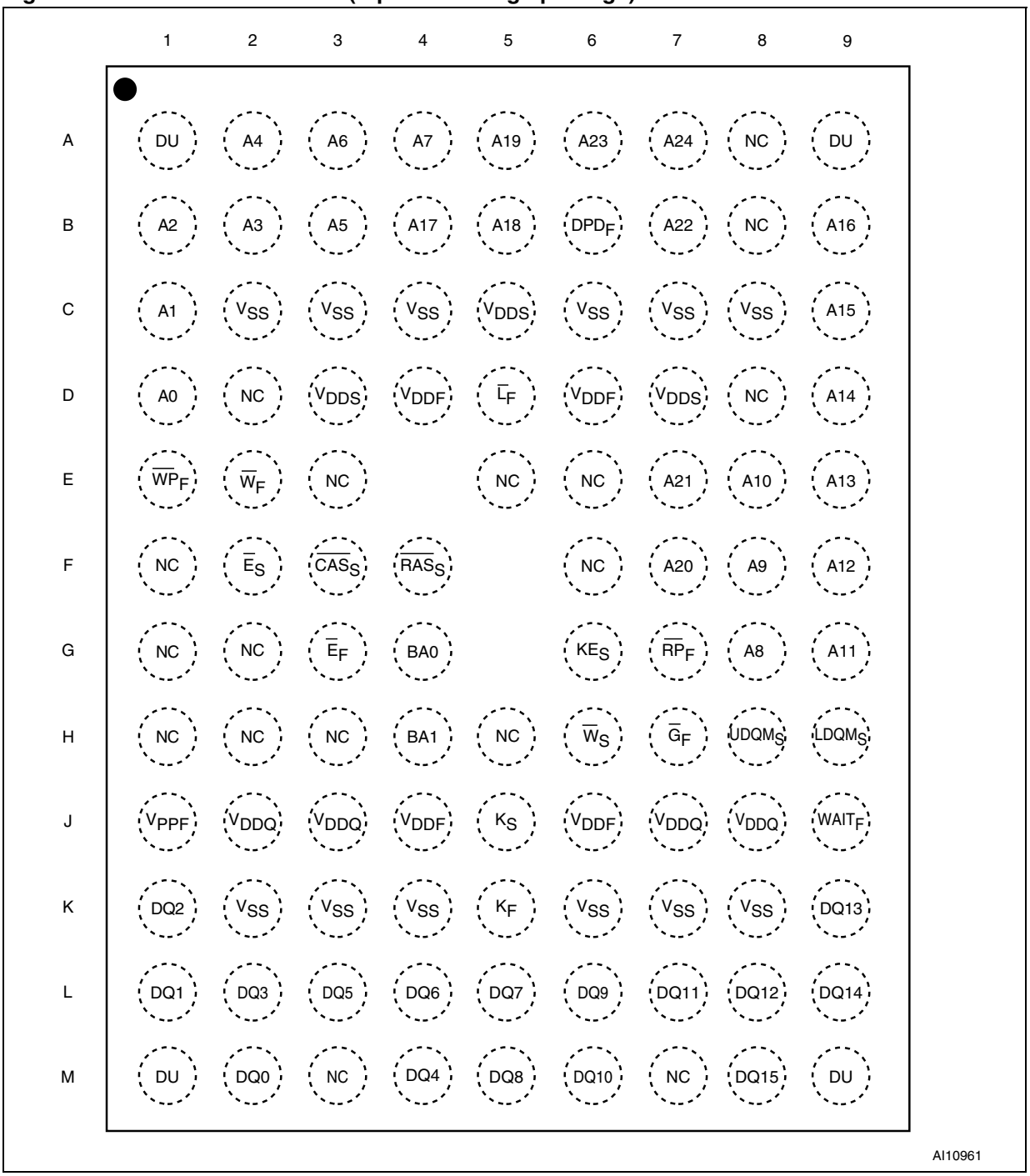


Table 1. Signal names

A0-A24[1]	Address Inputs
DQ0-DQ15	Common Data Input/Output
V_{DDQ}	Common Flash and LPSDRAM Power Supply for I/O Buffers
V_{PPF}	Flash Memory Optional Supply Voltage for Fast Program & Erase
V_{DDF}	Flash Memory Power Supply
V_{DDS}	LPSDRAM Power Supply
V_{SS}	Ground
NC	Not Connected Internally
DU	Do Not Use as Internally Connected
Flash Memory	
$\overline{E}_F$	Chip Enable input
$\overline{G}_F$	Output Enable Input
$\overline{W}_F$	Write Enable input
$\overline{RP}_F$	Reset input
$\overline{WP}_F$	Write Protect input
$\overline{L}_F$	Latch Enable input
K_F	Burst Clock
$WAIT_F$	Wait Output
DPD_F	Deep Power-Down
Low Power SDRAM	
$\overline{E}_S$	Chip Enable Input
$\overline{W}_S$	Write Enable input
K_S	LPSDRAM Clock input
KE_S	LPSDRAM Clock Enable input
$\overline{CAS}_S$	Column Address Strobe Input
$\overline{RAS}_S$	Row Address Strobe Input
BA0, BA1	Bank Select Inputs
$UDQM_S$	Upper Data Input/Output Mask
$LDQM_S$	Lower Data Input/Output Mask

1. A13-A24 are Address Inputs for the Flash memory component only.

Figure 2. TFBGA connections (top view through package)



2 Signal descriptions

See *Figure 1: Logic diagram* and *Table 1: Signal names*, for a brief overview of the signals connect-ed to this device.

2.1 Address inputs (A0-A24)

A0-A12 are common to the Flash memory and LPSDRAM components. A13-A24 are Address Inputs for the Flash memory component only. In the Flash memory, the Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the Program/Erase Controller.

In the LPSDRAM, the A0-A12 Address Inputs are used to select the row or column to be made active. If a column is selected, only the nine least significant Address Inputs, A0-A8, are used. In this latter case, A10 determines whether Auto Precharge is used. If A10 is High (set to '1') during Read or Write, the Read or Write operation includes an Auto Precharge cycle. If A10 is Low (set to '0') during Read or Write, the Read or Write cycle does not include an Auto Precharge cycle.

2.2 LPSDRAM Bank Select Address Inputs (BA0-BA1)

The BA0 and BA1 Bank Select Address Inputs are used by the LPSDRAM to select the bank to be made active. The LPSDRAM must be enabled, the Row Address Strobe, $\overline{RAS}_S$, must be Low, V_{IL}, the Column Address Strobe, $\overline{CAS}_S$, and $\overline{W}_S$ must be High, V_{IH}, when selecting the addresses. The address inputs are latched on the rising edge of the clock signal, K_S.

2.3 Data Inputs/Outputs (DQ0-DQ15)

In the Flash memory, the Data I/O output the data stored at the selected address during a Bus Read operation or input a command or the data to be programmed during a Bus Write operation.

In the LPSDRAM, the Data Inputs/Outputs are common to all memory components. They output the data stored at the selected address during a Read operation, or are used to input the data during a write operation.

2.4 Flash memory Chip Enable input ($\overline{E}_F$)

The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is at V_{IL} and Reset is at V_{IH} the device is in active mode. When Chip Enable is at V_{IH} the memory is deselected, the outputs are high impedance and the power consumption is reduced to the standby level. It is not allowed to have E_F and E_S all at V_{IL} at the same time, only one memory component should be enabled at a time.

2.5 Flash memory Output Enable ($\overline{G}_F$)

The Output Enable input controls data outputs during the Bus Read operation of the memory.

2.6 Flash memory Write Enable ($\overline{W}_F$)

The Write Enable input controls the Bus Write operation of the Flash memory's Command Interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable whichever occurs first.

2.7 Flash memory Write Protect input ($\overline{WP}_F$)

Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is at V_{IL}, the Lock-Down is enabled and the protection status of the Locked-Down blocks cannot be changed. When Write Protect is at V_{IH}, the Lock-Down is disabled and the Locked-Down blocks can be locked or unlocked. (See M58PR512J datasheet for details).

2.8 Flash memory Reset ($\overline{RP}_F$)

The Reset input provides a hardware reset of the memory. When

Reset is at V_{IL}, the memory is in reset mode: the outputs are high impedance and the current consumption is reduced to the Reset Supply Current

I_{DD2}. Refer to the M58PRxxxJ datasheet for the value of I_{DD2}. After Reset all blocks are in the Locked state and the Configuration Register is reset. When Reset is at V_{IH}, the device is in normal operation. Exiting reset mode the device enters asynchronous read mode, but a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs. The Reset pin can be interfaced with 3V logic without any additional circuitry. It can be tied to V_{RPH} (refer to the M58PRxxxJ datasheet).

2.9 Flash memory Deep Power-Down (DPD_F)

The Deep Power-Down input is used to put the Flash memory in Deep Power-Down mode.

When the Flash memory is in Standby mode and the Enhanced Configuration Register bit ECR15 is set, asserting the Deep Power-Down input will cause the memory to enter the Deep Power-Down mode.

When the device is in the Deep Power-Down mode, the memory cannot be modified and the data is protected.

The polarity of the DPD_F pin is determined by ECR14. The Deep Power-Down input is active Low by default.

2.10 Flash memory Latch Enable ($\overline{L}_F$)

The Latch Enable input latches the address bits on its rising edge. The address latch is transparent when Latch Enable is at V_{IL} and it is inhibited when Latch Enable is at V_{IH}. Latch Enable can be kept Low (also at board level) when the Latch Enable function is not required or supported.

2.11 Flash memory Clock (K_F)

The clock input synchronizes the memory to the microcontroller during synchronous read operations; the address is latched on a Clock edge (rising or falling, according to the configuration settings) when Latch Enable is at V_{IL}. Clock is ignored during asynchronous read and in write operations.

2.12 Flash memory Wait ($WAIT_F$)

Wait is an output signal used during synchronous read to indicate whether the data on the output bus are valid. This output is high impedance when Chip Enable is at V_{IH}, Output Enable is at V_{IH}, or Reset is at V_{IL}. It can be configured to be active during the wait cycle or one data cycle in advance.

2.13 LPSDRAM Chip Select ($\overline{E}_S$)

The Chip Select input $\overline{E}_S$ activates the LPSDRAM state machine, address buffers and decoders when driven Low, V_{IL}. When $\overline{E}_S$ is High, V_{IH}, the device is not selected.

2.14 LPSDRAM Column Address Strobe ($\overline{CAS}_S$)

The Column Address Strobe, $\overline{CAS}_S$, is used in conjunction with Address Inputs A8-A0 and BA1-BA0, to select the starting column location prior to a Read or Write.

2.15 LPSDRAM Row Address Strobe ($\overline{RAS}_S$)

The Row Address Strobe, $\overline{RAS}_S$, is used in conjunction with Address Inputs A11-A0 and BA1-BA0, to select the starting address location prior to a Read or Write.

2.16 LPSDRAM Write Enable ($\overline{W}_S$)

The Write Enable input, $\overline{W}_S$, controls writing to the LPSDRAM.

2.17 LPSDRAM Clock input (K_S)

The Clock signal, K_S, is used to clock the Read and Write cycles. During normal operation, the Clock Enable pin, KES, is High, V_{IH}. The clock signal K_S can be suspended to switch the device to the Self Refresh, Power-Down or Deep Power-Down mode by driving KE_S Low, V_{IL}.

2.18 LPSDRAM Clock Enable (KE_S)

The Clock Enable, KE_S, pin is used to control the synchronizing of the signals to Clock signal K_S. The signals are clocked when KE_S is High, V_{IH} When KE_S is Low, V_{IL}, the signals are no longer clocked and data Read and Write cycles are extended. KE_S is also involved in switching the device to the Self Refresh, Power-Down and Deep Power-Down modes.

2.19 LPSDRAM lower/upper data input/output mask ($LDQM_S$/$UDQM_S$)

Lower Data Input/Output Mask and Upper Data Input/Output Mask pins are input signals used to mask the Read or Write data. The DQM latency is two clock cycles for read operations and there is no latency for write operations.

2.20 Flash memory V_{DDF} supply voltage

V_{DDF} provides the power supply to the internal core of the Flash memory component. It is the main power supply for all operations (Read, Program and Erase).

2.21 LPSDRAM V_{DDS} supply voltage

V_{DDS} provides the power supply to the internal core of the LPSDRAM component. It is the main power supply for all operations (Read and Write).

2.22 V_{DDQ} supply voltage

V_{DDQ} is common to the Flash memory and LPSDRAM components. It provides the power supply to the I/O pins and enables all Outputs to be powered independently of V_{DDF} for the Flash memory, or V_{DDS} for the LPSDRAM. V_{DDQ} can be tied to V_{DDF} or V_{DDS}, or can use a separate supply.

2.23 Flash memory V_{PPF} Program supply voltage

V_{PPF} is both a control input and a power supply pin. The two functions are selected by the voltage range applied to the pin. If V_{PP} is kept in a low voltage range (0V to V_{DDQ}) V_{PP} is seen as a control input. In this case a voltage lower than V_{PPLK} gives an absolute protection against program or erase, while $V_{PP} > V_{PP1}$ enables these functions (see the M58PRxxxJ datasheet for the relevant values). V_{PP} is only sampled at the beginning of a program or erase; a change in its value after the operation has started does not have any effect and program or erase operations continue. If V_{PP} is in the range of V_{PPH} it acts as a power supply pin. In this condition V_{PP} must be stable until the Program/Erase algorithm is completed.

2.24 V_{SS} ground

V_{SS} ground is common to the LPSDRAM and Flash memory components. It is the reference for the core supply. It must be connected to the system ground.

Note: Each device in a system should have V_{DDF},V_{DDS}, V_{DDQ} and V_{PPF} decoupled with a 0.1µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See Figure 5: AC measurement load circuit The PCB track widths should be sufficient to carry the required V_{PPF} program and erase currents.

3 Functional description

The LPSDRAM and Flash memory components have separate power supplies but share the same grounds. They are distinguished by two Chip Enable inputs: $\overline{E}_F$ for the Flash memory and $\overline{E}_S$ for the LPSDRAM.

Recommended operating conditions do not allow more than one device to be active at a time. The most common example is a simultaneous read operations on the Flash memory and the LPSDRAM which would result in a data bus contention. Therefore it is recommended to put the other devices in the high impedance state when reading the selected device.

Figure 3. Functional block diagram

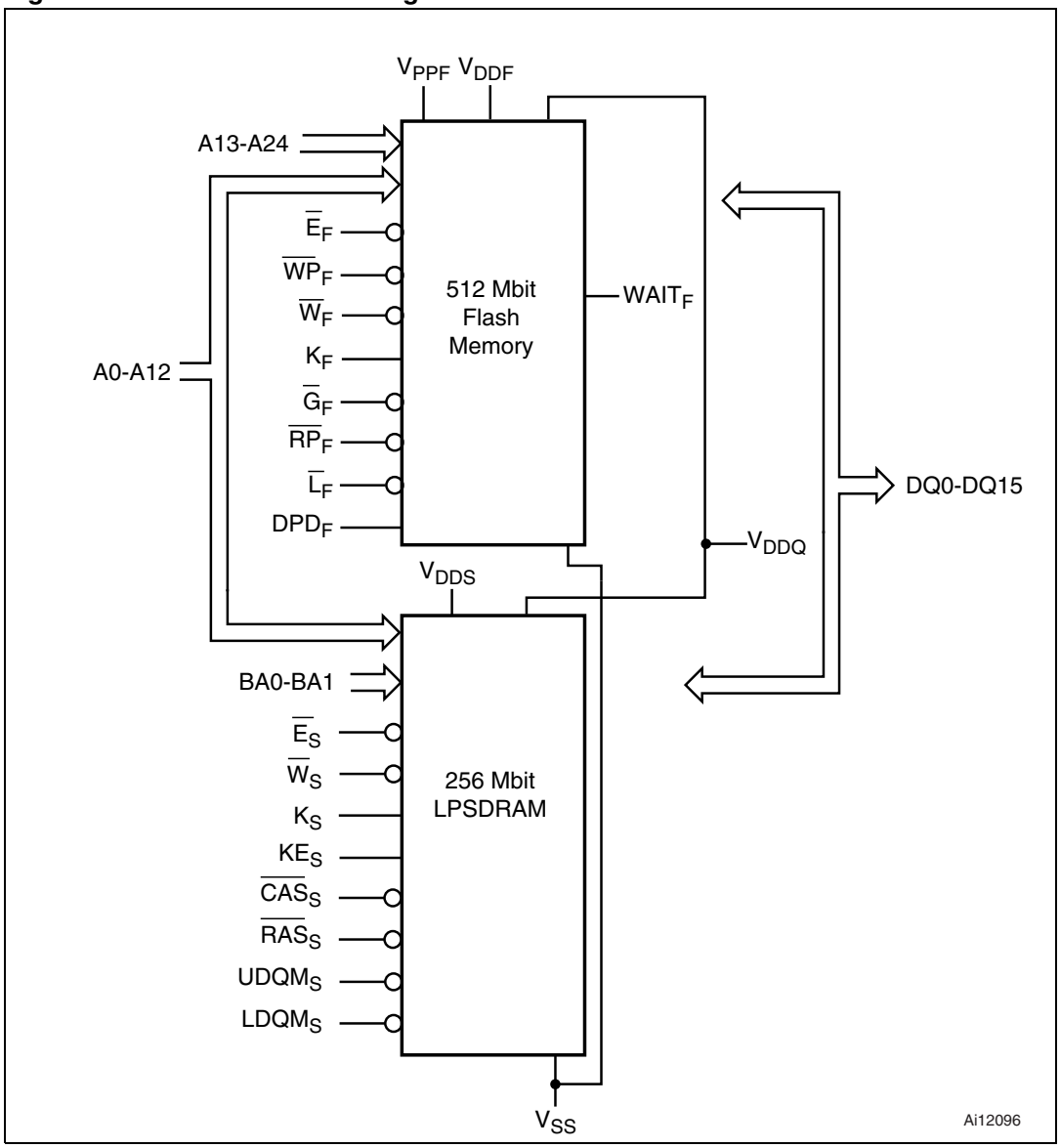


Table 2. Bus operations(1)

	Operation	$\overline{E}_F$	$\overline{G}_F$	$\overline{W}_F$	$\overline{L}_F$	$\overline{RP}_F$	DPD_F(2)	$WAIT_F$(3)	$\overline{E}_S$	$\overline{RAS}_S$	$\overline{CAS}_S$	$\overline{W}_S$	KE_Sn-1	KE_Sn	A10	A9, A11	A0-A7	BA0-BA1	$UDQM_S$/$LDQM_S$	DQ15-DQ0
Flash memory	Bus Read	V_{IL}	V_{IL}	V_{IH}	V_{IL}(4)	V_{IH}	de-a(5)		The SDRAM must be disabled											Data Output
	Bus Write	V_{IL}	V_{IH}	V_{IL}	V_{IL}(4)	V_{IH}	de-a(5)													Data Input
	Address Latch	V_{IL}	X	V_{IH}	V_{IL}	V_{IH}	de-a(5)													Data Output or Hi-Z(6)
	Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{IH}	de-a(5)	Hi-Z	Any SDRAM operation mode is allowed.											Hi-Z
	Standby	V_{IH}	X	X	X	V_{IH}	de-a(5)	Hi-Z												Hi-Z
	Reset	X	X	X	X	V_{IL}	de-a(5)	Hi-Z												Hi-Z
	Deep Power-Down	V_{IH}	X	X	X	V_{IH}	a(7)	Hi-Z												Hi-Z
SDRAM	Burst Read	The Flash memory must be disabled							V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	V_{IL}	V	SCA	BS	V	Data Output
	Burst Write								V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	V_{IL}	V	SCA	BS	X	Data Input
	Self Refresh								V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X			X	X	–
	Auto Refresh								V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X			X	X	–
	Power-Down with Precharge	Any Flash memory operation mode is allowed							V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	X			X	X	X
									V_{IH}	X	X	X								
	Deep Power-Down								V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X			X	X	X
	Device Deselect								V_{IH}	X	X	X	V_{IH}	X	X	X	X	X	X	X
	No Operation								V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	X				X	X

1. X = Don't care, de-a = de-asserted, a = asserted, SCA = Start Column Address, BS = Bank Select, V = Valid.
2. The DPD signal polarity depends on the value of the ECR14 bit.
3. $WAIT_F$ signal polarity is configured using the Set Configuration Register command.
4. $\overline{L}_F$ can be tied to V_{IH} if the valid address has been previously latched.
5. If ECR15 is set to '0', the device cannot enter the Deep Power-Down mode, even if DPD_F is asserted.
6. Depends on $\overline{G}_F$.
7. ECR15 has to be set to ‘1’ for the device to enter Deep Power-Down.

4 Maximum rating

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the Numonyx SURE Program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient Operating Temperature	–25	85	°C
T_{BIAS}	Temperature Under Bias	–25	85	°C
T_{STG}	Storage Temperature	–55	125	°C
V_{IO}	Input or Output Voltage	–0.5	2.6	V
V_{DDF}	Supply Voltage	–1.0	3.0	V
V_{DDS}	LPSDRAM Supply Voltage	–0.5	2.6	V
V_{DDQ}	Input/Output Supply Voltage	–0.5	2.6	V
V_{PPF}	Program Voltage	–1.0	11.5	V
I_O	Output Short Circuit Current		100	mA
t_{VPPH}	Time for V_{PP} at V_{PPH}		100	hours

5 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 4: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 4. Operating and AC measurement conditions

Parameter[1][2]	Flash memory		LPSDRAM		Unit
	Min	Max	Min	Max	
V_{DDF} Supply Voltage	1.7	1.95	–	–	V
V_{DDS} Supply Voltage	–	–	1.7	1.95	V
V_{DDQ} Supply Voltage	1.7	1.95	1.7	1.95	V
V_{PPF} Supply Voltage (Factory environment)	8.5	9.5	–	–	V
V_{PPF} Supply Voltage (Application environment)	–0.4	V_{DDQ}+0.4	–	–	V
Ambient Operating Temperature	–25	85	–25	85	°C
Impedance Output (Z_0)	50				Ω
Load Capacitance (C_L)	30		30		pF
Output Circuit Protection Resistance (R)	50				Ω
Input Rise and Fall Times		3	0.5		ns
Input Pulse Voltages	0 to V_{DDQ}		0.2 to 1.6		V
Input and Output Timing Ref. Voltages	$V_{DDQ}/2$		0.9		V

1. All voltages are referenced to V_{SS} = 0V.
2. T_A = 25°C, f = 1MHz

Figure 4. AC measurement I/O waveform

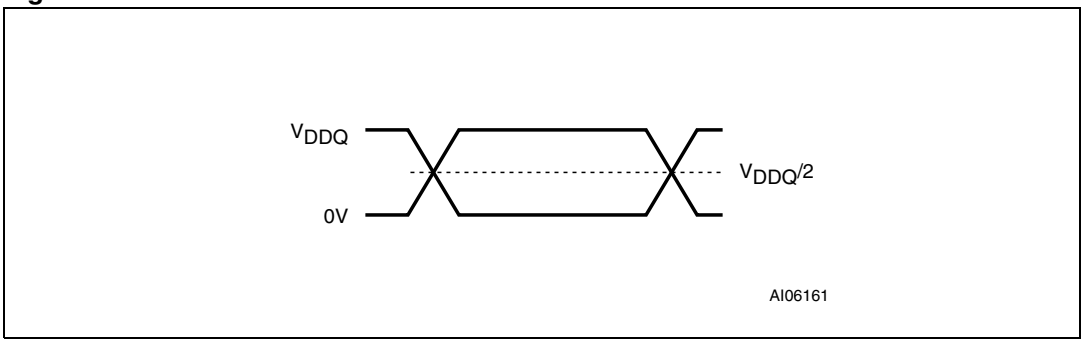


Figure 5. AC measurement load circuit

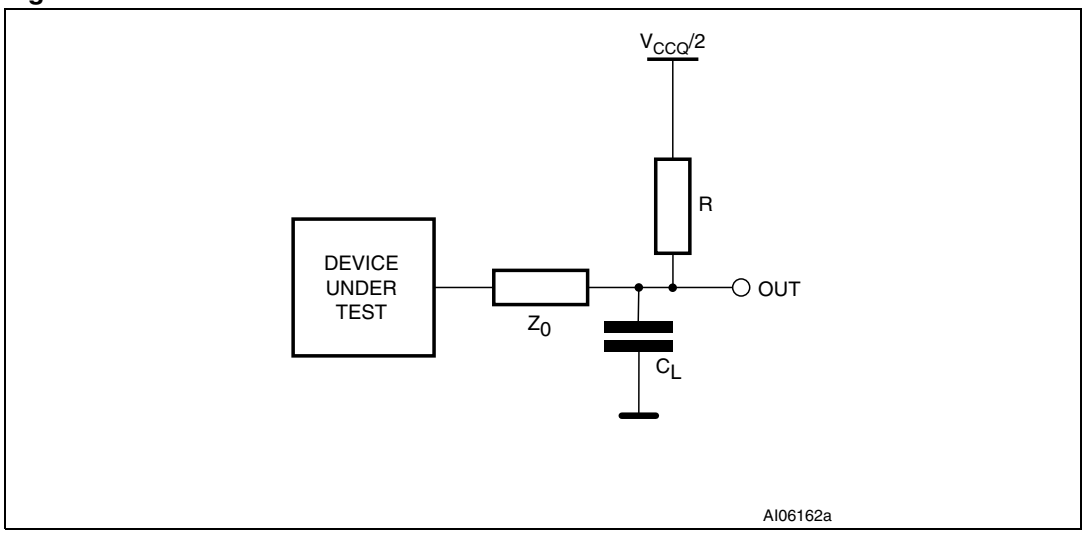


Table 5. Capacitance(1)

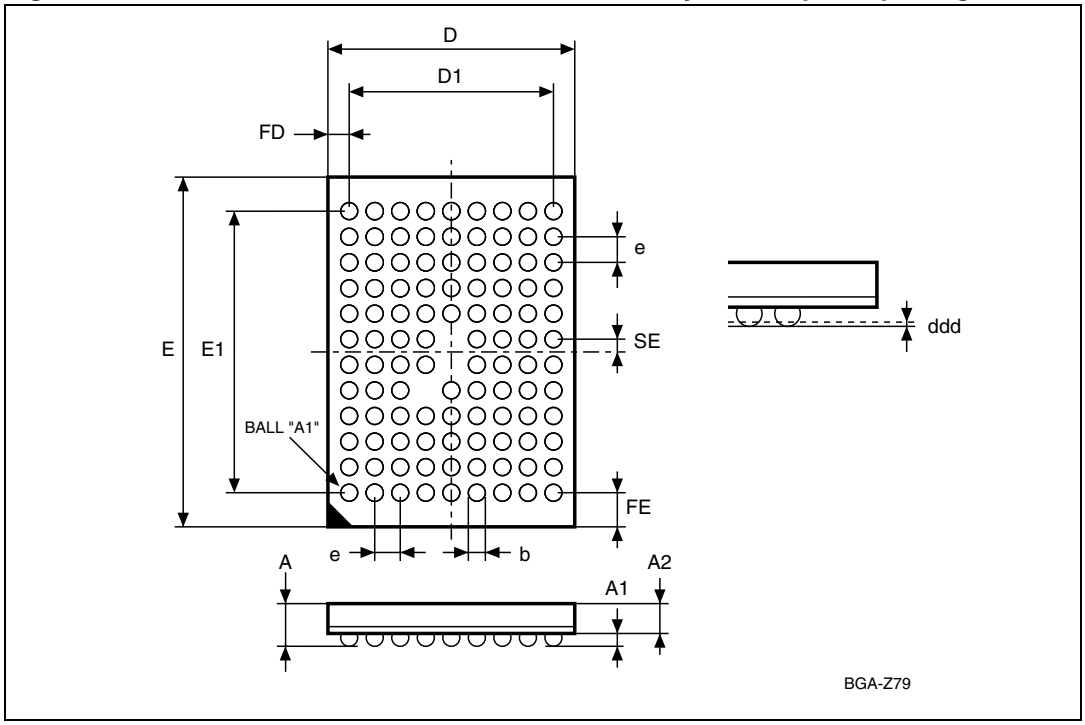
Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	–	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	–	15	pF

1. Sampled only, not 100% tested.

Please refer to the M58PRxxxL and M65KA256AF datasheets for further DC and AC characteristics values and illustrations.

6 Package mechanical

Figure 6. TFBGA105 9x11mm - 9x12 active ball array, 0.8mm pitch, package outline



1. Drawing is not to scale.

Table 6. TFBGA105 9x11mm - 9x12 active ball array, 0.8mm pitch, mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.20			0.008	
A2	0.80			0.031		
b	0.35	0.30	0.40	0.014	0.012	0.016
D	9.00	8.90	9.10	0.354	0.350	0.358
D1	6.40			0.252		
ddd			0.10			0.004
E	11.00	10.90	11.10	0.433	0.429	0.437
E1	8.80			0.346		
e	0.80	–	–	0.031	–	–
FD	1.30			0.051		
FE	1.10			0.043		
SE	0.40			0.016		

7 Part numbering

Table 7. Ordering information scheme

Example: M39 P 0 R 9 0 8 0 E 0 ZAD E

Device Type

M39 = Multi-Chip Package (Flash + LPSDRAM)

Flash 1 Architecture

P = Multi-Level, Multiple Bank, Large Buffer

Flash 2 Architecture

0 = No Die

Operating Voltage

R = V_{DDF} = V_{DDS} = V_{DDQ} = 1.7 to 1.95 V

Flash 1 Density

9 = 512 Mbits

Flash 2 Density

0 = No Die

RAM 1 Density

8 = 256 Mbit

RAM 0 Density

0 = No Die

Parameter Blocks Location

E = Even Block Flash Memory Configuration

Product Version

0 = 90nm Flash technology, 96 ns speed; LPSDRAM

Package

ZAD = stacked TFBGA105 D stacked footprint.

Option

Blank = Standard Packing

E = ECOPACK® Package, Standard packing

F = ECOPACK® Package, Tape & Reel packing

Note: Devices are shipped from the factory with the memory content bits erased to '1'. For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the Numonyx Sales Office nearest to you.

8 Revision history

Table 8. Document revision history

Date	Revision	Changes
15-Dec-2005	0.1	Initial release.
12-Oct-2006	1	Document status promoted from Target Specification to full Datasheet. Voltage ranges extended to 1.95V. *Flash memory* features updated to match the data in revision 2 of the M58PRxxxJ datasheet (random access time, programming time and V_{PPF} modified). *Table 2: Bus operations* modified. V_{PPF} max modified in *Table 3: Absolute maximum ratings*. Input Pulse voltages modified for SDRAM in *Table 4: Operating and AC measurement conditions*. Flash memory and SDRAM DC characteristics tables removed (see M58PRxxxJ and M65KA256AF datasheets for details).
30-Nov-2007	2	Applied Numonyx branding.

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