M39P0R9080E4
M39P0R1080E4

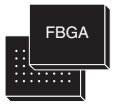
512 Mb or 1 Gb (x16, multiple bank, multilevel, burst) Flash memory 256 Mbit low power SDRAM, 1.8 V supply, multichip package

Features

- Multichip package
  - 1 die of 512 Mbit (32 Mb ×16) or 1 Gbit (64 Mb ×16) multiple bank, multilevel, burst) Flash memory
  - 1 die of 256 Mbit (4 banks of 4 Mb x16) low power synchronous dynamic RAM
- Supply voltage
  - $V_{DDF} = V_{CCP} = V_{DDQ} = 1.7$ to 1.95 V
  - $V_{PPF} = 9$ V for fast program
- Electronic signature
  - Manufacturer code: 20h
  - 512 Mbit device code: 8819
  - 1 Gbit device code: 880F
- ECOPACK® packages available

Flash memory

- Synchronous/asynchronous read
  - Synchronous Burst Read mode: 108 MHz, 66 MHz
  - Asynchronous Page Read mode
  - Random access: 96 ns
- Programming time
  - 4.2 µs typical word program time using Buffer Enhanced Factory Program command
- Memory organization
  - Multiple bank memory array: 64 Mbit banks (512 Mb devices) 128 Mbit banks (1Gb devices)
  - Four EFA (extended flash array) blocks of 64 Kbits
- Dual operations
  - program/erase in one bank while read in others
  - No delay between read and write operations
- 100,000 program/erase cycles per block



TFBGA165 (ZAS)
9 x 11 mm

- Block locking
  - All blocks locked at power-up
  - Any combination of blocks can be locked with zero latency
  - $\overline{WP}_F$ for block lock-down
  - Absolute write protection with $V_{PPF} = V_{SS}$
- Security
  - 64-bit unique device number
  - 2112-bit user programmable OTP cells
- CFI (Common Flash Interface)

LPSDRAM

- 256 Mbit synchronous dynamic RAM
  - Organized as 4 banks of 4 Mwords, each 16 bits wide
- Synchronous burst read and write
  - Fixed burst lengths: 1, 2, 4, 8 words or full page
  - Burst types: sequential and interleaved
  - Clock frequency: 133 MHz (7.5 ns speed)
  - $\overline{CAS}$ latency 3 at 133 MHz
- Automatic and controlled precharge
- Low power features:
  - PASR (partial array self refresh),
  - TCSR (automatic temperature compensated self refresh)
  - DS (driver strength)
  - Deep Power-Down mode
- Auto refresh and self refresh

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1 Description

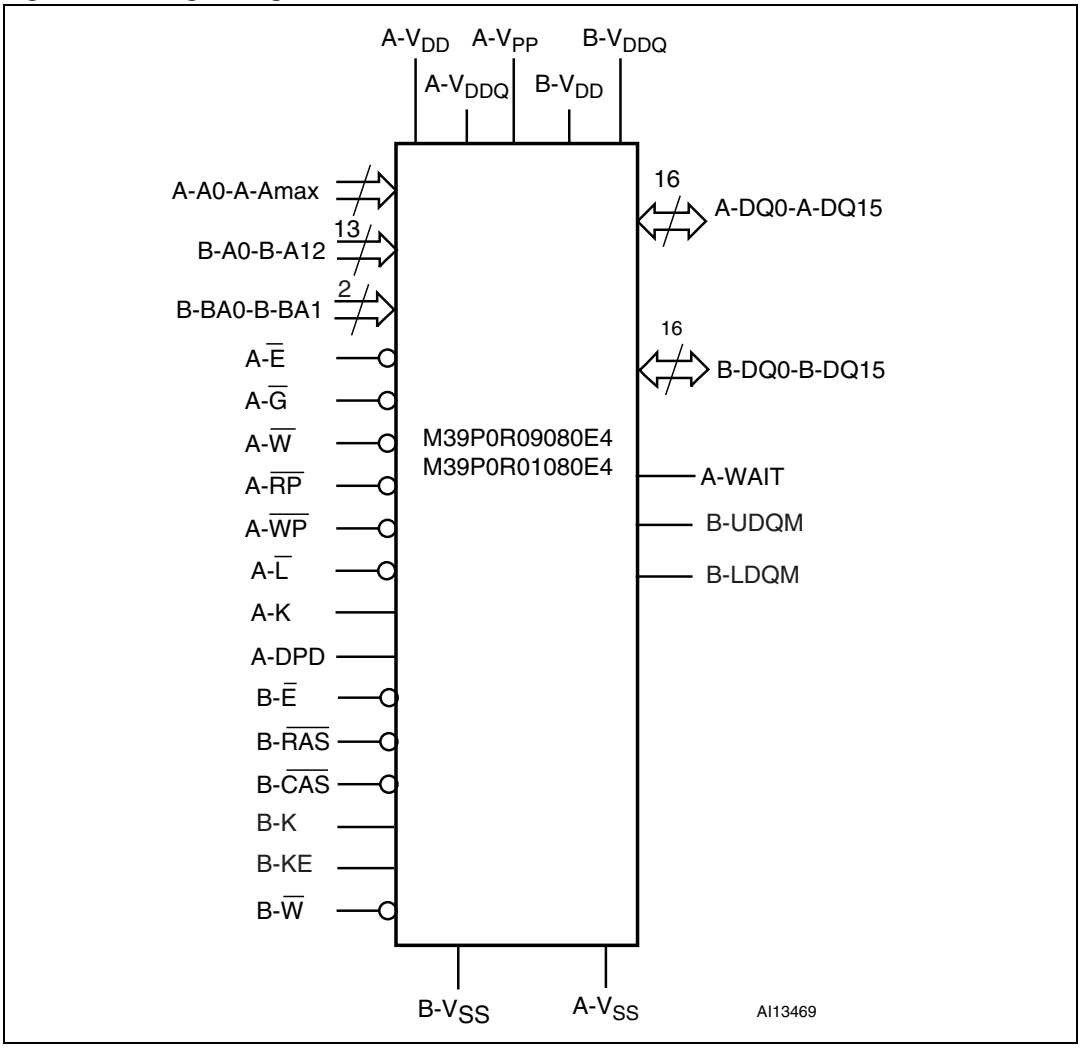
The M39P0R9080E4 and M39P0R1080E4 combine two memory devices in a multichip package:

- a 512-Mbit (M58PR512LE) or 1 Gbit (M58PR001LE) multiple bank Flash memory
- a 256-Mbit low power synchronous DRAM (the M65KA256Ax)

The purpose of this document is to describe how the two memory components operate with respect to each other. It should be read in conjunction with the M58PRxxxLE and M65KA256Ax datasheets, which fully detail all the specifications required to operate the Flash memory and LPSDRAM components.

The memory is offered in a stacked TFBGA165 package, and is supplied with all the bits erased (set to '1').

Figure 1. Logic diagram



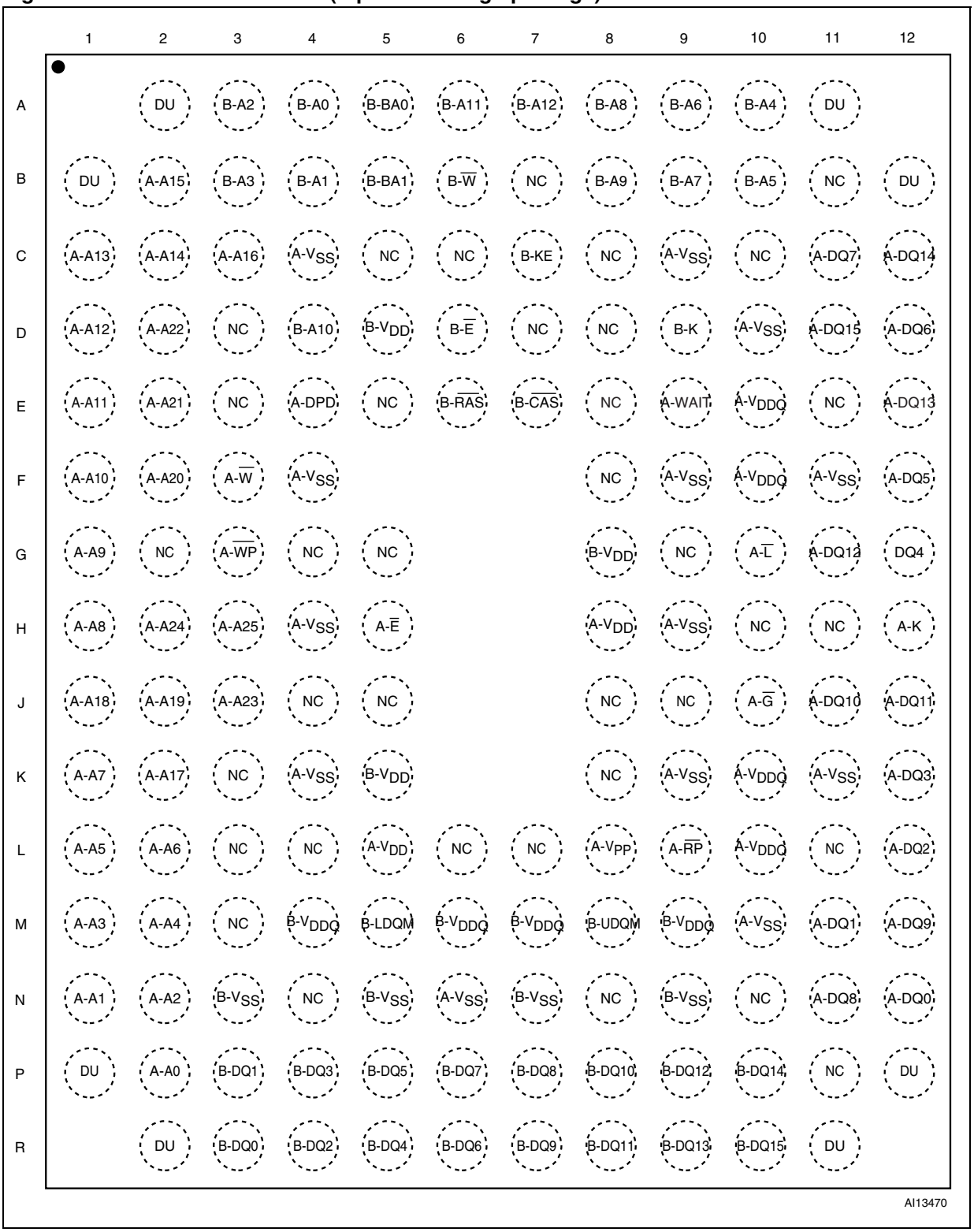
1. The Flash memory component is connected to the A bus whereas the LPSDRAM component is on the B bus.
2. Amax is A-A24 in the M39P0R9080E4 and it is A-A25 in the M39P0R1080E4.

Table 1. Signal names

Signal	Function	Direction
NC	Not connected internally	N/A
DU	Do not use as internally connected	N/A
Flash memory signals		
A-A0-A-Amax(1)	Address Inputs	Input
A-DQ0-A-DQ15	Data Inputs/Outputs	Input/output
A-$\overline{E}$	Chip Enable	Input
A-$\overline{G}$	Output Enable	Input
A-$\overline{W}$	Write Enable	Input
A-$\overline{RP}$	Reset	Input
A-$\overline{WP}$	Write Protect	Input
A-$\overline{L}$	Latch Enable	Input
A-K	Burst Clock	Input
A-WAIT	Wait	Output
A-DPD	Deep Power-Down	Input
A-V_{DDQ}	Power supply for I/O buffers	Power supply
A-V_{PP}	Optional supply voltage for fast program and erase	Power supply
A-V_{DD}	Power supply	Power supply
A-V_{SS}	Ground	N/A
Low Power SDRAM signal		
B-A0-B-A12	Address Inputs	Input
B-DQ0-B-DQ15	Data Inputs/Outputs	Input/output
B-$\overline{E}$	Chip Enable	Input
B-$\overline{W}$	Write Enable	Input
B-K	LPSDRAM Clock	Input
B-KE	LPSDRAM Clock Enable	Input
B-$\overline{CAS}$	Column Address Strobe	Input
B-$\overline{RAS}$	Row Address Strobe	Input
B-BA0, B-BA1	Bank Select	Input
B-UDQM	Upper Data Input/Output Mask	Input/output
B-LDQM	Lower Data Input/Output Mask	Input/output
B-V_{DD}	Power supply	Power supply
B-V_{DDQ}	Input/output supply voltage	Power supply
B-V_{SS}	Ground	N/A

1. Amax is A24 in the M39P0R9080E4 and it is A25 in the M39P0R1080E4.

Figure 2. TFBGA connections (top view through package)



2 Signal descriptions

See *Figure 1: Logic diagram* and *Table 1: Signal names*, for a brief overview of the signals connected to this device.

2.1 A bus

All Flash memory signals are connected to the A bus. They are described below.

2.1.1 Flash memory address inputs (A-A0-A-Amax)

Amax is the highest order Address Input. It is equal to A-A24 in the M39P0R9080E4, and to A-A25 in the M39P0R1080E4.

The Address Inputs select the cells in the memory array to access during bus read operations. During bus write operations they control the commands sent to the Command Interface of the Program/Erase Controller.

2.1.2 Flash memory data Inputs/Outputs (A-DQ0-A-DQ15)

The Data I/O output the data stored at the selected address during a bus read operation or input a command or the data to be programmed during a bus write operation.

2.1.3 Flash memory Chip Enable input (A-$\overline{E}$)

The Chip Enable input activates the memory control logic, input buffers, decoders, and sense amplifiers. When Chip Enable is at V_{IL} and Reset is at V_{IH} the device is in active mode. When Chip Enable is at V_{IH} the memory is deselected, the outputs are high impedance, and the power consumption is reduced to the standby level.

2.1.4 Flash memory Output Enable (A-$\overline{G}$)

The Output Enable input controls data outputs during the bus read operation of the memory.

2.1.5 Flash memory Write Enable (A-$\overline{W}$)

The Write Enable input controls the bus write operation of the Flash memory's Command Interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable, whichever occurs first.

2.1.6 Flash memory Write Protect input (A-$\overline{WP}$)

Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is at V_{IL}, the lock-down is enabled and the protection status of the locked-down blocks cannot be changed. When Write Protect is at V_{IH}, the lock-down is disabled and the locked-down blocks can be locked or unlocked. (See the M58PRxxxLE datasheet for details).

2.1.7 Flash memory Reset (A-$\overline{RP}$)

The Reset input provides a hardware reset of the memory. When Reset is at V_{IL}, the memory is in reset mode: the outputs are high impedance and the current consumption is reduced to the Reset Supply Current I_{DD2}. Refer to the M58PRxxxLE datasheet, for the value of I_{DD2}. After Reset, all blocks are in the locked state and the Configuration Register is reset. When Reset is at V_{IH}, the device is in normal operation. Exiting reset mode, the device enters asynchronous read mode, but a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs. The Reset pin can be interfaced with 3V logic without any additional circuitry. It can be tied to V_{RPH} (refer to the M58PRxxxLE datasheet).

2.1.8 Flash memory Deep Power-Down (A-DPD)

The Deep Power-Down input is used to put the Flash memory in deep power-down mode.

When the Flash memory is in standby mode and the Enhanced Configuration Register bit ECR15 is set, asserting the Deep Power-Down input causes the memory to enter the deep power-down mode.

When the device is in the deep power-down mode, the memory cannot be modified and the data is protected.

The polarity of the A-DPD pin is determined by ECR14. The Deep Power-Down input is active Low by default.

2.1.9 Flash memory Latch Enable (A-$\overline{L}$)

The Latch Enable input latches the address bits on its rising edge. The address latch is transparent when Latch Enable is at V_{IL} and it is inhibited when Latch Enable is at V_{IH}. Latch Enable can be kept Low (also at board level) when the Latch Enable function is not required or supported.

2.1.10 Flash memory Clock (A-K)

The clock input synchronizes the memory to the microcontroller during synchronous read operations; the address is latched on a Clock edge when Latch Enable is at V_{IL}. Clock is ignored during asynchronous read and in write operations.

2.1.11 Flash memory Wait (A-WAIT)

Wait is an output signal used during synchronous read to indicate whether the data on the output bus are valid. This output is high impedance when Chip Enable is at V_{IH}, Output Enable is at V_{IH}, or Reset is at V_{IL}. It can be configured to be active during the wait cycle or one data cycle in advance.

2.1.12 Flash memory A-V_{DD} supply voltage

A-V_{DD} provides the power supply to the internal core of the Flash memory component. It is the main power supply for all operations (read, program and erase).

2.1.13 Flash memory A-V_{DDQ} supply voltage

A-V_{DDQ} provides the power supply to the I/O pins and enables all outputs to be powered independently of A-V_{DD}. A-V_{DDQ} can be tied to A-V_{DD} or can use a separate supply.

A-V_{DDQ} is sampled at the beginning of program/erase operations. If A-V_{DDQ} is lower than V_{LKOQ}, the device is reset.

2.1.14 Flash memory A-V_{PP} program supply voltage

A-VPP is both a control input and a power supply pin. The two functions are selected by the voltage range applied to the pin. If A-V_{PP} is kept in a low voltage range (0V to A-V_{DDQ}) A-V_{PP} is seen as a control input. In this case a voltage lower than V_{PPLK} gives an absolute protection against program or erase, while A-V_{PP} > V_{PP1} enables these functions (see the M58PRxxxLE datasheet for the relevant values). A-V_{PP} is only sampled at the beginning of a program or erase operation; a change in its value after the operation has started does not have any effect and program or erase operations continue. If A-V_{PP} is in the range of V_{PPH} it acts as a power supply pin. In this condition A-V_{PP} must be stable until the program/erase algorithm is completed.

2.1.15 Flash memory A-V_{SS} ground

A-V_{SS} ground is the reference for the Flash memory's core supply. It must be connected to the system ground.

Note: Each device in a system should have A-V_{DD}, A-V_{DDQ} and A-V_{PPF} decoupled with a 0.1µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See Figure 6: AC measurement load circuit. The PCB track widths should be sufficient to carry the required A-V_{PP} program and erase currents.

2.2 B bus

All LPSDRAM signals are connected to the B bus. They are described below.

2.2.1 LPSDRAM address Inputs (B-A0-B-A12)

The B-A0-B-A12 Address Inputs are used to select the row or column to be made active. If a row is selected, all thirteen, B-A0-B-A12 Address Inputs are used. If a column is selected, only the nine least significant Address Inputs, B-A0-B-A8, are used. In this latter case, B-A10 determines whether Auto Precharge is used. If B-A10 is High (set to '1') during read or write, the read or write operation includes an auto precharge cycle. If B-A10 is Low (set to '0') during read or write, the read or write cycle does not include an auto precharge cycle.

2.2.2 LPSDRAM Bank Select Address Inputs (B-BA0-B-BA1)

The B-BA0 and B-BA1 Banks Select Address Inputs select the bank to be made active.

When selecting the addresses, the device must be enabled, the Row Address Strobe, B-$\overline{RAS}$, must be Low, V_{IL}, the Column Address Strobe, B-$\overline{CAS}$, and B-$\overline{W}$ must be High, V_{IH}. The address inputs are latched on the rising edge of the clock signal, B-K.

2.2.3 LPSDRAM Data Inputs/Outputs (B-DQ0-B-DQ15)

The Data Inputs/Outputs output the data stored at the selected address during a read operation, or are used to input the data during a write operation.

2.2.4 LPSDRAM Chip Select (B-$\overline{E}$)

The Chip Select input B-$\overline{E}$ activates the LPSDRAM state machine, address buffers and decoders when driven Low, V_{IL}. When High, V_{IH}, the device is not selected.

2.2.5 LPSDRAM Column Address Strobe (B-$\overline{CAS}$)

The Column Address Strobe, B-$\overline{CAS}$, is used in conjunction with Address Inputs B-A8-B-A0 and B-BA1-B-BA0, to select the starting column location prior to a read or write operation.

2.2.6 LPSDRAM Row Address Strobe (B-$\overline{RAS}$)

The Row Address Strobe, B-$\overline{RAS}$, is used in conjunction with Address Inputs B-A11-B-A0 and B-BA1-B-BA0, to select the starting address location prior to a read or write.

2.2.7 LPSDRAM Write Enable (B-$\overline{W}$)

The Write Enable input, B-$\overline{W}$, controls writing to the LPSDRAM.

2.2.8 LPSDRAM Clock Input (B-K)

The Clock signal, B-K, is used to clock the read and write cycles. During normal operation, the Clock Enable pin, B-KE, is High, V_{IH}. The clock signal B-K can be suspended to switch the device to the self refresh, power-down or deep power-down mode by driving B-KE Low, V_{IL}.

2.2.9 LPSDRAM Clock Enable (B-KE)

The Clock Enable, B-KE, pin is used to control the synchronizing of the signals to Clock signal B-K. The signals are clocked when B-KE is High, V_{IH} When B-KE is Low, V_{IL}, the signals are no longer clocked and data read and write cycles are extended. B-KE is also involved in switching the device to the self refresh, power-down and deep power-down modes.

2.2.10 LPSDRAM Lower/Upper Data Input/Output Mask (B-LDQM/B-UDQM)

Lower Data Input/Output Mask and Upper Data Input/Output Mask pins are input signals used to mask the read or write data. The DQM latency is two clock cycles for read operations and there is no latency for write operations.

2.2.11 LPSDRAM B-V_{DD} supply voltage

B-V_{DD} provides the power supply to the internal core of the LPSDRAM component. It is the main power supply for all operations (read and write).

2.2.12 LPSDRAM B-V_{DDQ} supply voltage

B-V_{DDQ} provides the power supply to the I/O pins and enables all outputs to be powered independently of B-V_{DD}. B-V_{DDQ} can be tied to B-V_{DD} or can use a separate supply.

It is recommended to power-up and power-down B-V_{DD} and B-V_{DDQ} together to avoid certain conditions that would result in data corruption.

2.2.13 LPSDRAM B-V_{SS} ground

Ground, B-$V_{SS,}$ is the reference for the LPSDRAM's core power supply. It must be connected to the system ground.

3 Functional description

The M39P0R9080E4 and M39P0R1080E4 consist of two distinct buses – the A and B buses.

The Flash memory component is connected to the A bus and the LPSDRAM component is connected to the B bus. The connections are shown in *Figure 3* and *Figure 4*. The components, therefore, have separate signals, separate power supplies, and grounds and can be operated simultaneously with no risk of bus contention.

Figure 3. Functional block diagram - A bus

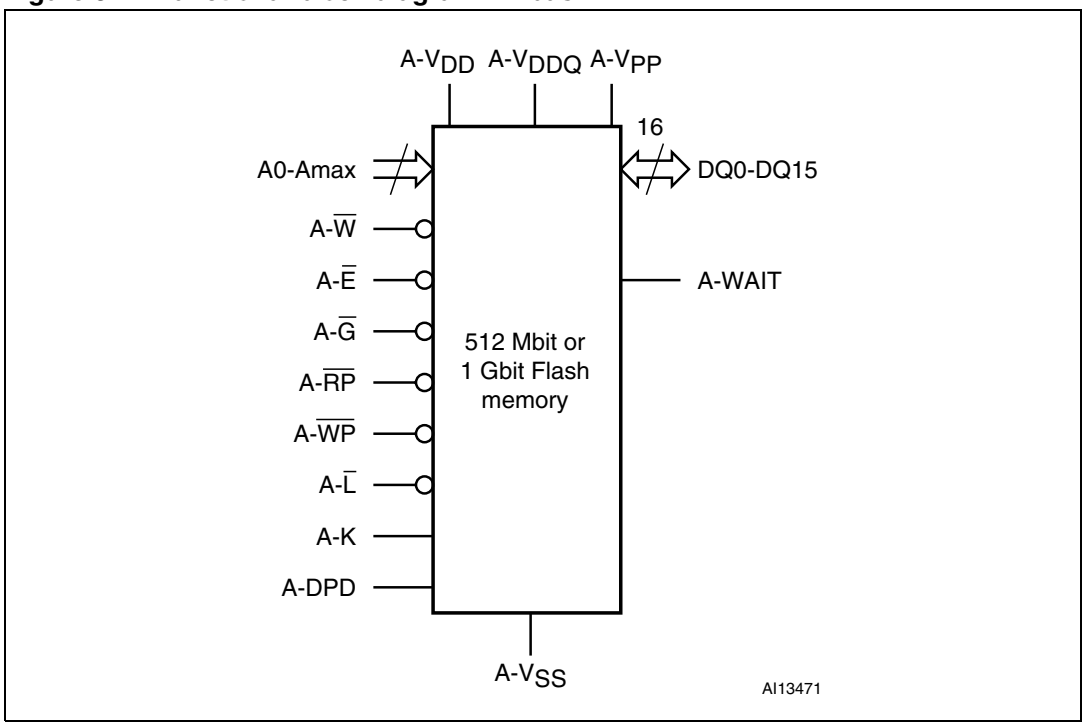
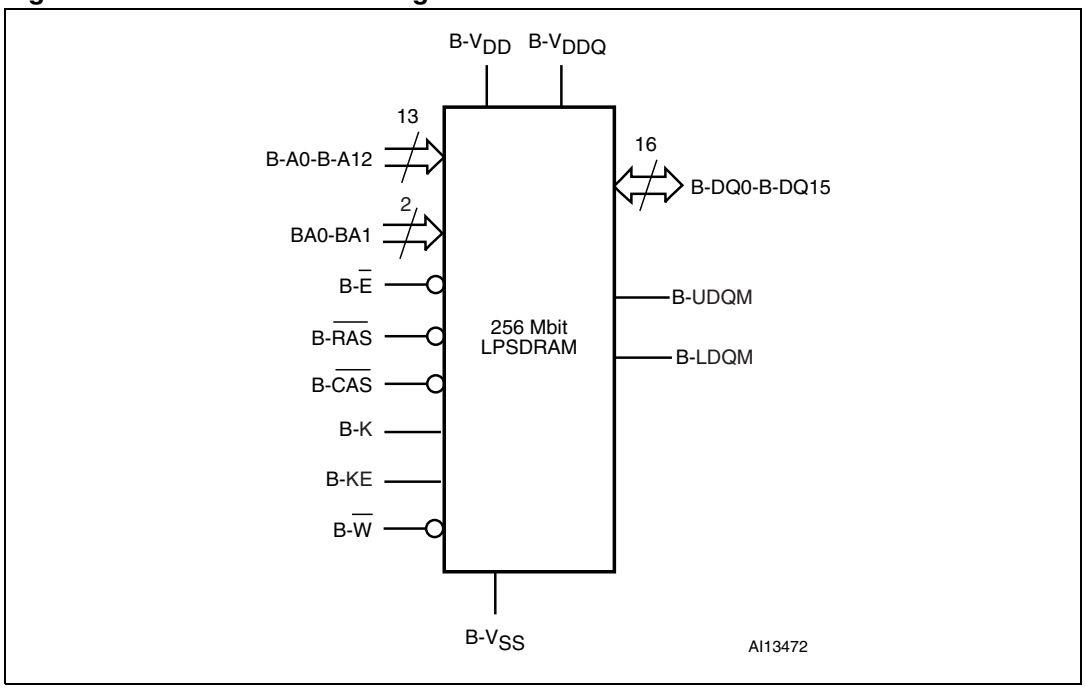


Figure 4. Functional block diagram - B bus



Main bus operations

AS the Flash memory and LPSDRAM components are connected to separate buses, there is no limitation to the modes allowed in one of them while the other is active. Refer to the M58PRxxxLE and M65KA256Ax datasheets for the details of the each memory's bus operations.

4 Maximum rating

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer to the Numonyx SURE Program and other relevant quality documents.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient operating temperature	–25	85	°C
T_{BIAS}	Temperature under bias	–25	85	°C
T_{STG}	Storage temperature	–55	125	°C
V_{IO}	Input or output voltage	–0.5	2.6	V
V_{DDF}	Supply voltage	–1.0	3.0	V
V_{DDS}	LPSDRAM supply voltage	–0.5	2.6	V
V_{DDQ}	Input/output supply voltage	–0.5	2.6	V
V_{PPF}	Program voltage	–1.0	11.5	V
I_O	Output short circuit current		100	mA
t_{VPPH}	Time for V_{PP} at V_{PPH}		100	hours

5 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in *Table 3: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 3. Operating and AC measurement conditions

Parameter[1][2]	Flash memory		LPSDRAM		Unit
	Min	Max	Min	Max	
V_{DDF} supply voltage	1.7	1.95	–	–	V
V_{DDS} supply voltage	–	–	1.7	1.95	V
V_{DDQ} supply voltage	1.7	1.95	1.7	1.95	V
V_{PPF} supply voltage (factory environment)	8.5	9.5	–	–	V
V_{PPF} supply voltage (application environment)	–0.9	2.0	–	–	V
Ambient operating temperature	–25	85	–25	85	°C
Impedance output (Z_0)	50				Ω
Load capacitance (C_L)	30		30		pF
Output circuit protection resistance (R)	50				Ω
Input rise and fall times		3	0.5		ns
Input pulse voltages	0 to V_{DDQ}		0.2 to 1.6		V
Input and output timing ref. voltages	$V_{DDQ}/2$		0.9		V

1. All voltages are referenced to V_{SS} = 0V.
2. T_A = 25°C, f = 1MHz

Figure 5. AC measurement I/O waveform

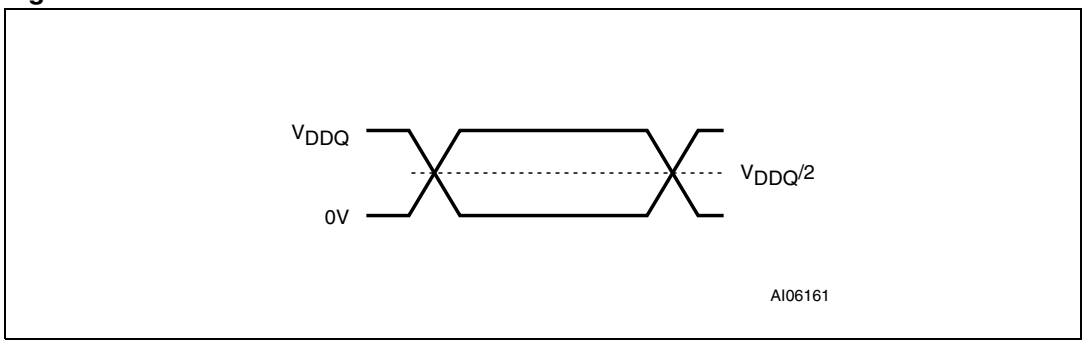


Figure 6. AC measurement load circuit

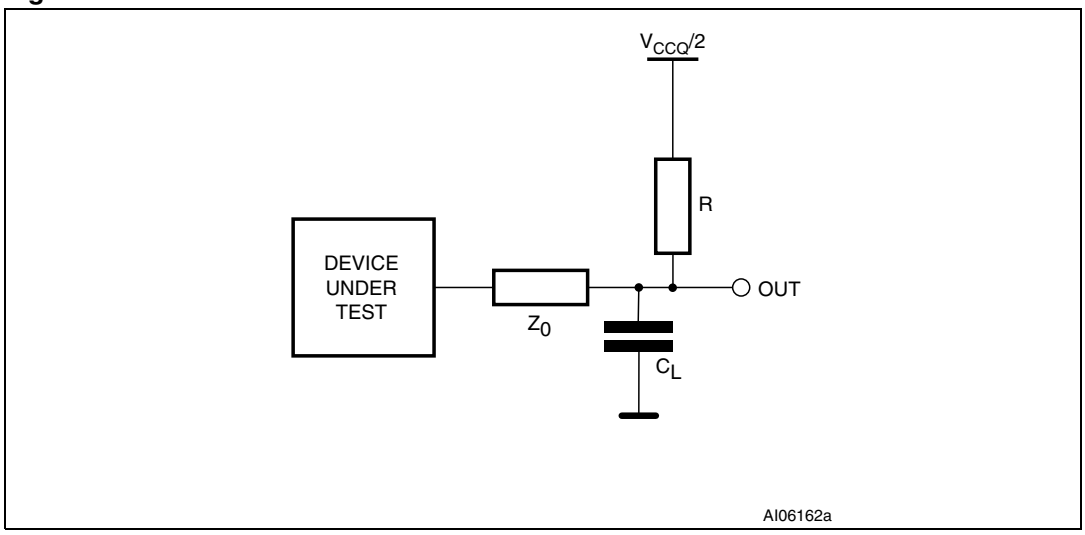


Table 4. Capacitance

Symbol	Parameter	Test condition	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0V	–	12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0V	–	15	pF

1. Sampled only, not 100% tested.

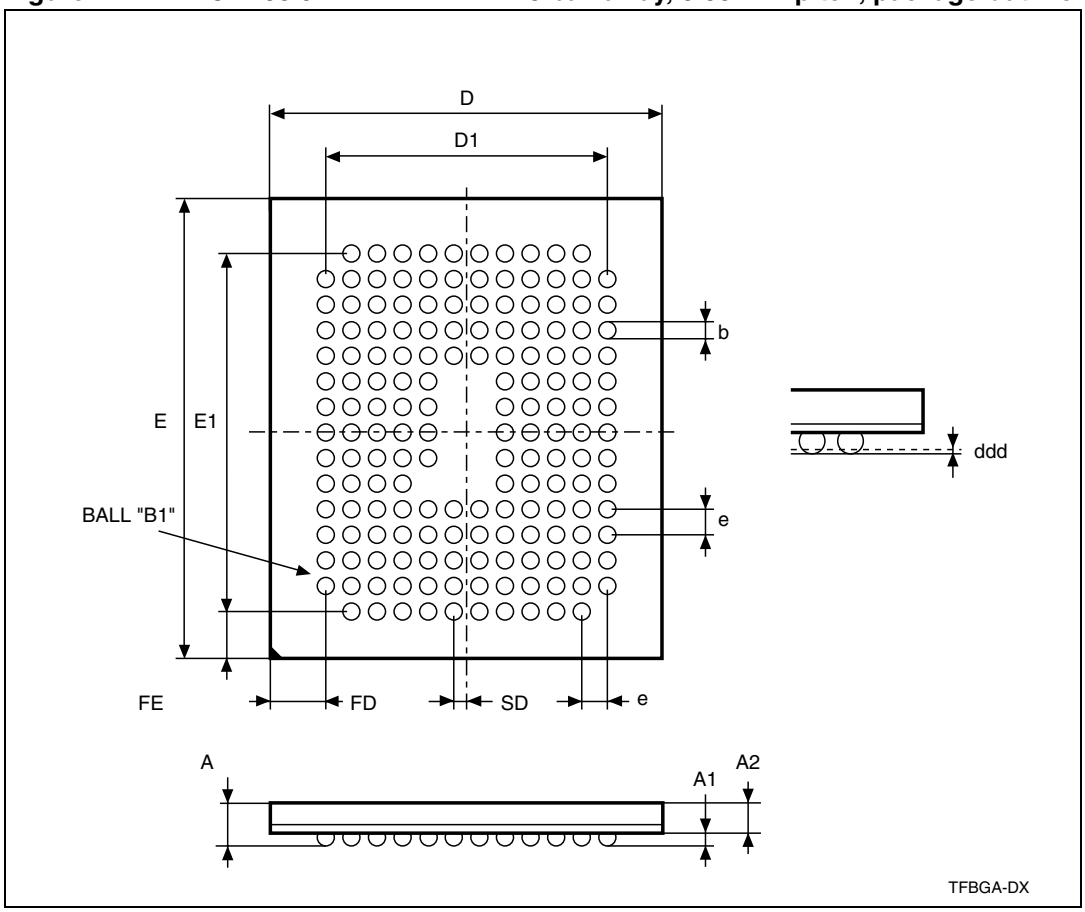
Please refer to the M58PRxxxLE and M65KA256Ax datasheets for further DC and AC characteristic values and illustrations.

6 Package mechanical

To meet environmental requirements, Numonyx offers these devices in ECOPACK® packages. These packages have a lead-free, second-level interconnect. In compliance with JEDEC Standard JESD97, the category of second-level interconnect is marked on the package and on the inner box label.

The maximum ratings related to soldering conditions are also marked on the inner box label.

Figure 7. TFBGA165 9 × 11 mm - 12 × 15 ball array, 0.65 mm pitch, package outline



1. Drawing is not to scale.

Table 5. TFBGA165 9 × 11 mm - 12 × 15 ball array, 0.65 mm pitch, package mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.200			0.0079	
A2	0.800			0.0315		
b	0.350	0.300	0.400	0.0138	0.0118	0.0157
D	9.000	8.900	9.100	0.3543	0.3504	0.3583
D1	7.150			0.2815		
ddd			0.100			0.0039
E	11.000	10.900	11.100	0.4331	0.4291	0.4370
E1	9.100			0.3583		
e	0.650	–	–	0.0256	–	–
FD	0.925			0.0364		
FE	0.950			0.0374		
SD	0.325			0.0128		

7 Part numbering

Table 6. Ordering information scheme

Example: M39 P 0 R 9 0 8 0 E 4 ZAS E

Device type

M39 = Multichip package (Flash + LPSDRAM)

Flash 1 architecture

P = Multilevel, multiple bank, large buffer

Flash 2 architecture

0 = No die

Operating voltage

R = V_{DDF} = V_{DDS} = V_{DDQ} = 1.7 to 1.95V

Flash 1 density

9 = 512 Mbits

1 = 1 Gbit

Flash 2 density

0 = No die

RAM 1 density

8 = 256 Mbit

RAM 0 density

0 = No Die

Parameter blocks location

E = Even block flash memory configuration

Product version

4 = 65 nm Flash technology, 96 ns speed; LPSDRAM

Package

ZAS = stacked TFBGA165 S stacked footprint.

Option

E = ECOPACK® package, standard packing

F = ECOPACK® package, tape and reel packing

Note: Devices are shipped from the factory with the memory content bits erased to '1'. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the Numonyx sales office nearest to you.

8 Revision history

Table 7. Document revision history

Date	Revision	Changes
28-Sep-2006	0.1	Initial release.
06-Oct-2006	0.2	V_{DDF}, V_{CCP} and V_{DDQ} voltage ranges extended to 1.95V.
28-Jun-2007	1	Changed all references to M65KA256AF to M65KA256Ax. Updated *Figure 7*, and removed standard packing option from *Table 6*.
14-Nov-2007	2	Applied Numonyx branding.

Please Read Carefully: