EPSON

SED1526/28 Series

Dot Matrix LCD Controller Driver

- Ultra Low Power Consumption
- Built-in Power Supply Circuit for LCD
- 97 Driver Outputs

■ DESCRIPTION

The SED1526 series is a single-chip LCD driver for dot-matrix liquid crystal displays (LCD's). It accepts serial or 8-bit parallel display data directly from a microprocessor and stores data in an on-chip display RAM. It can generate an LCD drive signal independent from microprocessor clock.
As the SED1526 series features the very low power dissipation and wide operating voltage range, it can easily realize a powerful but compact display unit having a small battery.
A single chip of SED1526 series can drive a 17×80-pixel or 33×64-pixel LCD panel.

(Note: The SED1526 series are not designed to have EMI resistance.)

■ FEATURES

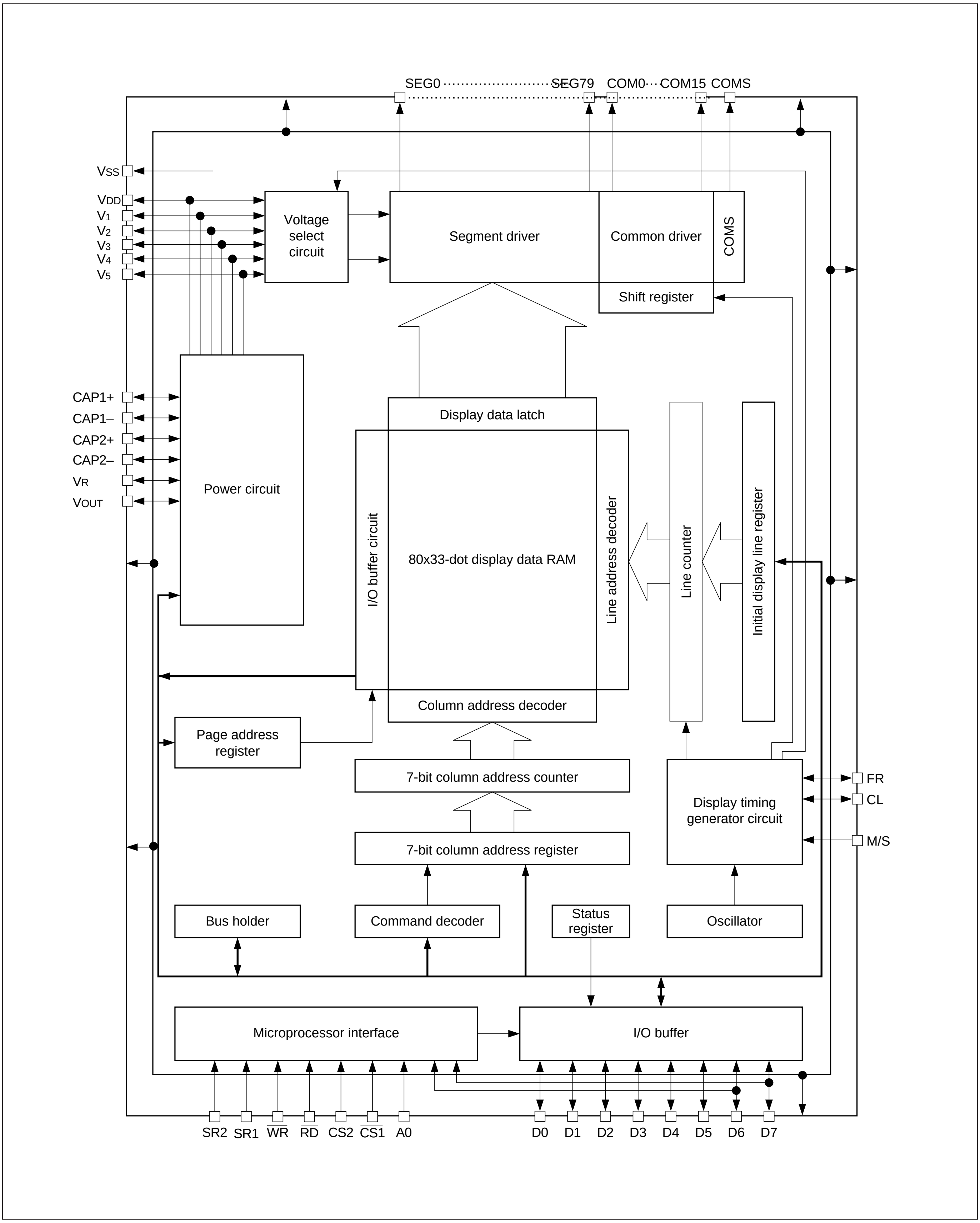
- Direct data display using the display RAM. When RAM data bit is 0, it is not displayed; when 1, it is displayed.
- Large 80×33-bit RAM capacity
- On-chip LCD driver circuit (97 segment and common drivers)
- High-speed, 8-bit microprocessor interface allowing direct connection to both the 8080 and 6800
- Supported serial interface
- Rich command functions (upward compatible to SED1520 Series); they are Read/Write Display Data, Display On/Off Switching, Set Page Address, Set Initial Display Line, Set Column Address, Read Status, Static Drive On/Off Switching, Select Duty, Duty+1, Read-Modify-Write, Select Segment Driver Direction, Power Save, Reset, Set Power Control, Set Electronic Controls, Clock Stop.
- On-chip CR oscillation circuit (OSC)
- On-chip LCD power circuit (The internal and external LCD power supplies are software selectable.)
- Very low power consumption
- Flexible power voltages; 2.4 to 6.0 V (for logic) and -13.0 to -4.0V(V_{DD}-V_5)
- –40 to +85°C wide operating temperature range
- CMOS process
- Package: QFP5-128pin (plastic), Die form (Al pad, Au bump)

■ LINE UP (Series specifications: ex. 128-pin flat package)

Model	Operating clock (Internal OSC)	Duty	Segment driver	Common driver	VREG type	CMOS pin positions
SED1526F0A	20 KHz	1/8, 1/9, 1/16, 1/17	80	17	Tpye 1	Type A
SED1526FAA	20 KHz	1/8, 1/9, 1/16, 1/17	80	17	Tpye 1	Type B
SED1526FEA	20 KHz	1/8, 1/9, 1/16, 1/17	80	17	Tpye 2	Type A
SED1528F0A	20 KHz	1/32, 1/33	64	33	Type 1	Type A

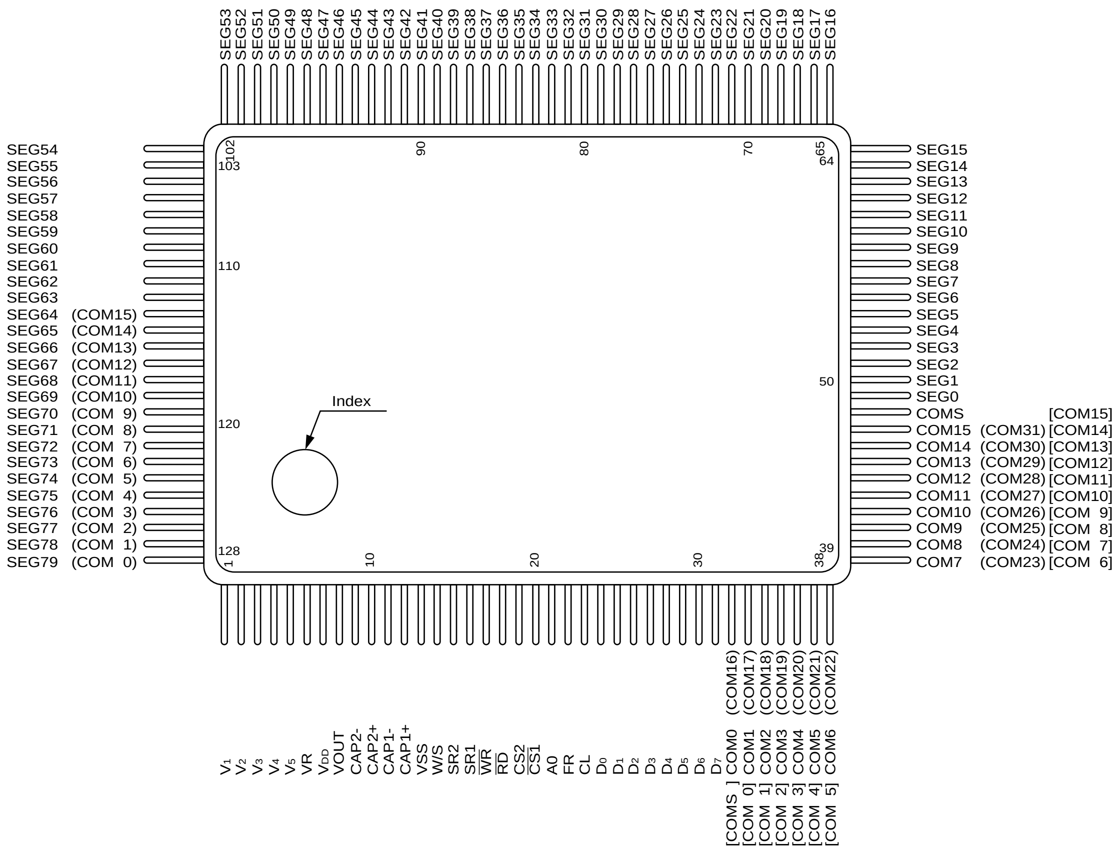
Type 1 VREG (Built-in power supply regulating voltage)
Temperature gradient: 0.17%/°C
Type 2 VREG (Built-in power supply regulating voltage)
Temperature gradient: 0.00%/°C
Refer to No. P3 (Package pin layout), No. P4 (PAD layout) and No. P5 (PAD coordinates).
An SED1526 series package has one of following subcodes according to its package type (an example of SED1526):
SED1526F0A: QFP5-128pin flat package
SED1526D0*: Bear chip
SED1526D0A having aluminium pad
SED1526D0B having gold bump
SED1526T**: TCP

■ BLOCK DIAGRAM (SED1526*0*)

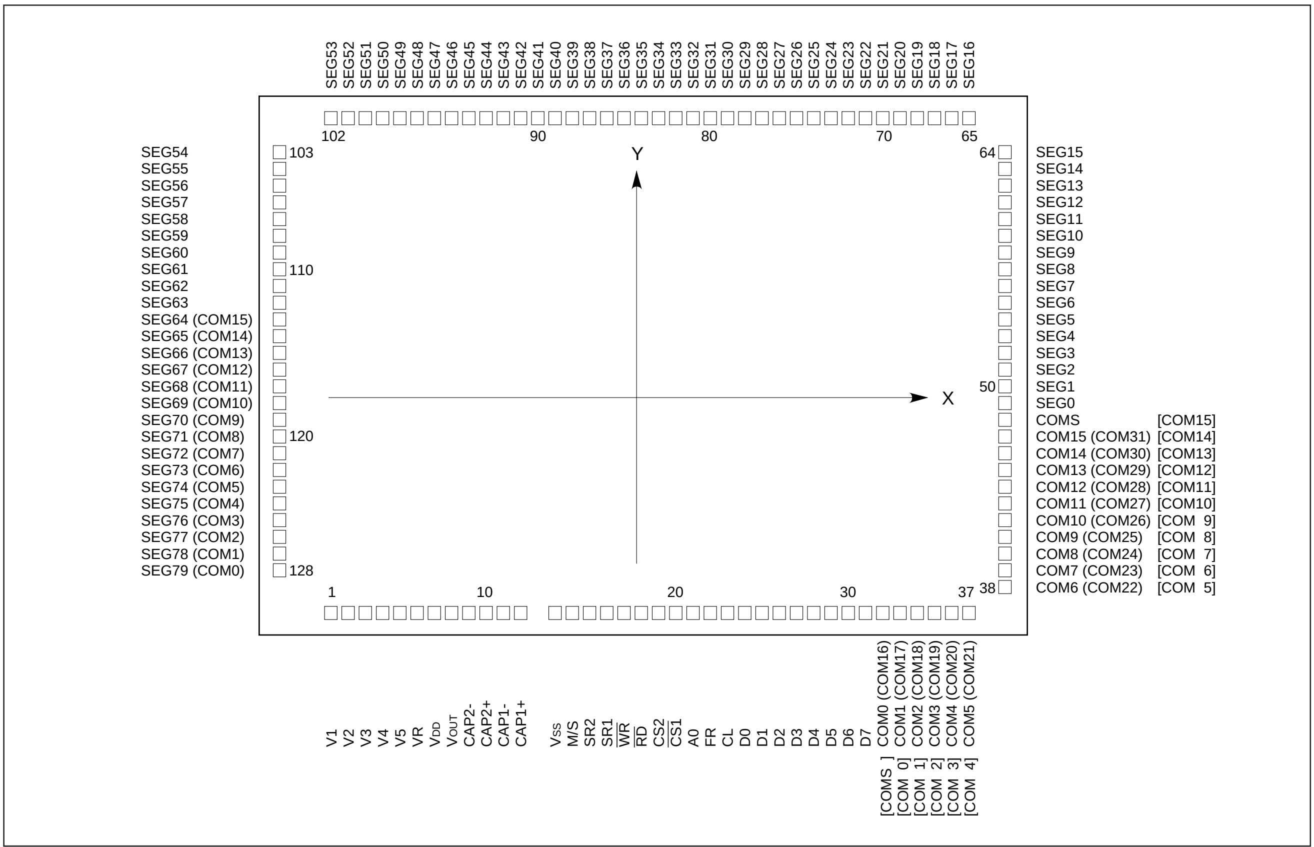


■ PIN ASSIGNMENT

● Package Pin Assignment



■ PAD LAYOUT



* Pin names in ( ) apply to SED1528.
* Pin names in [ ] apply to SED1526DA✻ (CMOS pin = Type B).

Aluminum pad chip
- Chip size: 5.92 mm × 4.68 mm
- Chip thickness: 0.4 mm
- Pad opening: 90.2 µm × 90.2 µm
- Pad pitch: 130 µm (Min)

Gold bump chip (reference)
- Chip size: 5.92 mm × 4.68 mm
- Chip thickness: 0.4 mm
- Bump size: 81.7 µm × 81.7 µm
- Bump height: 22.5 µm

■ PAD COORDINATES

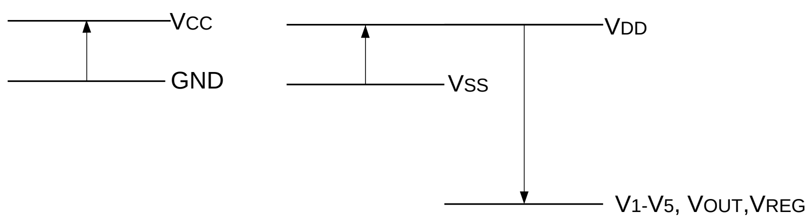
Unit: µm

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	V_1	–2767	–2106	65	SEG16	2516	2185
2	V_2	–2637		66	SEG17	2367	
3	V_3	–2507		67	SEG18	2218	
4	V_4	–2377		68	SEG19	2088	
5	V_5	–2246		69	SEG20	1957	
6	V_R	–2116	–2149	70	SEG21	1827	
7	V_{DD}	–1985	–2176	71	SEG22	1697	
8	V_{OUT}	–1857		72	SEG23	1567	
9	CAP2–	–1727		73	SEG24	1437	
10	CAP2+	–1522		74	SEG25	1307	
11	CAP1–	–1318		75	SEG26	1177	
12	CAP1+	–1113		76	SEG27	1046	
13	V_{SS}	–553	–2166	77	SEG28	916	
14	M/S	–356	–2185	78	SEG29	786	
15	SR2	–226		79	SEG30	656	
16	SR1	–95		80	SEG31	526	
17	WR	35		81	SEG32	396	
18	RD	165		82	SEG33	266	
19	CS2	295		83	SEG34	135	
20	CS1	425		84	SEG35	5	
21	A0	555		85	SEG36	–125	
22	FR	719		86	SEG37	–255	
23	CL	849		87	SEG38	–385	
24	D0	979		88	SEG39	–515	
25	D1	1109		89	SEG40	–646	
26	D2	1239		90	SEG41	–776	
27	D3	1369		91	SEG42	–906	
28	D4	1500		92	SEG43	–1036	
29	D5	1630		93	SEG44	–1166	
30	D6	1760		94	SEG45	–1296	
31	D7	1890		95	SEG46	–1426	
32	COM0 (COM16) [CMOS]	2069		96	SEG47	–1557	
33	COM1 (COM17) [COM0]	2199		97	SEG48	–1687	
34	COM2 (COM18) [COM1]	2329		98	SEG49	–1817	
35	COM3 (COM19) [COM2]	2459		99	SEG50	–1947	
36	COM4 (COM20) [COM3]	2589		100	SEG51	–2077	
37	COM5 (COM21) [COM4]	2719		101	SEG52	–2226	
38	COM6 (COM22) [COM5]	2802	–1654	102	SEG53	–2375	
39	COM7 (COM23) [COM6]		–1524	103	SEG54	–2802	1932
40	COM8 (COM24) [COM7]		–1393	104	SEG55		1802
41	COM9 (COM25) [COM8]		–1263	105	SEG56		1672
42	COM10 (COM26) [COM9]		–1133	106	SEG57		1541
43	COM11 (COM27) [COM10]		–1003	107	SEG58		1411
44	COM12 (COM28) [COM11]		–873	108	SEG59		1281
45	COM13 (COM29) [COM12]		–743	109	SEG60		1151
46	COM14 (COM30) [COM13]		–612	110	SEG61		1021
47	COM15 (COM31) [COM14]		–482	111	SEG62		891
48	COMS [COM15]		–352	112	SEG63		760
49	SEG0		–193	113	SEG64 (COM15)		599
50	SEG1		–63	114	SEG65 (COM14)		469
51	SEG2		67	115	SEG66 (COM13)		339
52	SEG3		197	116	SEG67 (COM12)		209
53	SEG4		327	117	SEG68 (COM11)		78
54	SEG5		457	118	SEG69 (COM10)		–52
55	SEG6		588	119	SEG70 (COM9)		–182
56	SEG7		718	120	SEG71 (COM8)		–312
57	SEG8		848	121	SEG72 (COM7)		–442
58	SEG9		978	122	SEG73 (COM6)		–572
59	SEG10		1108	123	SEG74 (COM5)		–703
60	SEG11		1238	124	SEG75 (COM4)		–833
61	SEG12		1368	125	SEG76 (COM3)		–963
62	SEG13		1499	126	SEG77 (COM2)		–1093
63	SEG14		1629	127	SEG78 (COM1)		–1223
64	SEG15		1759	128	SEG79 (COM0)		–1353

* Pin names in ( ) apply to SED1528.
* Pin names in [ ] apply to SED1526D$_A$* (CMOS pin = Type B).

■ ABSOLUTE MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Supply voltage range		V_{DD}	–0.3 to +7.0	V
	Triple voltage conversion	V_{DD}	–0.3 to +6.0	
Driver supply voltage range (1)		V_5	–18.0 to +0.3	V
Driver supply voltage range (2)		V_1, V_2, V_3, V_4	V5 to +0.3	V
Input voltage range		V_{IN}	–0.3 to V_{DD}+0.3	V
Output voltage range		V_0	–0.3 to V_{DD}+0.3	V
Allowable loss		P_D	250	mW
Operating temperature range		T_{OPR}	–40 to +85	°C
Storage temperature range	QFP • TCP	T_{STG}	–65 to +150	°C
	Bear chip		–55 to +125	
Soldering temperature and time		T_{SOLDER}	260/10 (at leads)	°C/sec



(Microprocessor side) (SED1526 series side)

Notes:
1. V_1 to V_5, V_{OUT}, and V_{REG} voltages are based on V_{DD}=0 V.
2. Voltages $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ must always be satisfied.
3. If an LSI exceeds its absolute maximum rating, it may be damaged permanently. It is desirable to use it under electrical characteristics conditions during general operation. Otherwise, an LSI malfunction or reduced LSI reliability may result.
4. The moisture resistance of the flat package may drop during soldering. Take care not to excessively heat the package resin during chip mounting.

■ ELECTRICAL CHARACTERISTICS

● DC Characteristics

(V_{DD} = 5 V ±10%, V_{SS} = 0 V, Ta = –40 to +85°C unless otherwise noted.)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Power voltage (1)	Operational	V_{DD}		2.4		6.0	V	V_{DD} *1
Operating voltage	Operational	V_5		–13.0		–4.0	V	V_5 *2
(2)	Operational	V_1, V_2		$0.6 \times V_5$		V_{DD}	V	V_1, V_2
	Operational	V_3, V_4		V_5		$0.4 \times V_5$	V	V_3, V_4
CMOS	High-level input voltage	V_{IHC}		$0.7 \times V_{DD}$		V_{DD}	V	*3
			V_{DD} = 2.7 V	$0.8 \times V_{DD}$		V_{DD}		
	Low-level input voltage	V_{ILC}		V_{SS}		$0.3 \times V_{DD}$	V	*3
			V_{DD} = 2.7 V	V_{SS}		$0.2 \times V_{DD}$		
	High-level output voltage	V_{OHC}	I_{OH} = –1 mA	$0.8 \times V_{DD}$		V_{DD}	V	*4
			V_{DD} = 2.7 V, I_{OH} = –0.5 mA	$0.8 \times V_{DD}$		V_{DD}		
	Low-level output voltage	V_{OLC}	I_{OH} = 1 mA	V_{SS}		$0.2 \times V_{DD}$	V	*4
			V_{DD} = 2.7 V, I_{OL} = 0.5 mA	V_{SS}		$0.2 \times V_{DD}$		
Schmitt	High-level input voltage	V_{IHS}		$0.4 \times V_{DD}$		$0.8 \times V_{DD}$	V	*5
			V_{DD} = 2.7 V	$0.4 \times V_{DD}$		$0.8 \times V_{DD}$		
	Low-level input voltage	V_{ILS}		$0.2 \times V_{DD}$		$0.6 \times V_{DD}$	V	*5
			V_{DD} = 2.7 V	$0.2 \times V_{DD}$		$0.6 \times V_{DD}$		
Input leakage current		I_{LI}		–1.0		1.0	µA	*6
Output leakage current		I_{LO}		–3.0		3.0	µA	*7
LCD driver ON resistance		R_{ON}	Ta = 25°C V_5 = –0.5 V		15.0	30.0	KΩ	SEG0 to 79 COS0 to 15 COMS *9
Static current consumption		I_{DDQ}	$\overline{CS}$ = C_L = V_{DD}		0.05	3.0	µA	V_{DD}
Input pin capacity		C_{IN}	Ta = 25°C, f = 1 MHz		5.0	8.0	pF	Input pins
CL output frequency		f_{CL}	Ta = 25°C, V_{DD} = 2.7 to 5 V	2.4	2.9	3.7	kHz	*8

● Dynamic current consumption (1) when the built-in power supply is OFF

(Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
SED1526	I_{DD} (1)	V_{DD} = 5.0V, V_5–V_{DD} = –6.0V	–	9.1	18	µA	*12
		V_{DD} = 3.0V, V_5–V_{DD} = –6.0V	–	12.0	24		
SED1528		V_{DD} = 5.0V, V_5–V_{DD} = –8.0V	–	7.5	15		
		V_{DD} = 3.0V, V_5–V_{DD} = –8.0V	–	9.5	19		

● Dynamic current consumption (2) when the built-in power supply is ON

Ta = 25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
SED1526	I_{DD} (2)	V_{DD} = 5.0V, V_5–V_{DD} = –6.0V, dual boosting	–	28	56	µA	*13
		V_{DD} = 3.0V, V_5–V_{DD} = –6.0V, triple boosting	–	52	104		
SED1528		V_{DD} = 5.0V, V_5–V_{DD} = –8.0V, dual boosting	–	29	58		
		V_{DD} = 3.0V, V_5–V_{DD} = –8.0V, triple boosting	–	48	96		

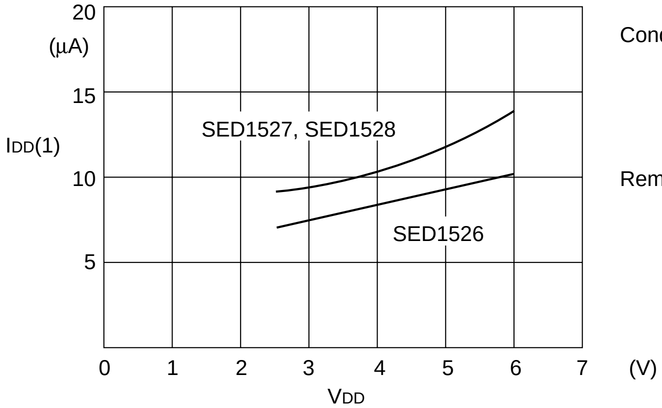
● Current consumption during Power Save mode V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V

Ta = 25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Power save mode	I_{DDS1}	SED1526, SED1528	—	3	6	µA	—

● Typical current consumption characteristics (reference data)

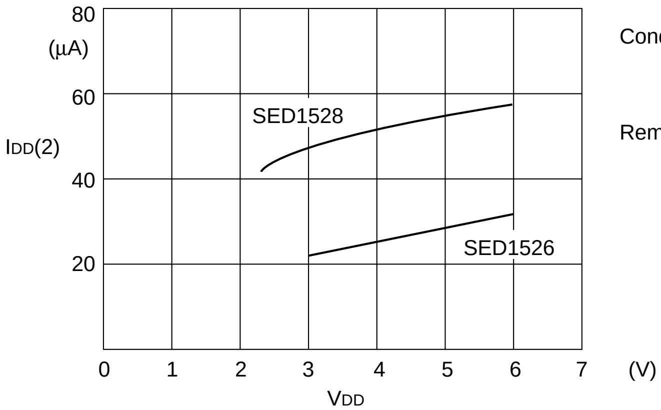
• Dynamic current consumption (1) when LCD external power mode lamp is ON



Conditions: The built-in power supply is OFF and an external power supply is used.
SED1526 V_5 -V_{DD} = –6.0V
SED1528 V_5 -V_{DD} = –8.0V

Remarks: *12

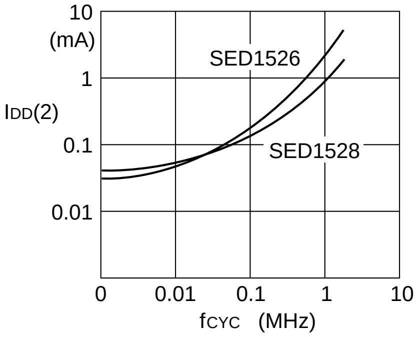
• Dynamic current consumption (2) when the LCD built-in power supply lamp is ON



Conditions: The built-in power supply is ON.
SED1526 V_5 -V_{DD} = –6.0V dual boosting
SED1528 V_5 -V_{DD} = –8.0V triple boosting

Remarks: *13

- Current consumption I_{DD} during access (2) during MPU access cycle



It shows the current consumption when a checker pattern is always written in f_{SYNC} timing. When not accessed, only the current consumption of I_{DD} (2) occurs.

Conditions: SED1526 V_5 -V_{DD} = –6.0V, dual boosting
SED1528 V_5 -V_{DD} = –8.0V, triple boosting
Ta = 25°C

	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Pins used
Built-in power circuit	Input voltage	V_{DD}	—	2.4	—	6.0	V	*10
	Booster output voltage	V_{OUT}	V_{DD} reference (during triple boosting)	–16.5	—	—	V	V_{OUT}
	Voltage regulator circuit operating voltage	V_{OUT}	V_{DD} reference	–16.5	—	–4.0	V	V_{OUT}
	Voltage follower operating voltage	V_5	V_{DD} reference	–13.0	—	–4.0	V	*11
	Reference voltage	V_{REG}	V_{DD} reference Ta = 25°C	–3.5	–3.1	–2.7	V	V_R

* See notes below.

*1 Although the wide range of operating voltage is guaranteed, a spike voltage change during access to the MPU is not guaranteed.
*2 The operating voltage range of the V_{DD} and V_5 systems (See Figure 9.)
The operating voltage range is applied if an external power supply is used.
*3 Pins D0 to D5, A0, CS1, CS2, RD (E), WR (R/W), M/S, CL, and FR
*4 Pins D0 to D7, FR, and CL
*5 Pins SI (D7), SCL (D6), SR1, and SR2
*6 Pins A0, RD (E), WR (R/W), CS1, CS2, M/S, SR1, and SR2
*7 Applied if pins D0 to D7, FR, and CL are high impedance.
*8 For the relationship between CL output frequency and frames, see Figure 7.
For the relationship between CL output frequency and power voltage, see Figure 8.
For the relationship between CL output frequency and temperature, see Figure 11.
*9 The resistance when the 0.1-volt voltage is applied between the SEG and COM output terminals and each power terminal (V_1, V_2, V_3 or V_4). It must be within operating voltage (2).

$$R_{ON} = 0.1\ V/\Delta I$$

where, ΔI is the current that flows between power supply and SEG or COM terminal when the 0.1-volt voltage is applied.
*10 If the triple voltage by the built-in power circuit are used the V_{DD} primary power must be used within the input voltage range.
*11 The V_5 voltage can be adjusted within the voltage follower operating range by use of voltage regulator.
*12 Applied if the built-in oscillation circuit is used and if not accessed by the MPU.
*13 Applied if the built-in oscillation circuit and the built-in power circuit are used, and if not accessed by the MPU.
The current flowing through the voltage regulator resistors (R1, R2 and R3) is not included.
When the built-in voltage booster is used, the current consumption for the V_{DD} power supply is shown.

- Relationship between CL output frequency and frames (SED 1526 series)

The relationship between CL output frequency (f_{CL}) and frame frequency (f_F) can be determined as follows:

	Duty	f_F
SED1526	1/9 1/17	8 • f_{CL}/288 8 • f_{CL}/272
SED1528	1/33	8 • f_{CL}/264

Figure 7

("f_F" indicates the LCD current alternating cycle, but not the cycle of f F signals.)

- Relationship between CL output frequency and power voltage

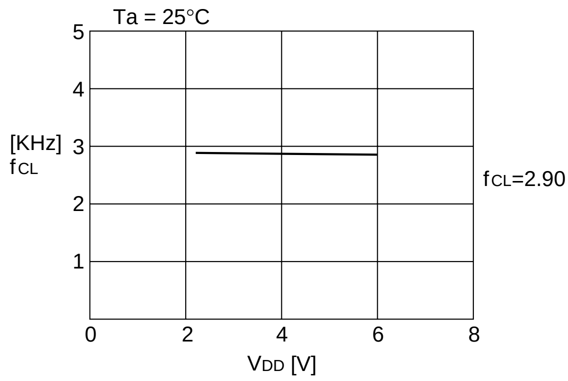
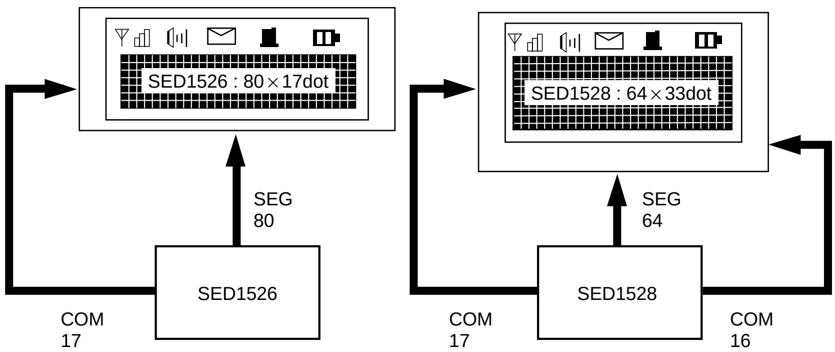


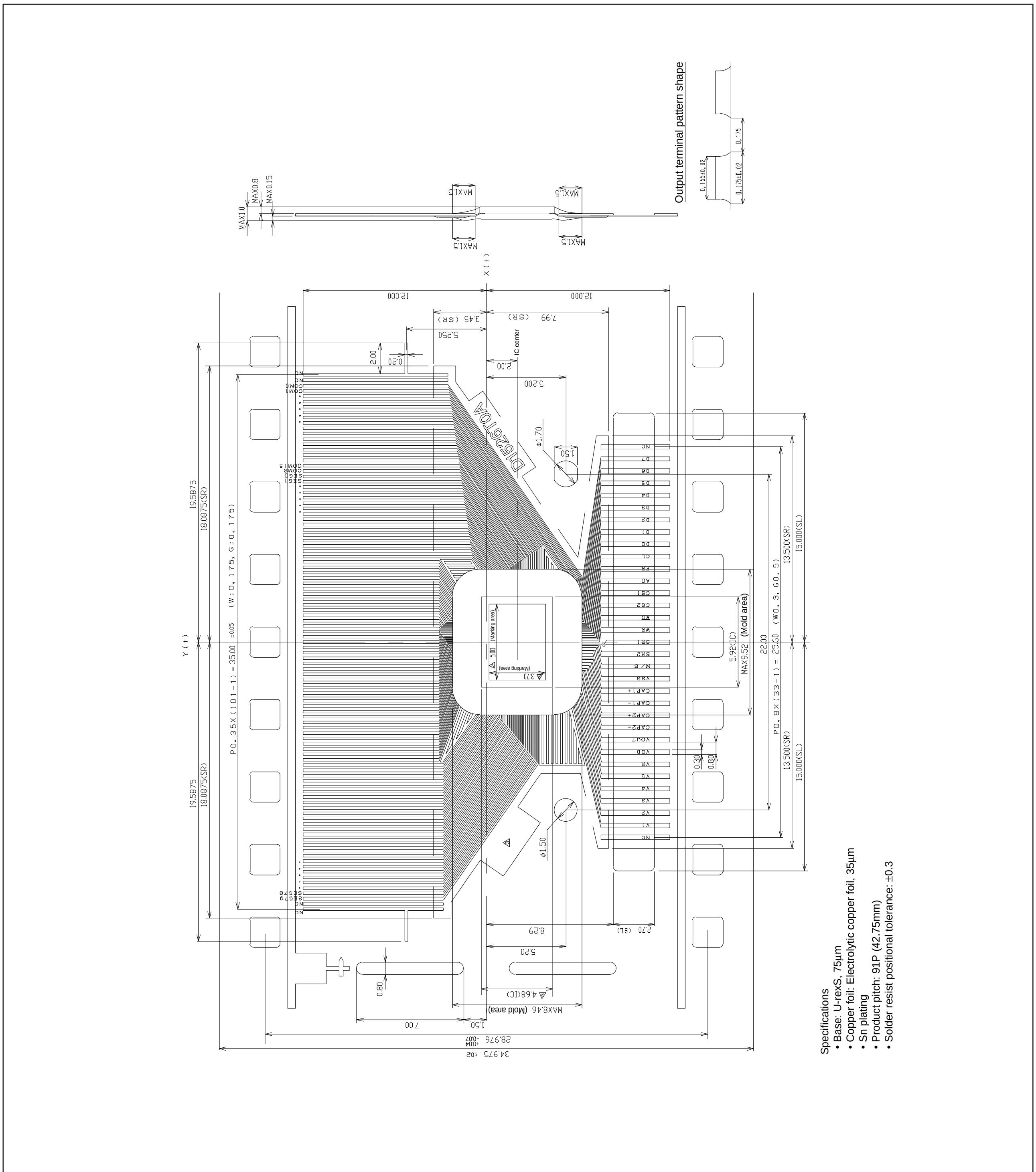
Figure 7

● LCD Panel and Wiring Examples

- Single-chip configuration

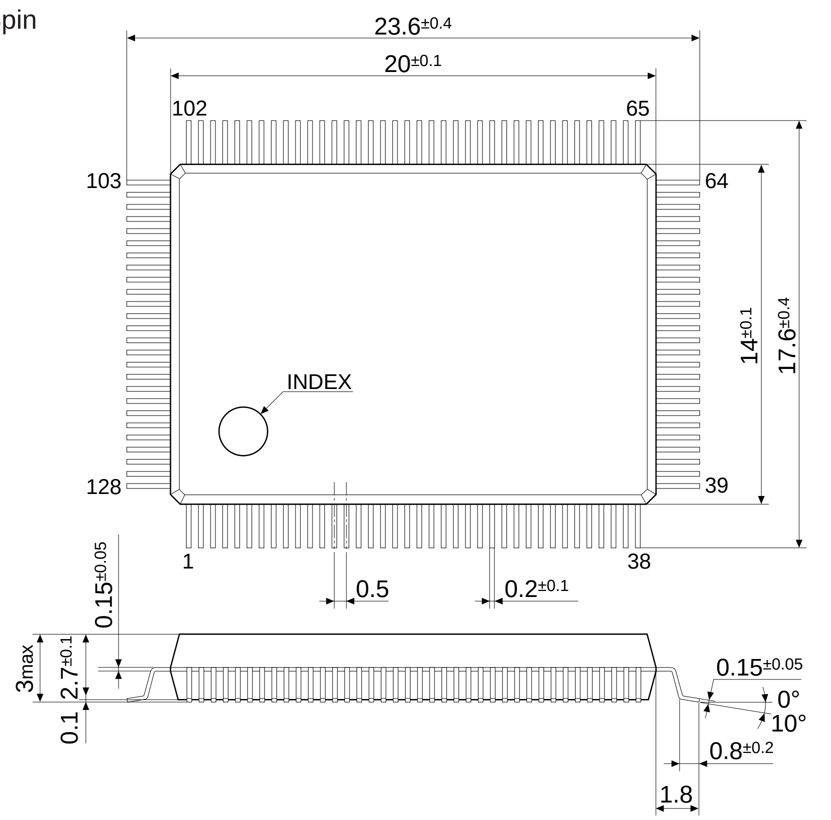


● **TPC shape SED1526T0A (Reference drawing)**



This dimensional outline drawing is subject to change for improvements without prior notice.

PACKAGE DIMENSIONS



The package dimensions are subject to change without notice.

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First issue Dec., 1996 Ⓗ
Printed Nov. 1996 in Japan