SED1560/1/2
Technical Manual
(Preliminary)

S-MOS Systems, Inc.
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Version 3.0 (Preliminary)

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Overview

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1.1 DESCRIPTION

The SED1560 Series are intelligent CMOS LCD driver-controllers with the ability to drive alphanumeric and graphic displays. The SED1560 Series communicates with a high-speed microprocessor, such as the Intel 80XX family or the Motorola 68XX family, through either a serial or an 8-bit parallel interface. It stores the data sent from the microprocessor in the built-in display data RAM (166 × 65 bits) and generates an LCD drive signal. These devices incorporate an internal DC/DC converter to generate the negative voltage needed for LCD contrast. The controllers feature software contrast adjustment by command setting.

The three different versions of the SED1560 Series support the following duty ratios and display sizes:

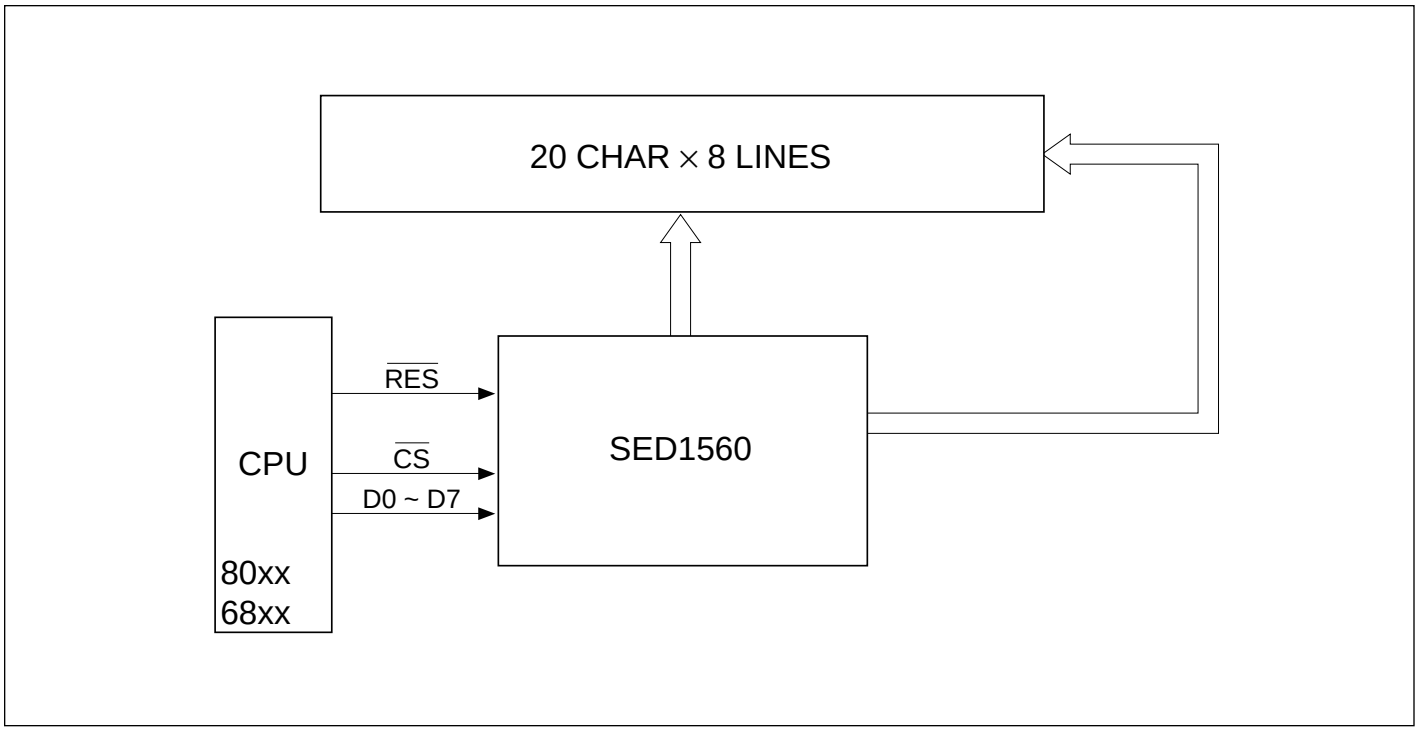
Model	Duty Ratio	SEG × COM
SED1560	1/65, 1/64, 1/49, 1/48	102 × 65
SED1561	1/33, 1/32, 1/25, 1/24	134 × 33
SED1562	1/17, 1/16	150 × 17

1.2 FEATURES

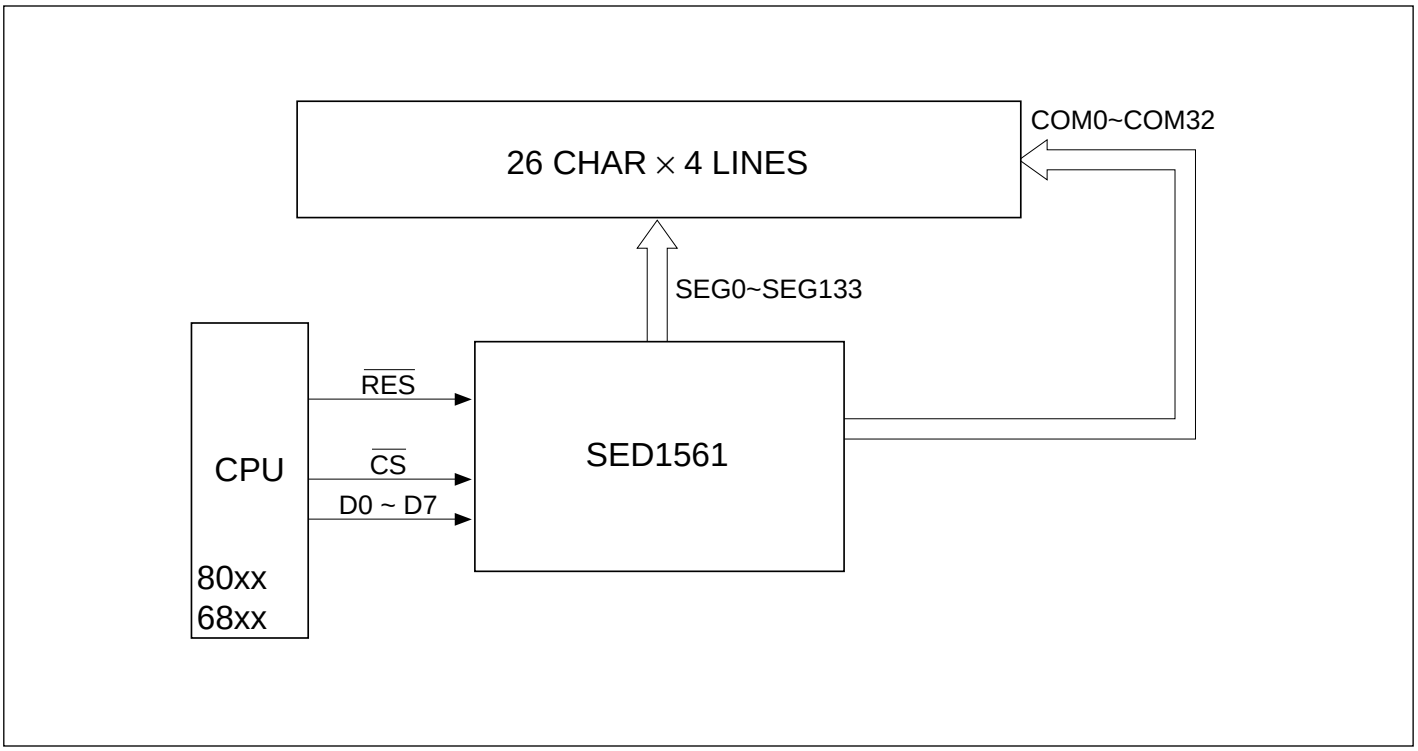
- Low-power operation: 8 μA @ 1 kHz, 6V LCD
- 350 μA current consumption during CPU access @ 200 kHz
- Direct interface to both 80XX and 68XX, 5 MHz, zero wait-state
- On-chip display data RAM (166 × 65 bits)
- On-chip DC/DC converter for LCD voltage
- On-chip voltage regulator and low-power voltage follower
- –.17% / °C temperature gradient
- On-chip oscillator with external resistor
- 32 levels of contrast adjustment by software
- Supports master/slave operation
- Selectable output configuration
- 2.4V to 6.0V supply voltage
- 3.5V to 16V LCD voltage
- Package:

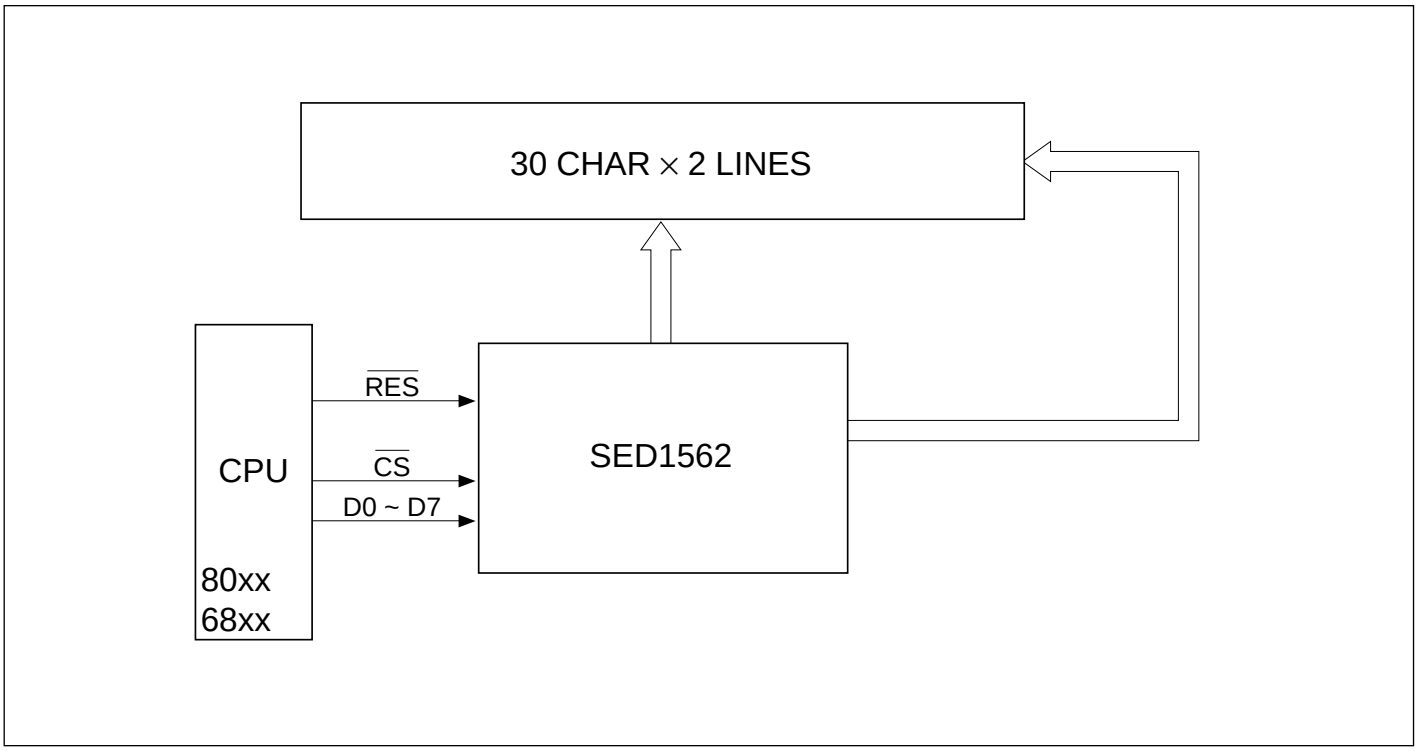
TAB 2 side	T0B
TAB 4 side	TQA
Al pad	D*A
Au bump	D*B
BGA 225 pad	B0A

1.3 SYSTEM BLOCK DIAGRAMS

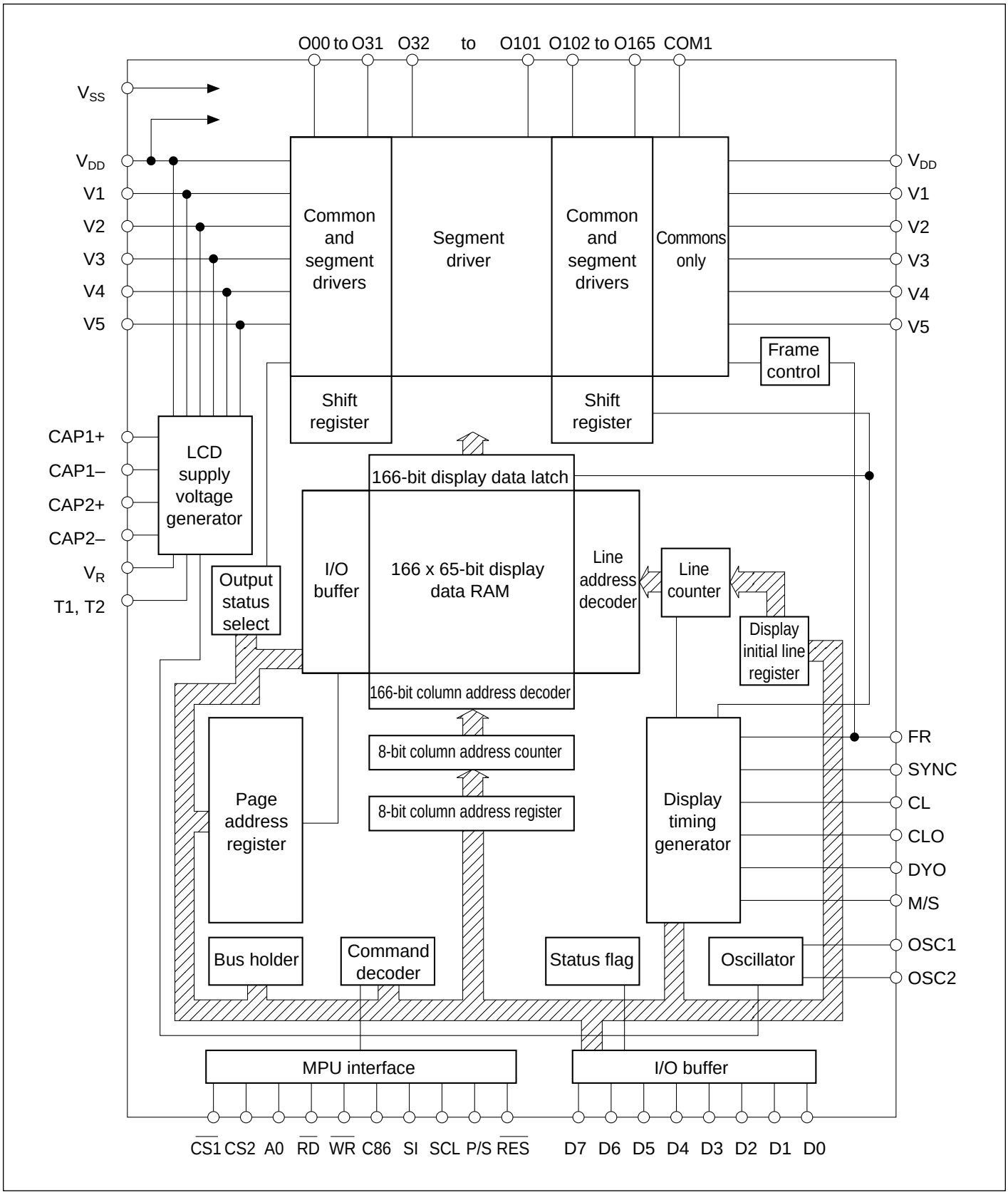


1.3 SYSTEM BLOCK DIAGRAMS (cont.)





1.4 BLOCK DIAGRAM



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2.0
Pin Description

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2.1 POWER SUPPLY

Number of Pins	I/O	Name	Description
2	Supply	V_{DD}	Common to MPU power supply pin V_{CC}
2	Supply	V_{SS}	Ground
11	Supply LCD voltage	V1 to V5	LCD driver supply voltages. The voltage determined by the LCD cell is impedance-converted by a resistive divider or an operational amplifier for application. Voltage levels are based on V_{DD}. The voltages must satisfy the following relationship: $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$ Master mode select: bias voltages are generated on-chip.

	SED1560	SED1561	SED1562
V1	1/9 V5	1/7 V5	1/5 V5
V2	2/9 V5	2/7 V5	2/5 V5
V3	7/9 V5	5/7 V5	3/5 V5
V4	8/9 V5	6/7 V5	4/5 V5

2.2 LCD DRIVER POWER SUPPLIES

Number of Pins	I/O	Name	Description
1	O	CAP1+	DC/DC voltage converter capacitor 1 positive connection
1	O	CAP1–	DC/DC voltage converter capacitor 1 negative connection
1	O	CAP2+	DC/DC voltage converter capacitor 2 positive connection
1	O	CAP2–	DC/DC voltage converter capacitor 2 negative connection
1	O	V_{OUT}	DC/DC voltage converter output
1	I	V_R	Voltage adjustment pin. Applies voltage between V_{DD} and V5 using a resistive divider.
2	I	T1, T2	Liquid crystal power control terminals

T1	T2	Boosting Circuit	Voltage Regulation Circuit	V/F Circuit
L	L	Valid	Valid	Valid
L	H	Valid	Valid	Valid*
H	L	Invalid	Valid	Valid
H	H	Invalid	Invalid	Valid

* V/F circuit current capacity enhancement

2.3 MICROPROCESSOR INTERFACE

<table>
<tr><th>Number of Pins</th><th>I/O</th><th>Name</th><th>Description</th></tr>
<tr><td>8</td><td>I/O</td><td>D0 to D7</td><td>Data is transferred between the controller and MPU via these pins</td></tr>
<tr><td>1</td><td>I</td><td>A0</td><td>Control/display data flag input. This is connected to the LSB of the microprocessor address bus.
• When LOW, the data on D0 to D7 is command data
• When HIGH, the data on D0 to D7 is display data</td></tr>
<tr><td>1</td><td>I</td><td>$\overline{RES}$</td><td>Reset input. Setting this pin low initializes the SED156X.</td></tr>
<tr><td>2</td><td>I</td><td>$\overline{CS1}$, CS2</td><td>Chip select inputs. Data input/output is enabled when $\overline{CS1}$ is LOW and CS2 is HIGH.</td></tr>
<tr><td>1</td><td>I</td><td>$\overline{RD}$</td><td>Read enable input. See note 1.</td></tr>
<tr><td>1</td><td>I</td><td>$\overline{WR}$</td><td>Write enable input. See note 2.</td></tr>
<tr><td>1</td><td>I</td><td>C86</td><td>Microprocessor interface select input.
• LOW when interfacing to 8080-series
• HIGH when interfacing to 6800-series</td></tr>
<tr><td>1</td><td>I</td><td>SI</td><td>Serial data input</td></tr>
<tr><td>1</td><td>I</td><td>SCL</td><td>Serial clock input. Data is read on the rising edge of SCL and converted to 8-bit parallel data.</td></tr>
<tr><td>1</td><td>I</td><td>P/S</td><td>Parallel/serial data input select
<table>
<tr><th>P/S</th><th>Operating Mode</th><th>Chip Select</th><th>Data/ com-mand</th><th>Data I/O</th><th>Read/ write</th><th>Serial Clock</th></tr>
<tr><td>HIGH</td><td>Parallel</td><td>$\overline{CS1}$, CS2</td><td>A0</td><td>D0 to D7</td><td>$\overline{RD}$, $\overline{WR}$</td><td>—</td></tr>
<tr><td>LOW</td><td>Serial</td><td>$\overline{CS1}$, CS2</td><td>A0</td><td>SI</td><td>Write only</td><td>SCL</td></tr>
</table>
In serial mode, data cannot be read from the RAM, and D0 to D7, HZ, $\overline{RD}$ and $\overline{WR}$ must be HIGH or LOW. In parallel mode, SI and SCL must be HIGH or LOW.</td></tr>
</table>

Notes:

1. When interfacing to 8080-series microprocessors, $\overline{RD}$ is active-LOW. When interfacing to 6800-series microprocessors, they are active-HIGH.
2. When interfacing to 8080-series microprocessors, $\overline{WR}$ is active-LOW. When interfacing to 6800-series microprocessors, read mode is selected when $\overline{WR}$ is HIGH, and write mode is selected when $\overline{WR}$ is LOW.

2.4 OSCILLATOR AND DISPLAY TIMING CONTROL

<table>
<tr><th>Number of Pins</th><th>I/O</th><th>Name</th><th>Description</th></tr>
<tr><td>2</td><td>I</td><td>OSC1</td><td>Using internal oscillator when M/S = “H”, connect resistor R_f to the OSC1 and OSC2 pins. The OSC2 pin is used for output of the oscillator amplifier.</td></tr>
<tr><td>2</td><td>I/O</td><td>OSC2</td><td>When M/S = “L”: the OSC2 pin is used for input of oscillation signal. The OSC1 pin should be left open. Fix the C_L pin to the V_{SS} level when using the internal oscillator circuit as the display clock.</td></tr>
<tr><td>1</td><td>I</td><td>C_L</td><td>Display clock input. The line counter increments on the rising edge of C_L, and the display pattern is output on the falling edge. When using the external display clock, OSC1 = “H”, OSC2 = “L”, and reset this LSI by $\overline{RES}$ pin.</td></tr>
<tr><td>1</td><td>O</td><td>C_{LO}</td><td>Display clock output. When using the internal oscillator, the clock signal is output on this pin. Connect C_{LO} to YSCL on the common driver.</td></tr>
<tr><td>1</td><td>I</td><td>M/S</td><td>Master/slave select input. Master produces signals for display, and slave receives them. This is for display synchronization.
<table>
<tr><th>Device</th><th>M/S</th><th>Operating Mode</th><th>Internal Oscillator</th><th>Power Supply</th><th>FR</th><th>SYNC</th><th>OSC1</th><th>OSC2</th><th>DYO</th></tr>
<tr><td rowspan="2">156X</td><td>LOW</td><td>Slave</td><td>OFF</td><td>OFF</td><td>I</td><td>I</td><td>Open</td><td>I</td><td>O</td></tr>
<tr><td>HIGH</td><td>Master</td><td>ON</td><td>ON</td><td>O</td><td>O</td><td>I</td><td>O</td><td>O</td></tr>
</table>
Note:
I = input mode
O = output mode</td></tr>
<tr><td>1</td><td>I/O</td><td>FR</td><td>LCD AC drive signal input/output. Output is selected when M/S is HIGH, and input is selected when M/S is LOW.</td></tr>
<tr><td>1</td><td>I/O</td><td>SYNC</td><td>Display sync input/output. Output is selected when M/S is HIGH, and input is selected when M/S is LOW.</td></tr>
<tr><td>1</td><td>O</td><td>DYO</td><td>Start-up output for common driver. Connect to DIO of the common driver, such as the SED1630.</td></tr>
</table>

* SED1630 has a DIO input.

2.5 LCD DRIVER OUTPUTS

<table>
<tr><th>Number of Pins</th><th>I/O</th><th>Name</th><th>Description</th></tr>
<tr><td>166</td><td>O</td><td>O0 to O165</td><td>LCD driver outputs. O0 to O31 and O102 to O165 are selectable segment or common outputs, determined by a selection command. O32 to O101 are segment outputs only.
For segment outputs, the ON voltage level is given as shown in the following table:
<table>
<tr><th rowspan="2">RAM Data</th><th rowspan="2">FR</th><th colspan="2">LCD ON Voltage</th></tr>
<tr><th>Normal Display</th><th>Inverse Display</th></tr>
<tr><td rowspan="2">LOW</td><td>LOW</td><td>V3</td><td>V5</td></tr>
<tr><td>HIGH</td><td>V2</td><td>V_{DD}</td></tr>
<tr><td rowspan="2">HIGH</td><td>LOW</td><td>V5</td><td>V3</td></tr>
<tr><td>HIGH</td><td>V_{DD}</td><td>V2</td></tr>
</table>
For common outputs, the ON voltage is given as shown in the following table:
<table>
<tr><th>Scan Data</th><th>FR</th><th>LCD ON Voltage</th></tr>
<tr><td rowspan="2">LOW</td><td>LOW</td><td>V4</td></tr>
<tr><td>HIGH</td><td>V1</td></tr>
<tr><td rowspan="2">HIGH</td><td>LOW</td><td>V_{DD}</td></tr>
<tr><td>HIGH</td><td>V5</td></tr>
</table></td></tr>
<tr><td>1</td><td>O</td><td>COM1</td><td>LCD driver common output. Common outputs when the “DUTY + 1” command is executed are as follows:
<table>
<tr><th>Device</th><th>“DUTY + 1” ON</th><th>“DUTY + 1” OFF</th></tr>
<tr><td>SED1560</td><td>COM64, COM48</td><td>V1 or V4</td></tr>
<tr><td>SED1561</td><td>COM32, COM24</td><td>V1 or V4</td></tr>
<tr><td>SED1562</td><td>COM16</td><td>V1 or V4</td></tr>
</table>
Common output special for the indicator.</td></tr>
</table>

3.0

Electrical Characteristics

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3.1 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{SS}	–7.0 to 0.03	V
		–6.0 to 0.3 (when triple voltage conversion)	
Driver supply voltage range (1)	V5	–18.0 to 0.3	V
Driver supply voltage range (2)	V1, V2, V3, V4	V5 to 0.3	V
Input voltage range	V_{IN}	V_{SS}–0.3 to 0.3	V
Output voltage range	V0	V_{SS}–0.3 to 0.3	V
Operating temperature range	T_{opr}	–30 to 85	°C
Storage temperature range (TCP)	T_{str}	–55 to 125	°C

Notes:

1. The voltages shown are based on V_{DD} = 0V.
2. Always keep the condition $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$ for voltages V1, V2, V3 and V4.
3. If devices are used over the absolute maximum rating, the LSIs may be destroyed permanently. It is desirable to use them under the electrical characteristic conditions for general operation. Otherwise, a malfunction of the LSI may be caused and LSI reliability may be affected.
4. For operating temperatures below –30°C, please consult an S-MOS engineer.

3.2 DC CHARACTERISTICS

V_{DD} = 0V, V_{SS} = –5 ± 10%, T_a = –30 to +85°C unless otherwise noted.

Parameter		Symbol	Condition		Min	Typ	Max	Unit	Applicable Pin
Power voltage (1)	Recommended operation	V_{SS}			–5.5	–5.0	–4.5	V	V_{SS}
	Operational				–6.0	—	–2.4		V_{SS} *1
Operating voltage (2)	Operational	V5			–16.0	—	–3.5	V	V5 *2
	Operational	V1, V2			0.4 × V5	—	V_{DD}	V	V1, V2
	Operational	V3, V4			V5	—	0.6 × V5	V	V3, V4
High-level input voltage		V_{IHC1}			0.3 × V_{SS}	—	V_{DD}	V	*3
		V_{IHC2}			0.15 × V_{SS}	—	V_{DD}	V	*4
		V_{IHC1}	V_{SS} = –2.7V		0.2 × V_{SS}	—	V_{DD}	V	*3
		V_{IHC2}	V_{SS} = –2.7V		0.15 × V_{SS}	—	V_{DD}	V	*4
Low-level input voltage		V_{ILC1}			V_{SS}	—	0.7 × V_{SS}	V	*3
		V_{ILC2}			V_{SS}	—	0.85 × V_{SS}	V	*4
		V_{ILC1}	V_{SS} = –2.7V		V_{SS}	—	0.8 × V_{SS}	V	*3
		V_{ILC2}	V_{SS} = –2.7V		V_{SS}	—	0.85 × V_{SS}	V	*4
High-level output voltage		V_{OHC1}		I_{OH} = –1 mA	0.2 × V_{SS}	—	V_{DD}	V	*5 OSC2
		V_{OHC2}		I_{OH} = –120 µA	0.2 × V_{SS}	—	V_{DD}		
		V_{OHC1}	V_{SS} = –2.7V	I_{OH} = –0.5 mA	0.2 × V_{SS}	—	V_{DD}	V	*5 OSC2
		V_{OHC2}	V_{SS} = –2.7V	I_{OH} = –50 µA	0.2 × V_{SS}	—	V_{DD}		
Low-level output voltage		V_{OLC1}		I_{OL} = 1 mA	V_{SS}	—	0.8 × V_{SS}	V	*5 OSC2
		V_{OLC2}		I_{OL} = 120 µA	V_{SS}	—	0.8 × V_{SS}		
		V_{OLC1}	V_{SS} = –2.7V	I_{OL} = 0.5 mA	V_{SS}	—	0.8 × V_{SS}	V	*5 OSC2
		V_{OLC2}	V_{SS} = –2.7V	I_{OL} = 50 µA	V_{SS}	—	0.8 × V_{SS}		
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS}		–1.0	—	1.0	µA	*6
Output leakage current		I_{LO}			–3.0	—	3.0	µA	*7
LCD driver ON resistance		R_{ON}	T_a = 25°C	V5 = –14.0V	—	2.0	3.0	kΩ	O0 ~ O166 *8
				V5 = –8.0V	—	3.0	4.5		
Static power consumption		I_{SSQ}			—	0.00	5.0	µA	V_{SS}
		I_{5Q}	V5 = –18.0V		—	0.01	15.0	µA	V5
Input terminal capacity		C_{IN}	T_a = 25°C	f = 1 MHz	—	5.0	8.0	pF	*3 *4
Oscillator frequency		f_{OSC}	R_f = 1 MΩ ±2%	V_{SS} = –5V	15	18	22	kHz	*9
				V_{SS} = –2.7V	11	16	21		

Reset time	t_R		1.0	—	—	µs	*10
Reset “L” pulse width	t_{RW}		10	—	—	µs	*11

(continued)

(continued) V_{DD} = 0V, V_{SS} = –5 ± 10%, T_a = –30 to +85°C unless otherwise noted.

	Parameter	Symbol	Condition	Min	Typ	Max	Unit	Applicable Pin
Built-in power circuit	Input voltage	V_{SS}		–6.0	—	–2.4	V	*12
	Amplified output voltage	V_{OUT}	If amplified 3 times	–18.0	—	—	V	V_{OUT}
	Voltage regulator circuit operation voltage	V_{OUT}		–18.0	—	–6.0	V	V_{OUT}
	Voltage follower operation voltage	V5 ①	Supplied to SED1560	–16.0	—	–6.0	V	*13
		V5 ②	Supplied to SED1561	–16.0	—	–5.0	V	
		V5 ③	Supplied to SED1562	–16.0	—	–4.5	V	
	Reference voltage	V_{REG}	T_a = 25°C	–2.35	–2.5	–2.65	V	

Notes: * See Notes on page 22.

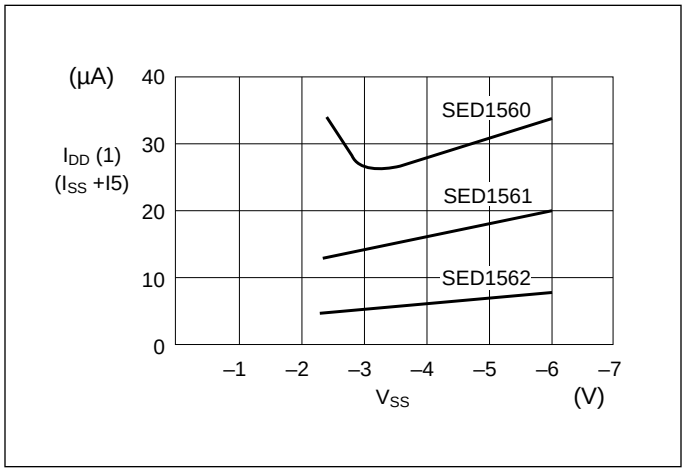
When dynamic current consumption (I) is displayed; the built-in power supply is on and T1 = T2 = Low.

Test conditions, unless otherwise specified: V_{DD} = 0V, V_{SS} = –5V ±10%, T_a = –30 to 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Remarks
SED1560	I_{DD} (1)	V5 = –12.5V; 3 times amplified		169	340	µA	*16
SED1561		V5 = –8.0V; 3 times amplified		124	250	µA	
SED1562		V5 = –6.0V; 2 times amplified		53	110	µA	
		V_{SS} = –2.7V; 3 times amplified V5 = –6.0V		66	130	µA	

Typical current consumption characteristics

● **Dynamic current consumption (I), if an external clock and an external power supply are used.**



Conditions: The built-in power supply is off but the external one is used.

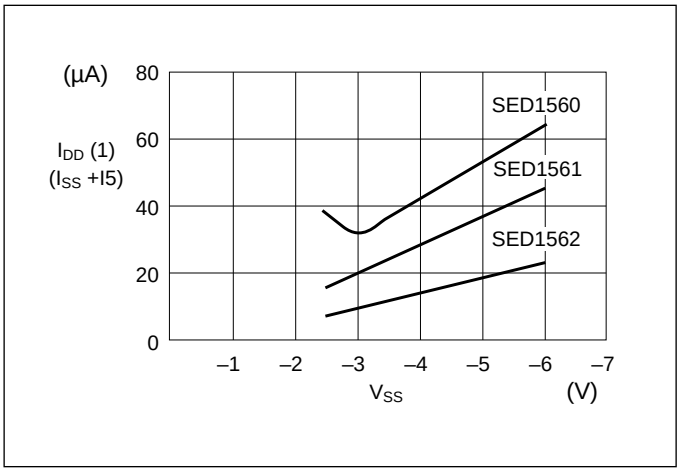
SED1560 ..... V5 = –12.5V
SED1561 ..... V5 = –8.0V
SED1562 ..... V5 = –6.0V

External clock:

SED1560 ..... f_{CL} = 4 kHz
SED1561 ..... f_{CL} = 2 kHz
SED1562 ..... f_{CL} = 1 kHz

Remarks: *14

● Dynamic current consumption (I), if the built-in oscillator and the external power supply are used.



Conditions: The built-in power supply is off but the external one is used.

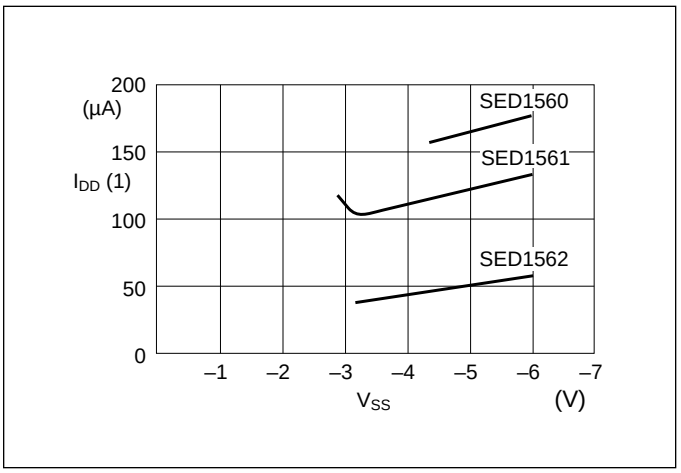
SED1560 ..... V5 = –12.5V
SED1561 ..... V5 = –8.0V
SED1562 ..... V5 = –6.0V

Internal oscillation:

SED1560 ..... Rf = 1 MΩ
SED1561 ..... Rf = 1 MΩ
SED1562 ..... Rf = 1 MΩ

Remarks: *15

● Dynamic current consumption (I), if the built-in power supply is used.



Conditions: The built-in power supply is on and T1 = T2 = Low.

SED1560 ..... V5 = –12.5V; 3 times amplified

SED1561 ..... V5 = –8.0V; 3 times amplified

SED1562 ..... V5 = –6.0V; 2 times amplified

Internal oscillation:

SED1560 ..... Rf = 1 MΩ
SED1561 ..... Rf = 1 MΩ
SED1562 ..... Rf = 1 MΩ

Remarks: *16

Notes:

*1. A wide range of operating voltage is possible, but considerable voltage variation during MPU access is not guaranteed.

*2. The operating voltage range of the V_{SS} and V5 systems (see Figure 3.3). The operating voltage range is applied if an external power supply is used.

*3. Pins A0, D0 to D7, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, FR, SYNC, M/S, C86, SI, P/S, T1 AND T2.

*4. Pins CL, SCL, and $\overline{RES}$.

*5. Pins D0 to D7, FR, SYNC, CL0, and DY0

*6. Pins A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CL, M/S, $\overline{RES}$, C86, SI, SCL, P/S, T1, and T2.

*7. Applied if pins D0 to D7, FR, and SYNC are high impedance.

*8. The resistance when the 0.1 -volt voltage is applied between the "On" output terminal and each power terminal (V1, V2, V3 or V4). It must be within the operating voltage (2).

*9. The relationship between the oscillation frequency, frame and Rf value (see Figure 3.2).

10. "tr" (reset time) indicates the period between the time when the $\overline{RES}$ signal rises and when the internal circuit has been reset. Therefore, the SED156 is usually operable after "tr" time.

*11. Specifies the minimum pulse width of RES signal. The Low pulse greater than "t_{RW}" must be entered for reset.

*12. If the voltage is amplified three times by the built-in power circuit, the primary power V_{SS} must be used within the input voltage range.

*13. The V5 voltage can be adjusted within the voltage follower operating range by the voltage regulator circuit.

*14, 15, 16. Indicates the current consumed by the separate IC. The current consumption due to the LCD panel capacity and wiring capacity is not included.

The current consumption is shown if the checker is used, the display is turned on, the output status of Case 6 is selected, and the SED1560 is set to 1/64 duty, the SED1561 is set to 1/32 duty, and the SED1562 is set to 1/64 duty.

*14. Applied if an external clock is used and if not accessed by the MPU.

*15. Applied if the built-in oscillation circuit is used and if not accessed by the MPU.

*16. Applied if the built-in oscillation circuit and the built-in power circuit are used (T1 = T2 = Low) and if not accessed by the MPU.

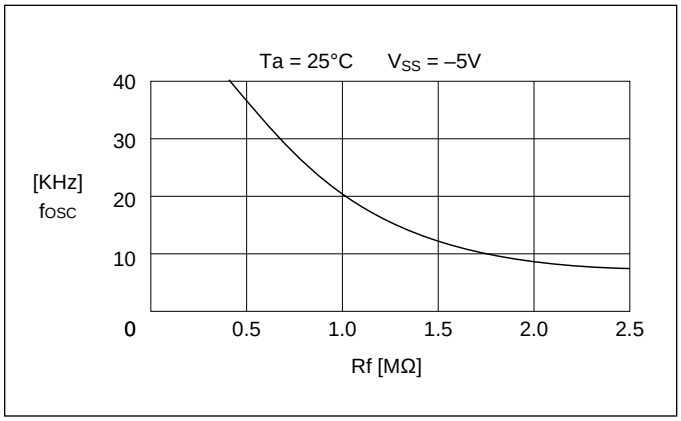


Figure 3.1
Oscillator frequency vs. frame vs. Rf
[SED1560 Series]

The relationship between oscillator frequency fOSC and LCD frame frequency fF is obtained from the following expression:

Table 3.1

Device	Duty	fF
SED1560	1/64	fOSC/256
	1/48	fOSC/192
SED1561	1/32	fOSC/256
	1/24	fOSC/192
SED1562	1/16	fOSC/256

(fF indicates not fF signal cycle but cycle of LCD AC.)

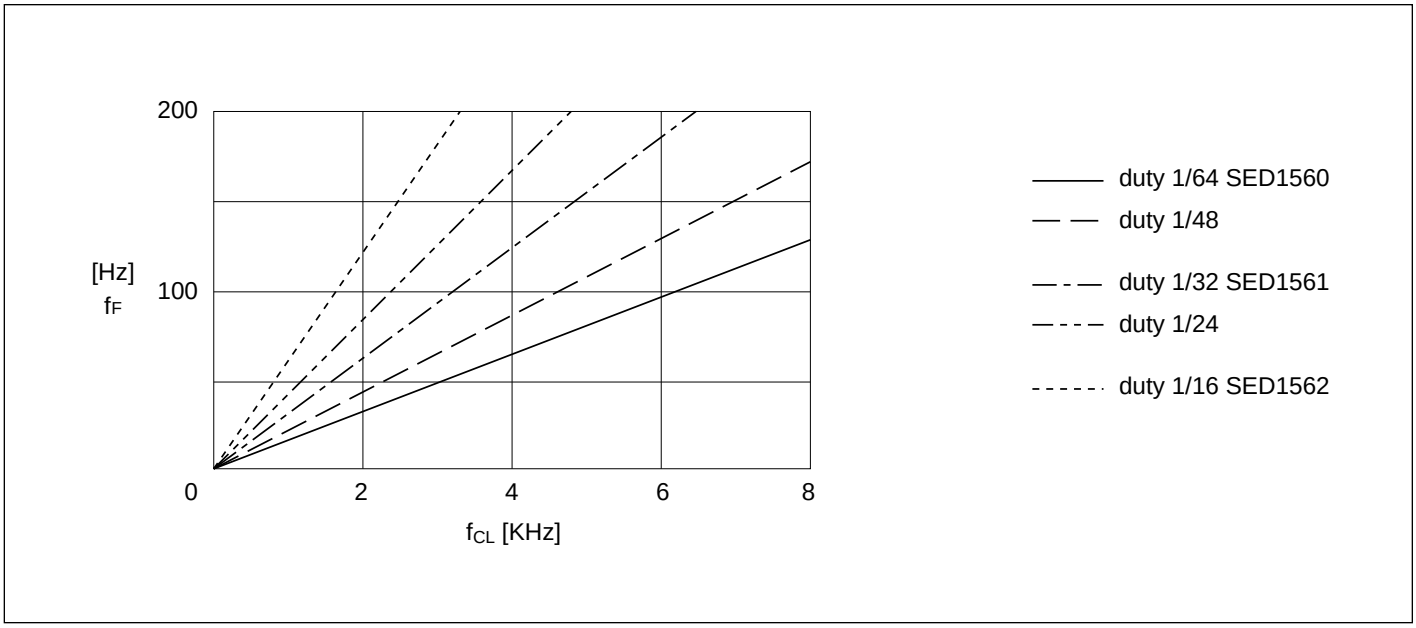


Figure 3.2 External clock (fCL) vs. frame frequency [SED1560 Series]

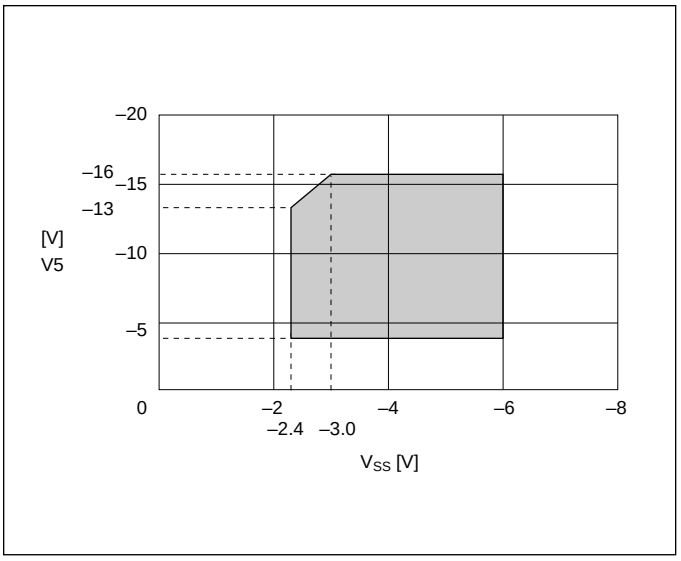


Figure 3.3
Operating voltage range for VSS and V5

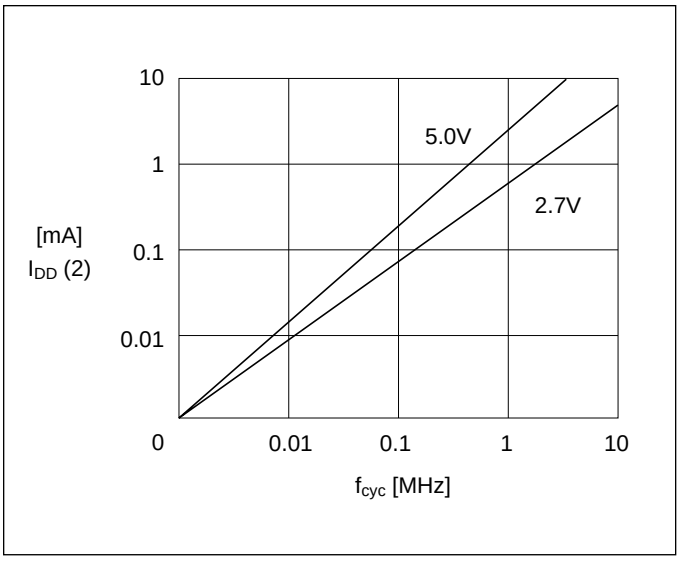


Figure 3.4
Power consumption during CPU access cycle (IDD [2])

3.3 AC CHARACTERISTICS

3.3.1 Reset

Table 3.5 Reset

Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Reset time	t_R	t_R is measured from the rising edge of $\overline{RES}$. The SED156X resumes normal operating mode after a reset.	1.0	—	—	µs
Reset LOW-level pulsewidth	t_{RW}		1.0	—	—	µs

3.4 DISPLAY CONTROL TIMING

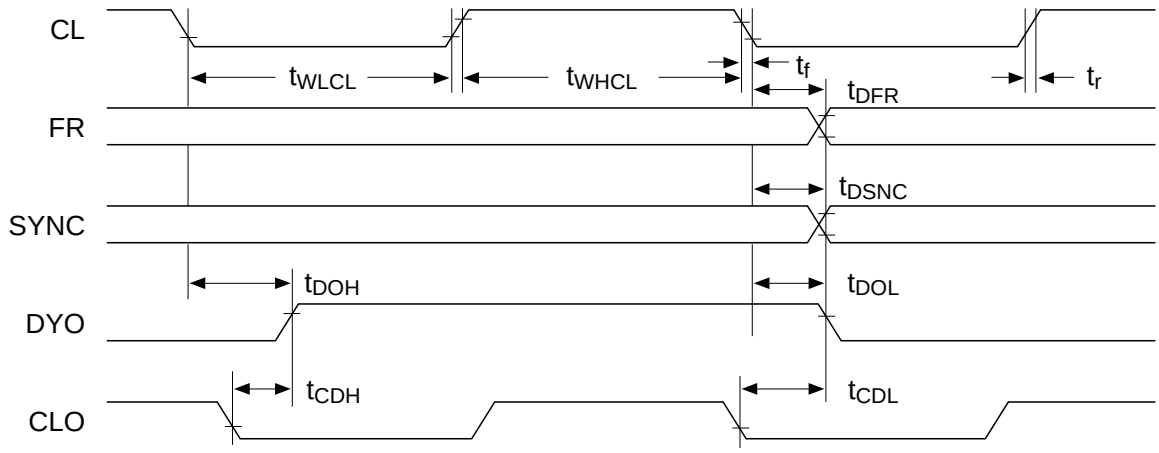


Figure 3.5 Display control timing

Display Control Input Timing

V_{SS} = –5.5 to –4.5V, T_a = –30 to 85°C

Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
CL LOW-level pulsewidth	t_{WLCL}		35	—	—	µs
CL HIGH-level pulsewidth	t_{WHCL}		35	—	—	µs
CL rise time	t_r		—	30	—	ns
CL fall time	t_f		—	30	—	ns
FR delay time	t_{DFR}		–1.0	—	1.0	µs
SYNC delay time	t_{DSNC}		–1.0	—	1.0	µs

V_{SS} = –4.5 to –2.7V, T_a = –30 to 85°C

Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
CL LOW-level pulsewidth	t_{WLCL}		35	—	—	µs
CL HIGH-level pulsewidth	t_{WHCL}		35	—	—	µs
CL rise time	t_r		—	40	—	ns
CL fall time	t_f		—	40	—	ns
FR delay time	t_{DFR}		–1.0	—	1.0	µs
SYNC delay time	t_{DSNC}		–1.0	—	1.0	µs

1. Effective only when the SED156X is in the master mode.
2. The FR/SYNC delay time input timing is provided in the slave operation. The FR/SYNC delay time output timing is provided in the master operation.
3. Each timing is based on 20% and 80% of V_{SS}.

Display Control Output Timing

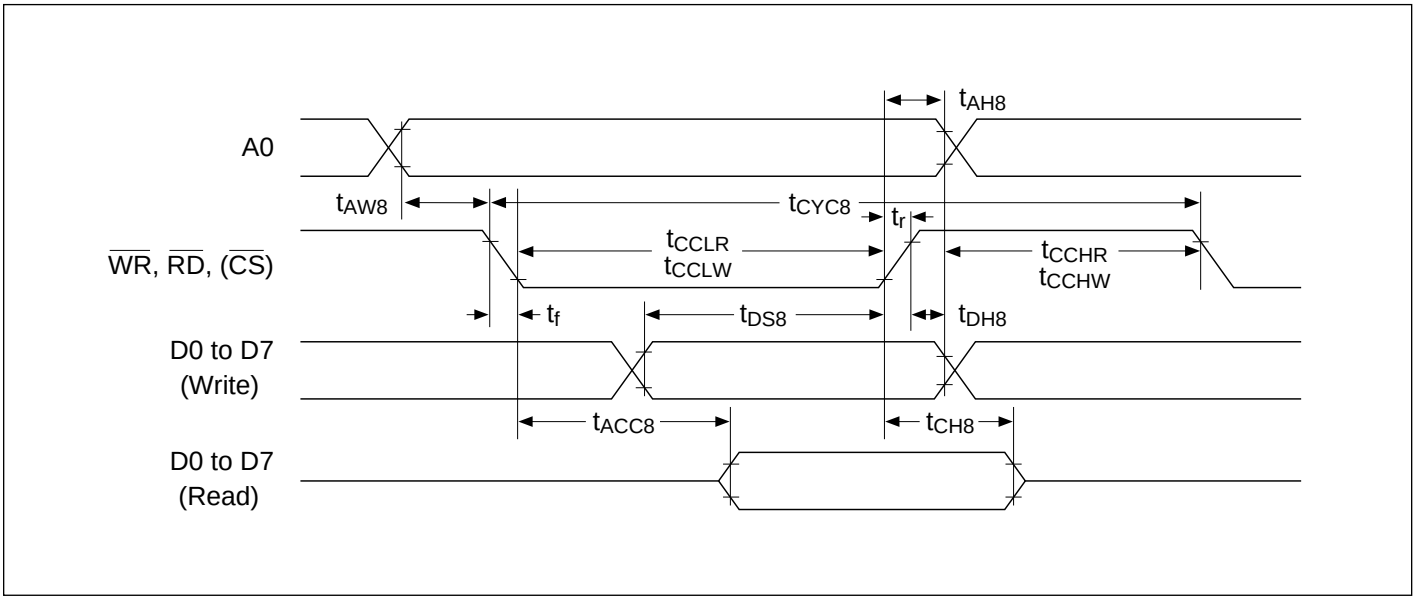
V_{SS} = –5.5 to –4.5V, T_a = –30 to 85°C

Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
FR delay time	t_{DFR}	C_L = 50 pF	—	60	150	ns
SYNC delay time	t_{DSNC}	C_L = 100 pF	—	60	150	ns
DYO LOW-level delay time	t_{DOL}		—	70	160	ns
DYO HIGH-level delay time	t_{DOH}		—	70	160	ns
CLO to DYO LOW-level delay time	t_{CDL}	SED156X operating in master mode only	—	40	100	ns
CLO to DYO HIGH-level delay time	t_{CDH}	SED156X operating in master mode only	—	40	100	ns

V_{SS} = –4.5 to –2.7V, T_a = –30 to 85°C

Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
FR delay time	t_{DFR}	C_L = 50 pF	—	120	240	ns
SYNC delay time	t_{DSNC}	C_L = 100 pF	—	120	240	ns
DYO LOW-level delay time	t_{DOL}		—	140	250	ns
DYO HIGH-level delay time	t_{DOH}		—	140	250	ns
CLO to DYO LOW-level delay time	t_{CDL}	SED156X operating in master mode only	—	100	200	ns
CLO to DYO HIGH-level delay time	t_{CDH}	SED156X operating in master mode only	—	100	200	ns

3.5 SYSTEM BUSES: READ/WRITE CHARACTERISTICS I (80-SERIES MPU)



V_{SS} = –5.0 ± 10%, T_a = –30 to 85°C

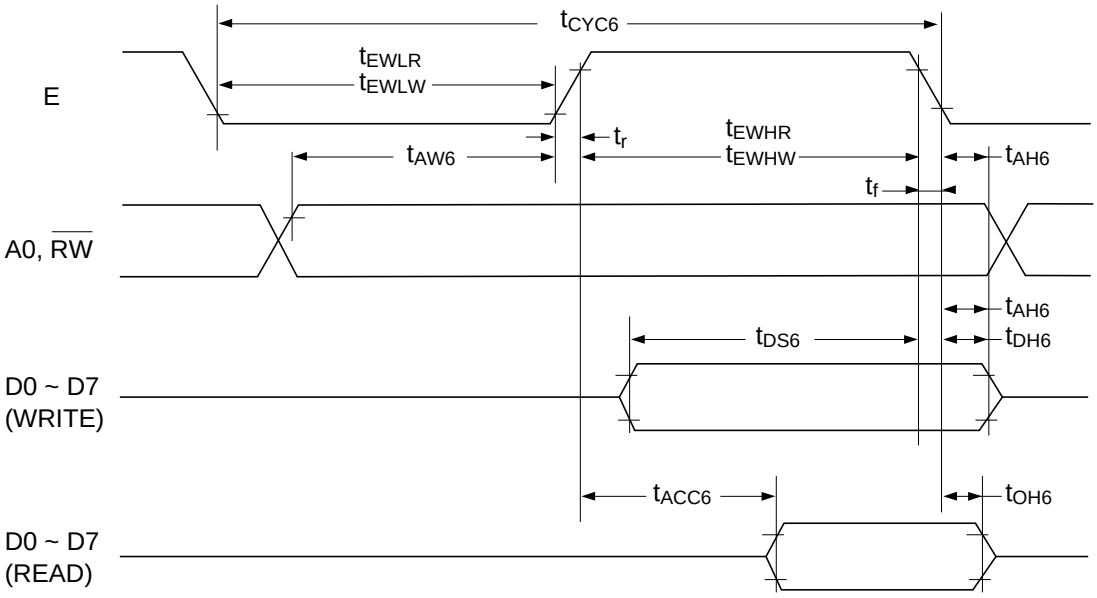
Parameter	Signal	Symbol	Condition	Min	Max	Unit
Address hold time	A0, CS	t_{AH8}		10	—	ns
Address setup time		t_{AW8}		10	—	ns
System cycle time		t_{CYC8}		200	—	ns
Control L pulse width (WR)	$\overline{WR}$	t_{CCLW}		22	—	ns
Control L pulse width (RD)	$\overline{RD}$	t_{CCLR}		77	—	ns
Control H pulse width (WR)	$\overline{WR}$	t_{CCHW}		172	—	ns
Control H pulse width (RD)	$\overline{RD}$	t_{CCHR}		117	—	ns
Data setup time		t_{DS8}		20	—	ns
Data hold time		t_{DH8}		10	—	ns
$\overline{RD}$ access time	D0 ~ D7	t_{ACC8}	CL = 100pF	—	70	ns
Output disable time		t_{CH8}		10	50	ns
Input signal change time		t_r, t_f		—	15	ns

V_{SS} = –2.7 to –4.5V, T_a = –30 to 85°C

Parameter	Signal	Symbol	Condition	Min	Max	Unit
Address hold time	A0, CS	t_{AH8}		25	—	ns
Address setup time		t_{AW8}		25	—	ns
System cycle time		t_{CYC8}		450	—	ns
Control L pulse width (WR)	$\overline{WR}$	t_{CCLW}		44	—	ns
Control L pulse width (RD)	$\overline{RD}$	t_{CCLR}		194	—	ns
Control H pulse width (WR)	$\overline{WR}$	t_{CCHW}		394	—	ns
Control H pulse width (RD)	$\overline{RD}$	t_{CCHR}		244	—	ns
Data setup time		t_{DS8}		40	—	ns
Data hold time		t_{DH8}		20	—	ns
$\overline{RD}$ access time	D0 ~ D7	t_{ACC8}	CL = 100pF	—	140	ns
Output disable time		t_{CH8}		10	100	ns
Input signal change time		t_r, t_f		—	15	ns

Notes:
1. When using the system cycle time in the high-speed mode, it is limited by $t_r + t_f \leq (t_{CYC8} – t_{CCLW} – t_{CCHW})$ or $t_r + t_f \leq (t_{CYC8} – t_{CCLR} – t_{CCHR})$
2. All signal timings are limited based on 20% and 80% of V_{SS} voltage.
3. Read/write operation is performed while CS ($\overline{CS1}$ and CS2) is active and the RD or WR signal is in the low level.
   If read/write operation is performed by the RD or WR signal while CS is active, it is determined by the $\overline{RD}$ or $\overline{WR}$ signal timing.
   If read/write operation is performed by CS while the RD or WR signal is in the low level, it is determined by the CS active timing.

3.6 SYSTEM BUSES: READ/WRITE CHARACTERISTICS II (68-SERIES MPU)



V_{SS} = –5.0 ± 10%, T_a = –30 to 85°C

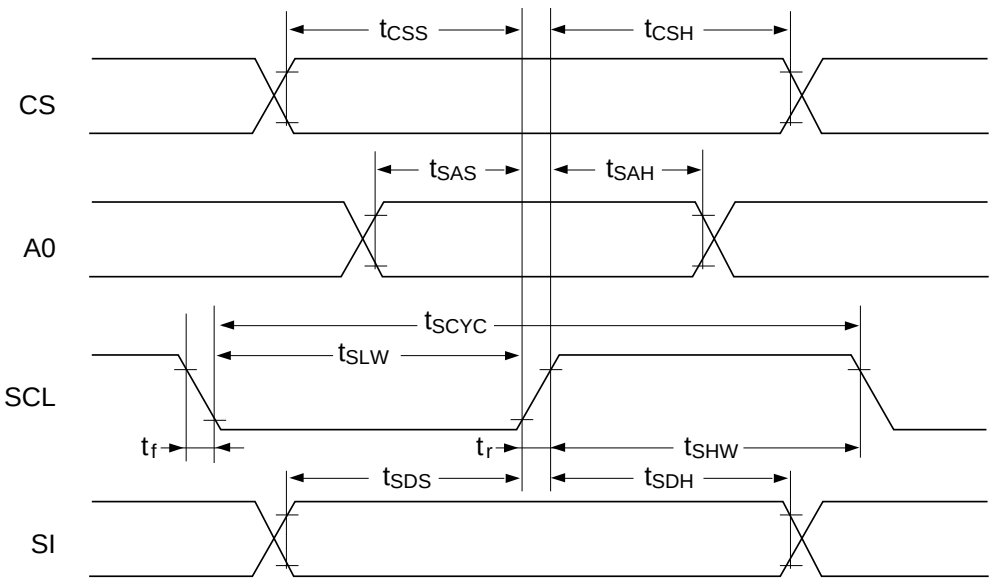
Parameter		Signal	Symbol	Condition	Min	Max	Unit
System cycle time			t_{CYC6}		200	—	ns
Address setup time		(A0)	t_{AW6}		10	—	ns
Address hold time		R/$\overline{W}$	t_{AH6}		10	—	ns
Data setup time		D0 ~ D7	t_{DS6}		20	—	ns
Data hold time			t_{DH6}		10	—	ns
Output disable time			t_{OH6}	CL = 100pF	10	50	ns
Access time			t_{ACC6}		—	70	ns
Enable H pulse width	READ	E	t_{EWHR}		77	—	ns
	WRITE		t_{EWHW}		22	—	ns
Enable L pulse width	READ	E	t_{EWLR}		117	—	ns
	WRITE		t_{EWLW}		172	—	ns
Input signal change time			t_r, t_f		—	15	ns

V_{SS} = –2.7 to +4.5V, T_a = –30 to 85°C

Parameter		Signal	Symbol	Condition	Min	Max	Unit
System cycle time		A0, CS	t_{CYC6}		450	—	ns
Address setup time		($\overline{CS1}$, CS2)	t_{AW6}		25	—	ns
Address hold time		R/$\overline{W}$	t_{AH6}		25	—	ns
Data setup time		D0 ~ D7	t_{DS6}		40	—	ns
Data hold time			t_{DH6}		20	—	ns
Output disable time			t_{OH6}	CL = 100pF	20	100	ns
Access time			t_{ACC5}		—	140	ns
Enable H pulse width	READ	E	t_{EWHR}		154	—	ns
	WRITE		t_{EWHW}		44	—	ns
Enable L pulse width	READ	E	t_{EWLR}		244	—	ns
	WRITE		t_{EWLW}		394	—	ns
Input signal change time			t_r, t_f		—	15	ns

Notes:
1. When using the system cycle time in the high-speed mode, it is limited by $t_r + t_f \leq (t_{CYC6} - t_{EWLW} - t_{EWHW})$ or $t_r + t_f \leq (t_{CYC6} - t_{EWLR} - t_{EWHR})$
2. All signal timings are limited based on 20% and 80% of V_{SS} voltage.
3. Read/write operation is performed while CS ($\overline{CS1}$ and CS2) is active and the E signal is in the high level.
   If read/write operation is performed by the E signal while CS is active, it is determined by the E signal timing.
   If read/write operation is performed by CS while the E signal is in the high level, it is determined by the CS active timing.

3.7 SERIAL INTERFACE



V_{SS} = –5.0 ± 10%, T_a = –30 to 85°C

Parameter	Signal	Symbol	Condition	Min	Max	Unit
Serial clock cycle	SCL	t_{SCYC}		500	—	ns
SCL high pulse width		t_{SHW}		150	—	ns
SCL low pulse width		t_{SLW}		150	—	ns
Address setup time	A0	t_{SAS}		120	—	ns
Address hold time		t_{SAH}		200	—	ns
Data setup time	SI	t_{SDS}		120	—	ns
Data hold time		t_{SDH}		50	—	ns
CS-SCL time	CS	t_{CSS}		30	—	ns
		t_{CSH}		400	—	ns
Input signal change time		t_r, t_f		—	50	ns

V_{SS} = –2.7 to –4.5V, T_a = –30 to 85°C

Parameter	Signal	Symbol	Condition	Min	Max	Unit
Serial clock cycle	SCL	t_{SCYC}		1000	—	ns
SCL high pulse width		t_{SHW}		300	—	ns
SCL low pulse width		t_{SLW}		300	—	ns
Address setup time	A0	t_{SAS}		250	—	ns
Address hold time		t_{SAH}		400	—	ns
Data setup time	SI	t_{SDS}		250	—	ns
Data hold time		t_{SDH}		100	—	ns
CS-SCL time	CS	t_{CSS}		60	—	ns
		t_{CSH}		800	—	ns
Input signal change time		t_r, t_f		—	50	ns

Note: *2. All signal timings are limited based on 20% and 80% of V_{SS} voltage.

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4.0

Functional Description

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4.1 MICROPROCESSOR INTERFACE

4.1.1 Parallel/Serial Interface

Table 4.1 Parallel/serial Interface Selection

P/S	Input Type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	SI	SCL	D0 to D7
HIGH	Parallel	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	×	×	D0 to D7
LOW	Serial	$\overline{CS1}$	CS2	A0	×	×	×	SI	SCL	(Hi-Z)

× = don't care

Parallel data can be transferred in either direction between the controlling microprocessor and the SED1560 Series via an 8-bit I/O buffer (D0 to D7). Serial data can be sent from the microprocessor to the SED1560 Series through the serial data input (SI), but not from the SED1560 Series to the microprocessor. The parallel or serial interface is selected by setting P/S as shown in Table 4.1.

For the parallel interface, the type of microprocessor is selected by C86 as shown in Table 4.2.

Table 4.2 Microprocessor Selection for Parallel Interface

C86	MPU Bus Type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7
HIGH	6800-series	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	D0 to D7
LOW	8080-series	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7

4.1.2 Parallel Interface

A0, $\overline{WR}$ (or R/$\overline{W}$) and $\overline{RD}$ (or E) determine the type of parallel data transfer. See Table 4.3.

Table 4.3 Parallel Data Transfer

Com-mon	6800 Series	8080 Series		Description
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Display data read out
1	0	1	0	Display data write
0	1	0	1	Status read
0	0	1	0	Write to internal register (command)

4.1.3 Serial Interface

The serial interface consists of an 8-bit shift register and a 3-bit counter. These are reset when CS1 is HIGH and CS2 is LOW. When these states are reversed, serial data and clock pulses can be received from the microprocessor on SI and SCL respectively.

Serial data is read on the rising edge of SCL and must be input at SI in the sequence D7 to D0. On every eighth clock pulse, the data is transferred from the shift register and processed as 8-bit parallel data.

Input data is display data when A0 is HIGH and command data when A0 is LOW. A0 is read on the rising edge of every eighth clock signal. See Figure 4.1.

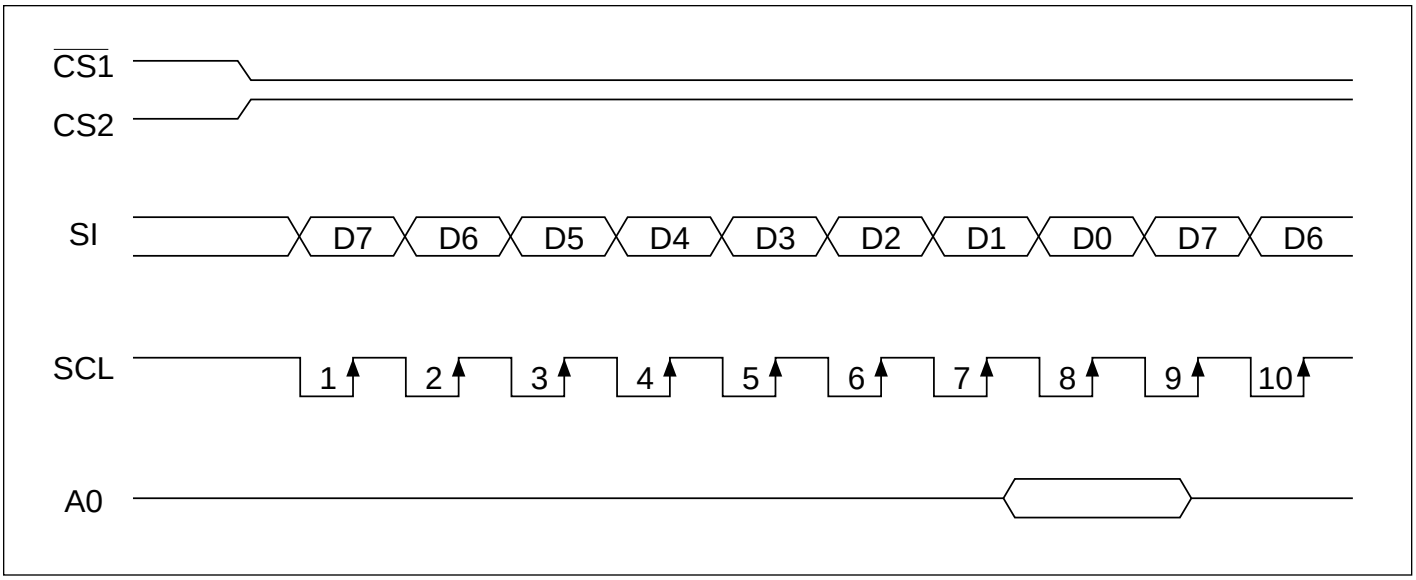


Figure 4.1 Serial interface timing

4.1.4 Chip Select Inputs

Data transfer between the microprocessor and the SED1560 Series is enabled when CS1 is LOW and CS2 is HIGH. If these pins are set to any other values, D0 to D7 are in high impedance state and will not accept data.

4.2 DATA TRANSFER

To match the timing of the display data RAM and registers to that of the controlling microprocessor, the SED1560 Series uses an internal data bus and bus buffer. When the microprocessor reads the contents of RAM, the data for the initial read cycle is first stored in the bus buffer (dummy read cycle). On the next read cycle, the data is read from the bus buffer onto the microprocessor bus. At the same time, the next block of data is transferred from RAM to the bus buffer. Likewise, when the microprocessor writes data to display data RAM, the data is first stored in the bus buffer before being written to RAM at the next write cycle.

When writing data from the microprocessor to RAM, there is no delay since data is automatically transferred from the bus buffer to the display data RAM. If the data rate is required to slow down, the microprocessor can insert a NOP instruction which has the same effect as executing a wait procedure.

When a sequence of address sets is executed, a dummy read cycle must be inserted between each pair of address sets. This is necessary because the addressed data from the RAM is delayed one cycle by the bus buffer, before it is sent to the microprocessor. A dummy read cycle is thus necessary after an address set and after a write cycle.

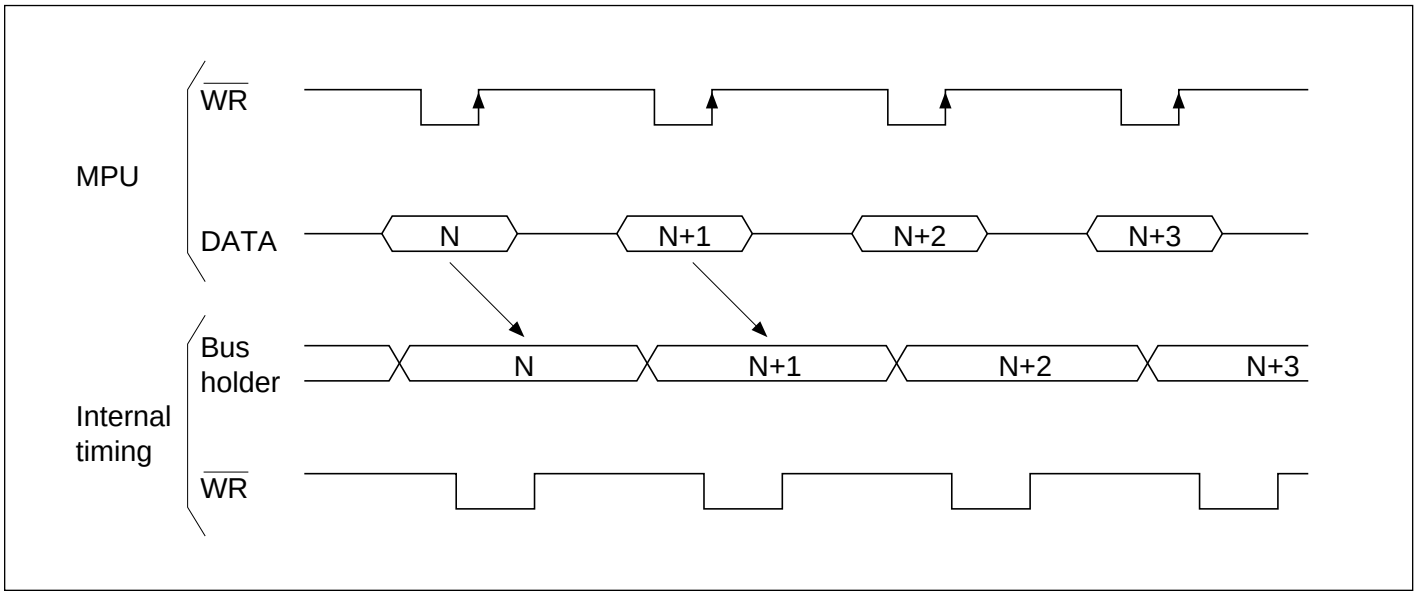


Figure 4.2 Write timing

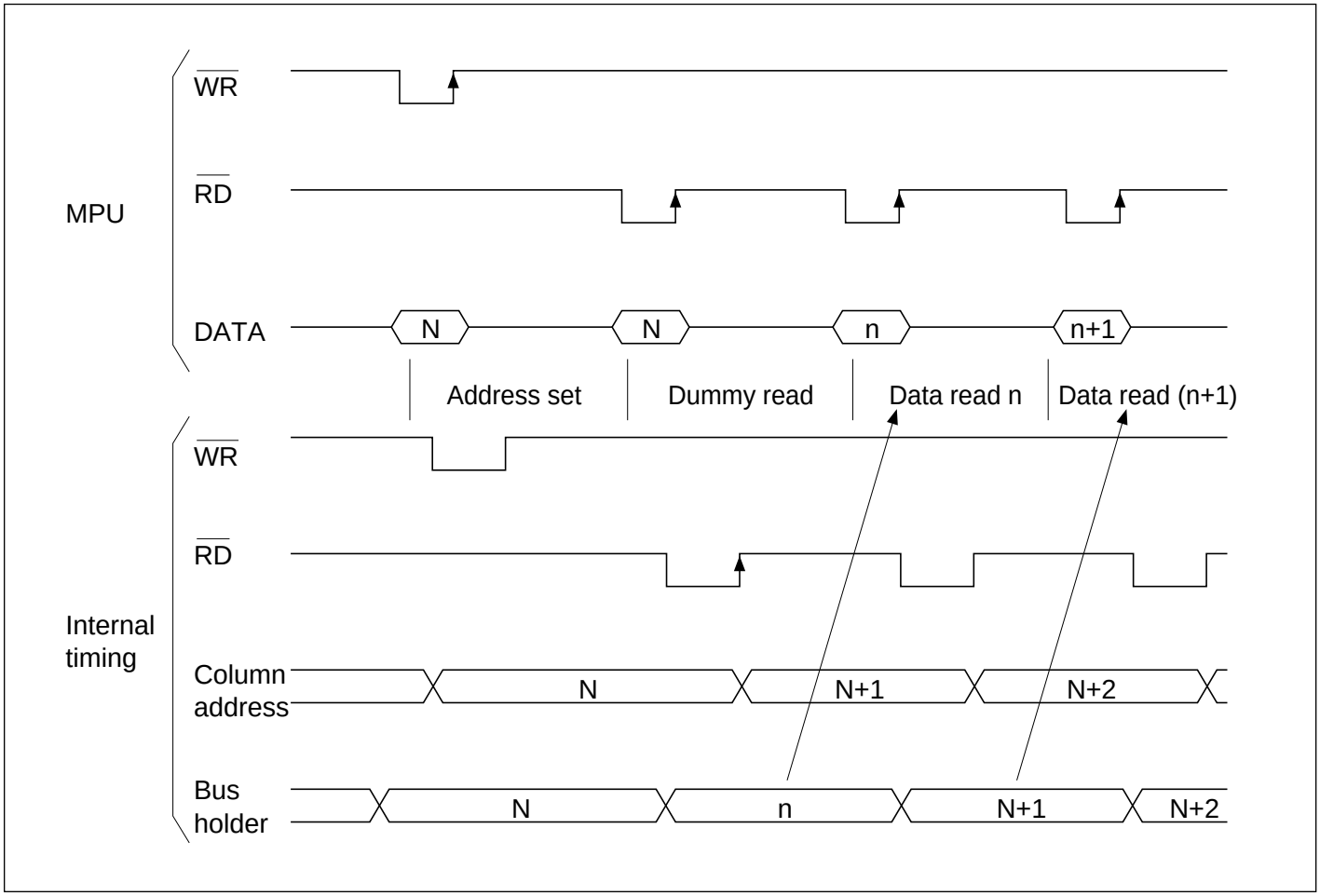


Figure 4.3 Read timing

4.3 STATUS FLAG

The SED1560 Series has a single bit status flag, D7. When D7 is HIGH, the device is busy and will accept only a Status Read command. It is not necessary for the microprocessor to check the status of this bit before each command, if enough time is allowed for the last cycle to be completed.

4.4 DISPLAY DATA RAM

The SED1560 Series stores the display data sent from the microcomputer in the built-in display data RAM (166 × 65 bits) and generates the LCD drive signals. It is a 166-column × 65-row addressable array as shown in Figure 4.4.

The 65 rows are divided into 8 pages of 8 lines and a ninth page with a single line (D0 only). Data is read from or written to the 8 lines of each page directly through D0 to D7.

The microprocessor reads from and writes to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written to RAM at the same time as data is being displayed, without causing the LCD to flicker.

The time taken to transfer data is very short, because the microprocessor inputs D0 to D7 correspond to the LCD common lines as shown in Figure 4.5. Large display configuration can thus be created using multiple SED1560 Series devices.

4.5 COLUMN ADDRESS COUNTER

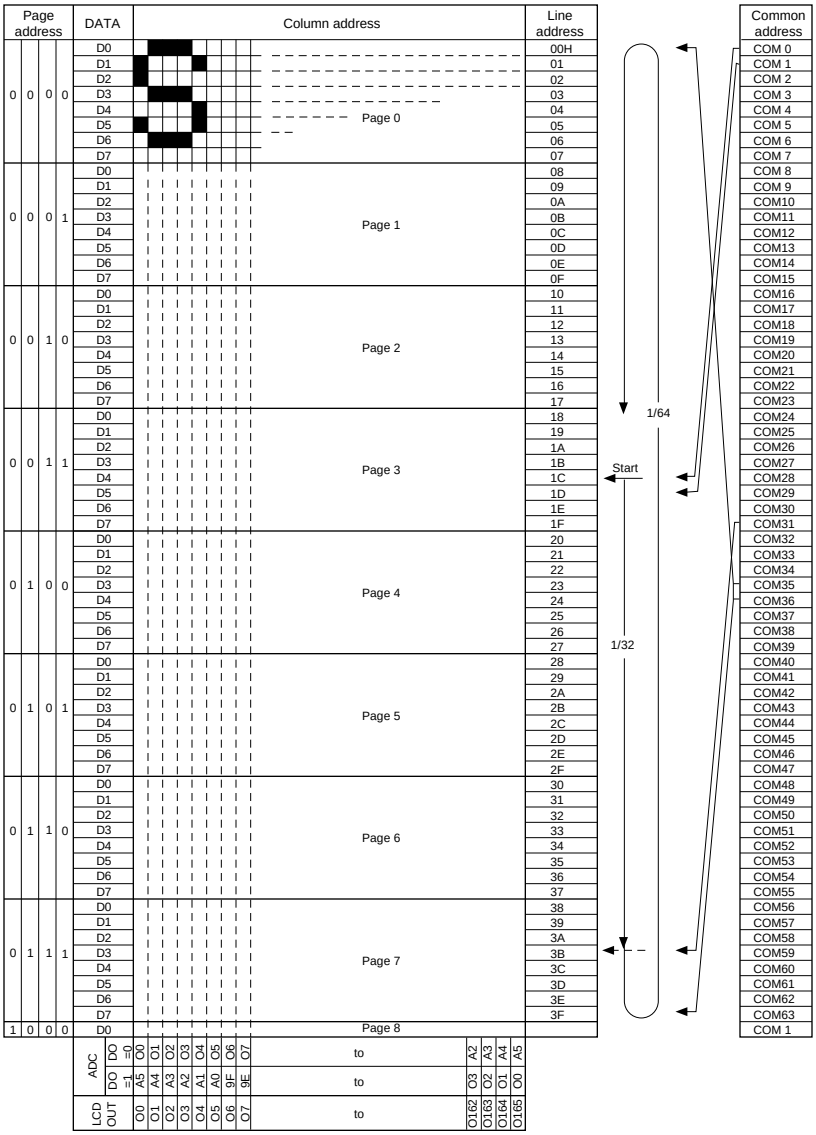
The column address counter is an 8-bit presettable counter that provides the column address to display data RAM. See Figure 4.4. It is incremented by 1 each time a read or write command is received. The counter automatically stops at the highest address, A6H. The contents of the column address counter are changed by the Column Address Set command. This counter is independent of the page address register.

When the Select ADC command is used to select inverse display operation, the column address decoder inverts the relationship between the RAM column data and the display segment outputs.

4.6 PAGE ADDRESS REGISTER

The 4-bit page address register provides the page address to display data RAM. The contents of the register are changed by the Page Address Set command.

Page address 8 (1000) is a special use RAM area for the indicator.



Note: For 1/65 and 1/33 display duty cycles, page 9 is accessed following 1BH and 3BH, respectively.

Figure 4.4 Display data RAM addressing

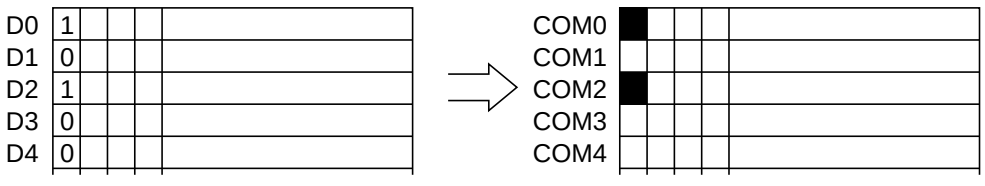


Figure 4.5 RAM-to-LCD data transfer

4.7 INITIAL DISPLAY LINE REGISTER

The Initial Display Line register stores the address of the RAM line that corresponds to the first (normally the top) line (COM0) of the display. See Figure 4.4. The contents of this 6-bit register are changed by the Initial Display Line command. At the start of each LCD frame, synchronized with SYNC, the initial line is copied to the line counter. The line counter is then incremented on the CL clock signal once for every display line. This generates the line addresses for the transfer of the 166 bits of RAM data to the LCD drivers.

If a 1/65 or 1/33 display duty cycle is selected by the DUTY+1 command, the line address corresponding to the 65th or 33rd SYNC signal is changed and the indicator special-use line address is selected. If the DUTY+1 command is not used, the indicator special-use line address is not selected.

4.8 OUTPUT SELECTION CIRCUIT

The number of common (COM) and segment (SEG) driver outputs can be selected to fit different LCD panel configurations by the output selection circuit.

There are 70 segment-only outputs (O32 to O101) and 96 common or segment dual outputs (O0 to O31 and O102 to O165). A command selects the status of the dual common/segment outputs. Figure 4.6 shows the six different LCD driver arrangements.

The necessary LCD driver voltage is automatically allocated to the COM/SEG dual outputs when their function is determined by the output selection circuit.

The SED1560 selects Case 1, 2 or 6 while the SED1561 selects Case 3, 4, 5 or 6. The COM/SEG output status for the SED1562 is fixed and so cannot be selected.

When COM outputs are assigned to the output drivers, the unused RAM area is not available. However, all RAM column addresses can still be accessed by the microprocessor.

Since duty setting and output selection are independent, the appropriate duty must be selected for each case.

Cases 1 to 6 are determined according to the three lowest bits in the output status register in the output selection circuit. The COM output scanning direction can be selected by setting bit D3 in the output status register to “H” or “L”.

When the DUTY+1 command is executed, pin COM1 becomes as shown in Figure 4.4 irrelevant to output selection.

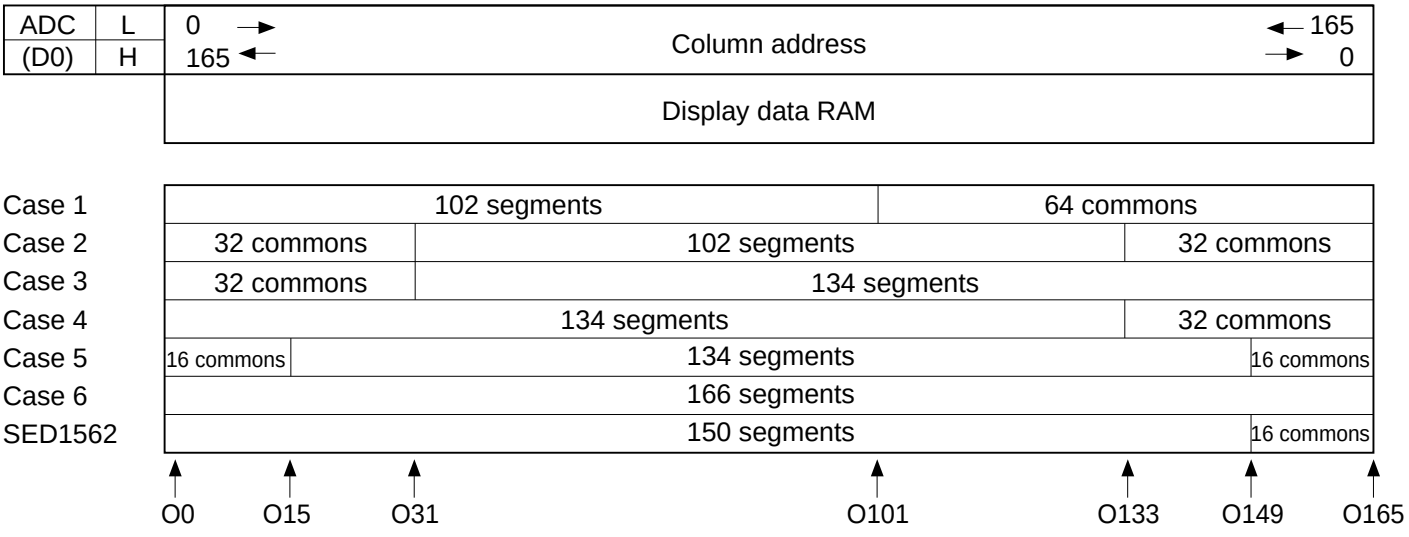


Figure 4.6 Output configuration selection

Since master/slave operation and the output selection circuit are completely independent in the SED1560 Series, a chip on either the master or slave side can be allocated to the COM output function in multi-chip configuration.

The LCD driver outputs shown in Table 4.5 become ineffective when the SED1560 or SED1561 is used with 1/48 or 1/24 duty, respectively. In this case, ineffective outputs are used in the open state.

Table 4.4

	SED1560		SED1561		SED1562
Duty	1/64	1/48	1/32	1/24	1/16
COMI function	COM64	COM48	COM32	COM24	COM16

Table 4.5

		Output Status Register				Ineffective Output
		D3	D2	D1	D0	
SED1560	Case 1	0	1	0	1	O150 ~ O165
		1	1	0	1	O102 ~ O117
	Case 2	0	1	1	0	O150 ~ O165
		1	1	1	0	O16 ~ O31
SED1561	Case 3	0	0	1	1	O0 ~ O7
		1	0	1	1	O23 ~ O31
	Case 4	0	0	1	0	O158 ~ O165
		1	0	1	0	O134 ~ O141
	Case 5	0	0	0	1	O158 ~ O165
		1	0	0	1	O8 ~ O15

4.9 SED1560 OUTPUT STATUS

The SED1560 selects any output status from Cases 1, 2 and 6.

1/64 Duty (Display Area 102 × 64)

Case	Status Register				LCD Driver Output							
	D3	D2	D1	D0	O0	O31	O32	O101	O102	O133	O134	O165
1	0	1	0	1					COM0 →			COM63
	1	1	0	1					COM63 ←			COM0
2	0	1	0	0	COM31 ←	COM0	SEG102				COM32 →	COM63
	1	1	0	0	COM32 →	COM63	SEG102				COM31 ←	COM0
6	—	0	0	0	SEG166							

1/48 Duty (Display Area 102 × 48)

Case	Status Register				LCD Driver Output							
	D3	D2	D1	D0	O0	O31	O32	O101	O102	O133	O134	O165
1	0	1	0	1					COM0 →		COM47	
	1	1	0	1						COM47 ←		COM0
2	0	1	0	0	COM31 ←	COM0	SEG102				COM32→47	
	1	1	0	0	COM32→47		SEG102				COM31 ←	COM0
6	—	0	0	0	SEG166							

4.10 SED1561 OUTPUT STATUS

The SED1561 selects any output status from Cases 3, 4, 5 and 6.

1/32 Duty (Display Area 134 × 32)

Case	Status Register				LCD Driver Output						
	D3	D2	D1	D0	O0	O15	O16	O31	O32	O133	O134 149	150 O165
3	0	0	1	1	COM31 ←	COM0	SEG134					
	1	0	1	1	COM0 →	COM31	SEG134					
4	0	0	1	0	SEG134						COM0 →	COM31
	1	0	1	0	SEG134						COM31 ←	COM0
5	0	0	0	1	15 ←	COM0	SEG134					COM16→31
	1	0	0	1	COM16→31		SEG134					15 ← COM0
6	—	0	0	0	SEG166							

1/24 Duty (Display Area 134 × 24)

Case	Status Register				LCD Driver Output				
	D3	D2	D1	D0	O0 O15	O16 O31	O32 O133	O134 149	150 O165
3	0	0	1	1		COM23 ← COM0	SEG134		
	1	0	1	1	COM0 → COM23		SEG134		
4	0	0	1	0	SEG134			COM0 → COM23	
	1	0	1	0	SEG134				COM23 ← COM0
5	0	0	0	1	15 ← COM0	SEG134			16 → 23
	1	0	0	1	16 → 23	SEG134			15 ← COM0
6	—	0	0	0	SEG166				

4.11 SED1562 OUTPUT STATUS

COM/SEG output status of the SED1562 is fixed.

1/16 Duty (Display Area 150 × 16)

LCD Driver Output	
O0 O149	O150 O165
SEG150	15 ← COM0

4.12 DISPLAY TIMERS

4.12.1 Line Counter and Display Data Latch Timing

The display clock, CL, provides the timing signals for the line counter and the display data latch. The RAM line address is generated synchronously using the display clock. The display data latch synchronizes the 166-bit display data with the display clock.

The timing of the LCD panel driver outputs is independent of the timing of the input data from the microprocessor.

4.12.2 FR and SYNC

The LCD AC signal, FR, and the synchronization signal, SYNC, are generated from the display clock. The FR controller generates the timing for the LCD panel driver outputs. Normally, 2-frame wave patterns are generated, but *n*-line inverse wave patterns can also be generated. These produce a high-quality display if *n* is based on the LCD panel being used.

SYNC synchronizes the timing of the line counter and common timers. It is also needed to synchronize the frame period and a 50% duty clock.

In a multiple-chip configuration, FR and SYNC are inputs. The SYNC signal from the master synchronizes the line counter and common timing of the slave.

4.12.3 Common Timing Signals

The internal common timing and the special-use common driver start signal, DYO, are generated from CL. As shown in Figures 4.7 and 4.8, DYO outputs a HIGH-level pulse on the rising edge of the CL clock pulse that precedes a change on SYNC. DYO is generated by both the SED1560 Series devices, regardless of whether the device is in master or slave mode. However, when operating in slave mode, the device duty and the external SYNC signal must be the same as that of the master. In a multiple-chip configuration, FR and SYNC must be supplied to the slave from the master.

Table 4.6 Master and Slave Timing Signal Status

Part Number	Mode	FR	SYNC	CLO	DYO
SED1560 Series	Master	Output	Output	CL Output	Output
	Slave	Input	Input	High Imped-ance	Output

4.13 TWO-FRAME AC DRIVER WAVEFORM (SED1561, 1/32 DUTY)

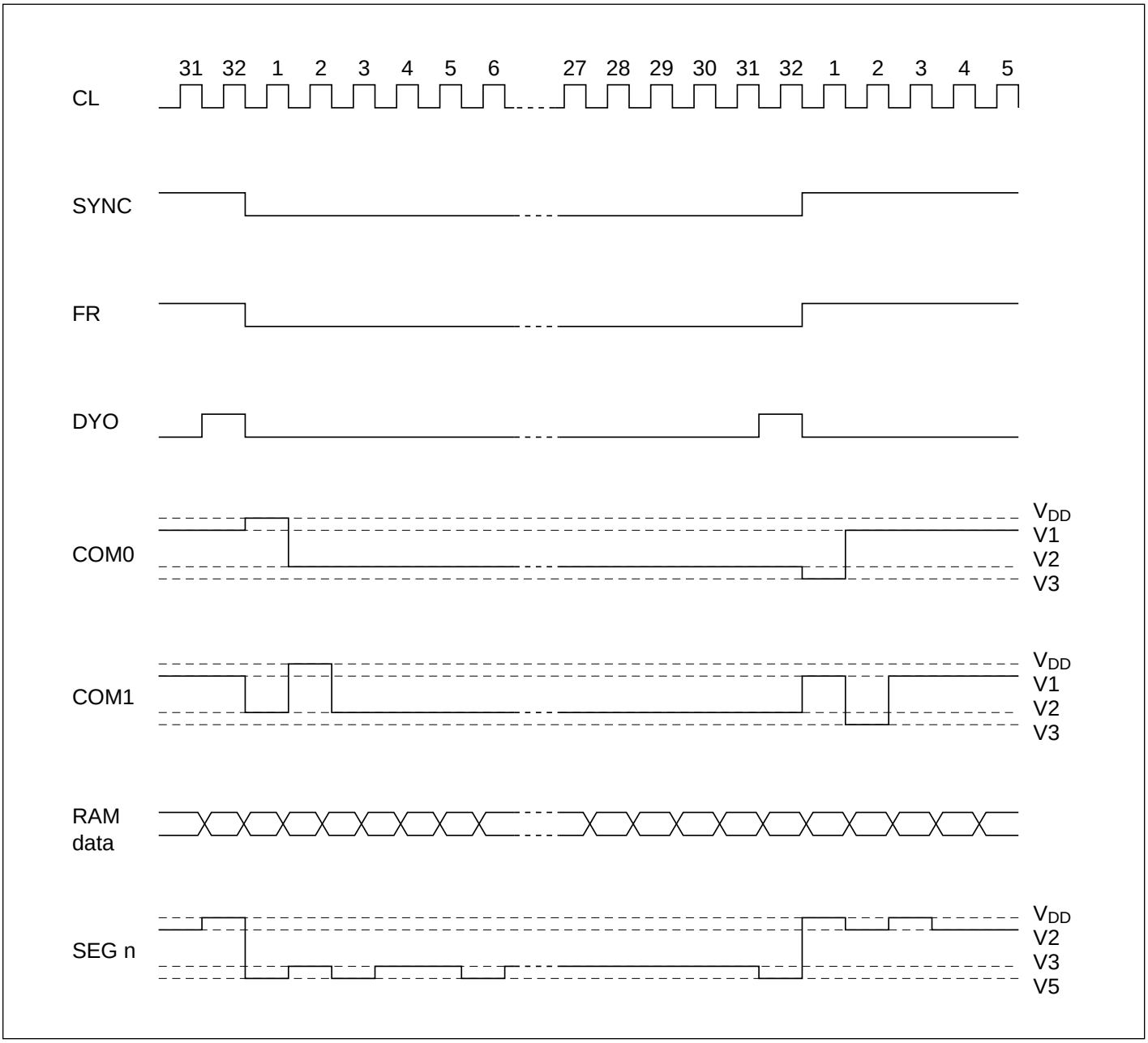
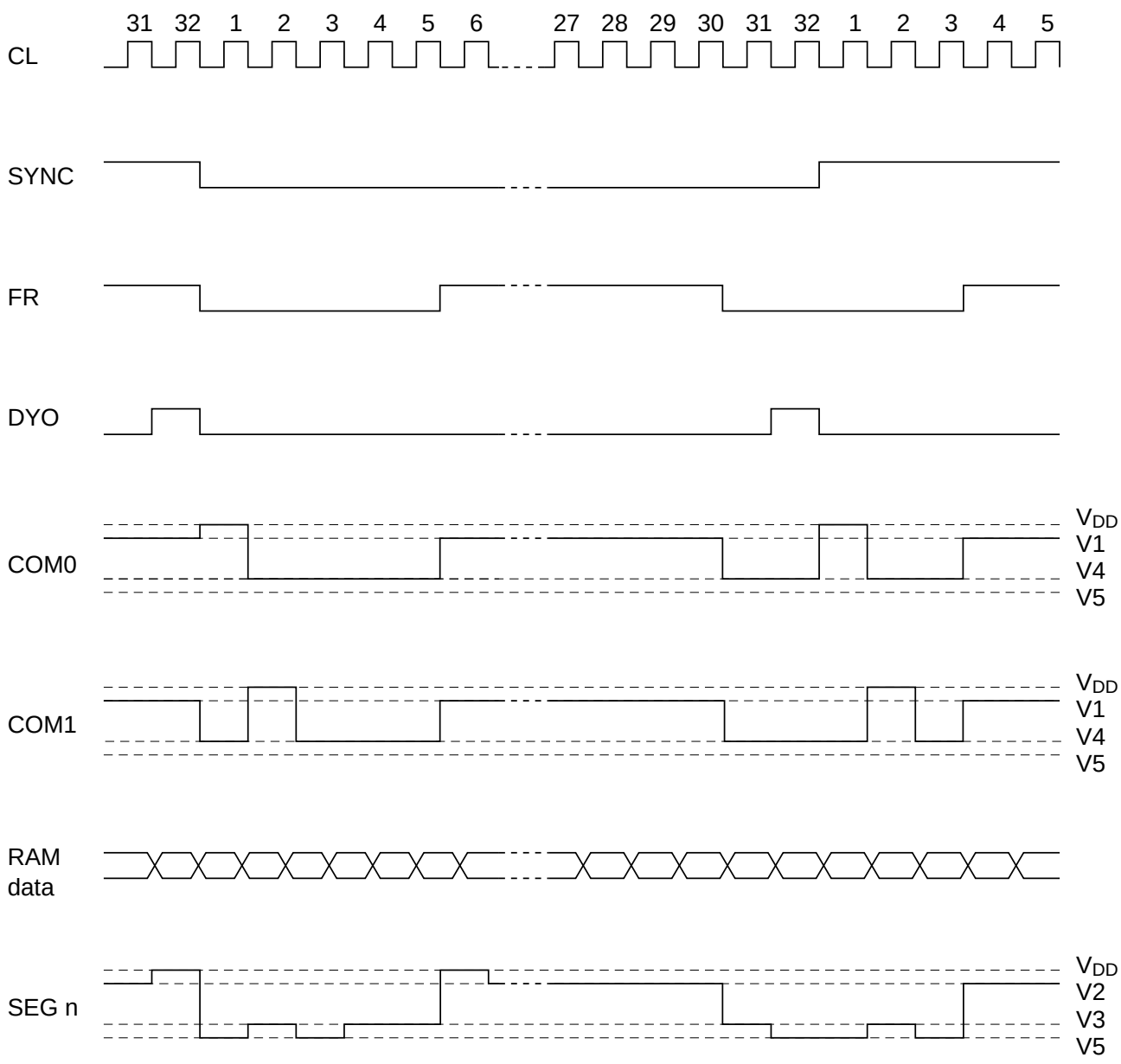


Figure 4.7 Frame driver timing for duty 1/32

4.14 *n* LINE INVERSE DRIVER WAVEFORM (*n*=5, LINE INVERSE REGISTER 4)



Note: When *n* = 5, the line inversion register is set to 4.

Figure 4.8 Line inverse driver timing

4.15 DISPLAY DATA LATCH

Display data is transferred from RAM to the LCD drivers through the display data latch. This latch is controlled by the Display ON/OFF, Display All Points ON/OFF and Normal/Inverse Display commands.

These commands do not alter the data.

4.16 LCD DRIVER

The LCD driver converts RAM data into the 167 outputs that drive the LCD panel. There are 70 segment outputs, 96 segment or common dual outputs, and a COM1 output for the indicator display.

Two shift registers for the common/segment drivers are used to ensure that the common outputs are output in the correct sequence. The driver output voltages depend on the display data, the common scanning signal and FR.

4.17 DISPLAY DATA LATCH CIRCUIT

The display data latch circuit temporarily stores the output display data from the display data RAM to the LCD driver circuit in each common period. Since the Normal/Inverse Display, Display ON/OFF and Display All Points ON/OFF commands control the data in this latch, the data in the display data RAM remains unchanged.

4.18 LCD DRIVER CIRCUIT

This multiplexer generates 4-value levels for the LCD driver, having 167 outputs of 70 SEG outputs, 96 SEG/COM dual outputs and a COM output for the indicator display. The SEG/COM dual outputs have a shift register and sequentially transmit COM scanning signals. The LCD driver voltage is output according to the combination of display data, COM scanning signal and FR signal. Figure 4.9 shows a typical SEG/COM output waveform.

4.19 OSCILLATOR CIRCUIT

The low power consumption type CR oscillator adjusting the oscillator frequency by use of only oscillator resistor R_f is used as a display timing signal source or clock for the voltage raising circuit of the LCD power supply.

The oscillator circuit is available only in the master operation mode. When a signal from the oscillator circuit is used for display clock, fix the CL pin to the V_{SS} level. When the oscillator circuit is not used, fix the OSC1 or OSC2 pin to the V_{DD} or V_{SS} level, respectively.

The oscillator signal frequency is divided and output from the CL0 pin as display clock. The frequency is divided to one-fourth, one-eighth, or one-sixteenth in the SED1560, SED1561, or SED1562, respectively.

4.20 FR CONTROL CIRCUIT

The LCD driver voltage supplied to the LCD driver outputs is selected using FR signal.

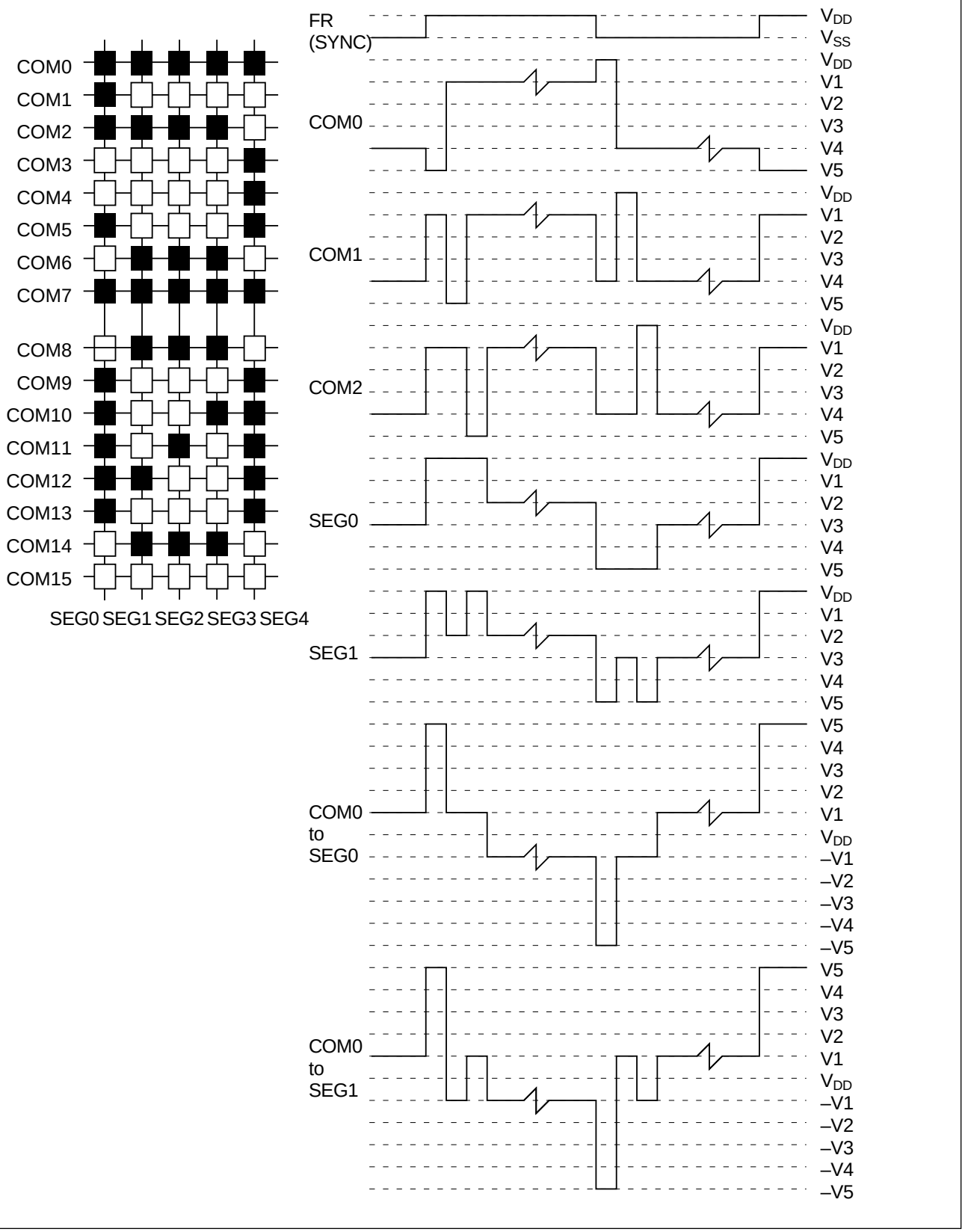


Figure 4.9 Example of segment and common timing

4.21 POWER SUPPLY CIRCUIT

The SED1560 Series has an internal DC/DC converter to generate LCD bias voltages. The internal power supply circuit can be used only when the controller operates in master mode. The power circuit consists of a triple boosting circuit, a voltage regulation circuit and a low power voltage follower circuit.

The power circuit built into SED1560 Series is set for smaller scale liquid crystal panels and it is not suitable when the picture element is larger or to drive a liquid crystal panel with larger indication capacity using multiple chips. It is recommended that an external power supply is used when using a liquid crystal panel with a larger load capacity.

The power supply circuit can be controlled by the built-in power ON/OFF command. When the built-in power is turned off, the boosting circuit, voltage regulation circuit and voltage follower circuit all go open. In this case, the liquid crystal driving voltage V1, V2, V3, V4 and V5 should be supplied from outside and the terminals CAP1+, CAP1–, CAP2+, CAP2–, V_{OUT} and V_R should be kept opened.

Various functions of the power circuit can be selected by combinations of the setting of the T1 and T2. It is also possible to make a combined use of the external power supply and a portion of the functions of the built-in power supply.

When (T1, T2) = (H, L), the boosting circuit does not work and open the boosting circuit terminals (CAP1+, CAP1–, CAP2+ and CAP2–) and apply liquid crystal driving voltage to the V_{OUT} terminals from outside.

When (T1, T2) = (H, H), the boosting circuit and voltage regulation circuit do not work and open the boosting circuit terminals and the VR terminals and apply liquid crystal driving voltage to the V5, and leave the V_{OUT} pin open.

4.22 TRIPLER BOOSTING CIRCUIT

By connecting capacitors C1 between CAP1+ and CAP1–, CAP2+ and CAP2– and V_{SS} – V_{OUT}, the electric potential between V_{DD} – V_{SS} is boosted to the triple toward negative side and outputted from the V_{OUT} terminal. When a double boosting is required, disconnect the capacitor between CAP2+ and CAP2– and short-circuit the CAP2– and V_{OUT} terminals to obtain output boosted to the double out of the V_{OUT} (or CAP2–) terminal.

Signals from the oscillation circuit are used in the boosting circuit and it then is necessary that the oscillation circuit is in operation.

Electric potentials by the boosting functions are shown in Figure 4.10 and 4.11.

Table 4.7

T1	T2	Voltage Converter Circuit	Voltage Regulation Circuit	V/F Circuit	External Voltage Input	Voltage Converter Circuit Terminals	Voltage Regulation Terminals
L	L	O	O	O	—		
L	H	O	O	O	—		
H	L	X	O	O	V_{OUT}	OPEN	
H	H	X	X	O	V5	OPEN	OPEN

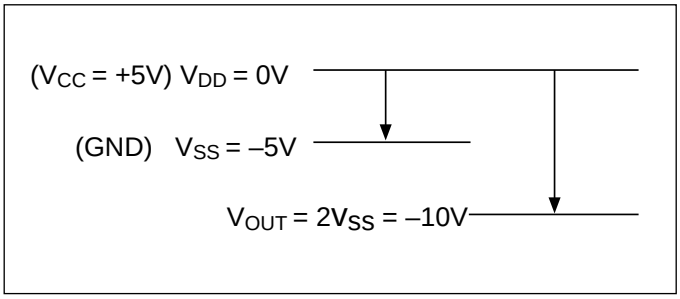


Figure 4.10
Electric potentials of double boosting

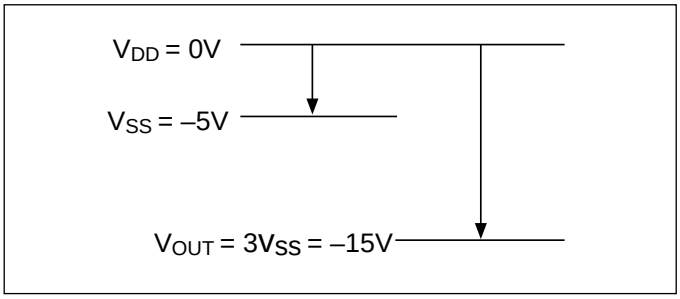


Figure 4.11
Electric potentials of triple boosting

4.23 VOLTAGE REGULATION CIRCUIT (SOFTWARE CONTRAST ADJUSTMENT FUNCTION IS NOT USED)

The boosted voltage coming out from V_{OUT} is adjusted to become the liquid crystal driving voltage V5 via the voltage regulation circuit. V5 voltage can be regulated within a range of $|V5| < |V_{OUT}|$ by adjustment of resistors Ra and Rb and it may be calculated by the following equation:

$$V5 = (1 + \frac{Rb}{Ra}) V_{REG} \qquad \text{Equation 4.1}$$

wherein V_{REG} is the constant voltage source inside the IC and the voltage is constant at $V_{REG} \approx 2.5V$.

Voltage regulation of the V5 output is made by connecting variable resistors between V_R, V_{DD} and V5. For fine adjustment of the V5 voltage, a combination of fixed resistors R1 and R3 and a variable resistor R2 is needed.

Examples of settings of R1, R2, and R3:

- R1 + R2 + R3 = 5 MΩ (determined by the current required to flow between V_{DD} and V5)
- Voltage variation range by R2: –11V ~ –13V (determined based on the characteristics of the liquid crystal being used)

Using the above conditions and Equation 4.1, the following calculations can be made:

R1 = 0.947 MΩ
R2 = 0.174 MΩ
R3 = 3.879 MΩ

The voltage regulation circuit renders a temperature gradient, after V_{REG} output, of about –0.17% / °C, but when any other temperature gradient is needed, connect a thermistor in series with the output voltage regulating resistors.

Since the VR terminal has a high input impedance, it is necessary to take some noise suppression measures, such as using the shortest length wiring or shielded wiring.

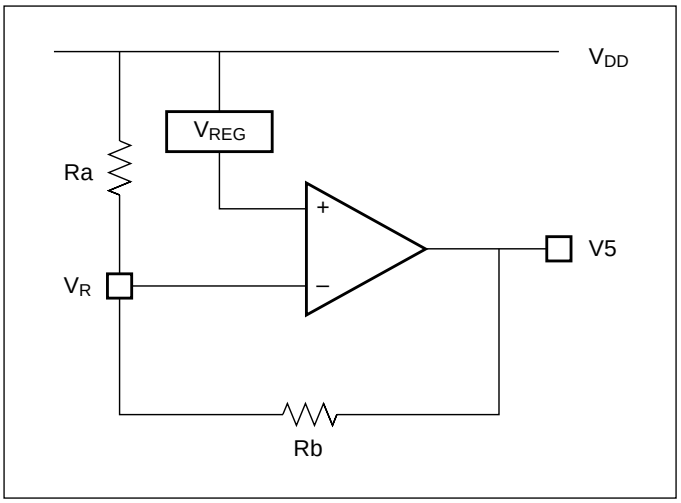


Figure 4.12
Voltage regulation circuit

4.24 VOLTAGE REGULATION CIRCUIT USING SOFTWARE CONTRAST ADJUSTMENT CONTROL FUNCTION

By using software contrast adjustment control function, it is possible to control the liquid crystal driving voltage V5 by inputting corresponding commands to adjust the contrast of the liquid crystal display.

With such an electronic contrast control function, setting 5-bit data to the electronic contrast control register will make available 32 states of voltages from which one voltage level can be selected for the liquid crystal driving voltage V5.

When using the software contrast control function, it is necessary to execute built-in power supply on command after one of (T1, T2) = (L, L), (T1, T2) = (L, H), or (T1, T2) = (H, L) is set.

Example of Constant Setting When Using the Software Contrast Adjustment Control Function

(1) Determine a V5 voltage setting range by the electronic contrast control.

Liquid crystal driving voltage .....V5 – 10V max. to –15V min.
V5 variable voltage width 4V

(2) Determine R_b.

R_b = V5 variable voltage width / I_{REF} (32 states $I_{REF} \approx 6.5\mu A$ constant-current value)
R_b = 4V / 6.5μA (16 states $I_{REF} \approx 3.2\mu A$ constant-current value)
= 615 kΩ

(3) Determine R_a.

$$R_a = \frac{V_{REG}}{(V5 \text{ set voltage max} - V_{REG}) / R_b}$$

(For V_{REG} and V5 set voltage, absolute values are used.)

$$R_a = \frac{2.5V}{(10V - 2.5V) / 615\Omega}$$

= 205 kΩ

(4) Adjust R_a.

Set the electronic contrast control register value to (D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0) or (0, 1, 1, 1, 1), and adjust the R_a value to the optimum contrast.

To set the voltage value by the software contrast adjustment control to the 16 states, fix the data D4 of the electronic contrast control register to L and set data in D3 to D0. At this time, set $I_{REF} \approx 3.2\mu A$ and determine R_a and R_b according to the above steps (1) to (4).

Because I_{REF} is a simplified constant-current source, it is necessary to consider the variation of maximum ±40% as manufacturing dispersion. The temperature dependency of I_{REF} becomes $\Delta I_{REF} \approx -0.0525\ \mu A/°C$ (in the variable voltage 32 states) or $\Delta I_{REF} \approx -0.0234\ \mu A/°C$ (variable voltage 16 states).

Determine R_a and R_b for the LCD to be used, by taking the above dispersion and variations due to temperatures into consideration.

When using the software contrast adjustment control function, R_a must be a variable resistance and the

optimum contrast adjustment described in (4) must be made for each IC chip in order to compensate the V5 voltage value due to the dispersion of V_{REG} and I_{REF}.

When the contrast control function is not used, set the register value to (D4, D3, D2, D1, D0) = (0, 0, 0, 0, 0) by the $\overline{RES}$ signal or electronic contrast control register set command.

4.25 PRECAUTIONS ON USING THE SED1560 SERIES SOFTWARE CONTRAST ADJUSTMENT CONTROL FUNCTION

The SED1560 Series is provided with a software contrast adjustment control function having up to 32 levels to control the regulator. The V5 voltage, when the software contrast control function is used, is represented by the following expression:

$$V5 = (1 + R_b / R_a) . V_{REG} + R_b \times \Delta I_{REF}$$

By this expression, the software contrast control function controls an increment of V5 voltage by means of the current source I_{REF} built into the IC. (In the case of 32 levels, $\Delta I_{REF} = I_{REF} / 32$).

The V5 minimum voltage is set by the resistance ratio of the externally-installed R_a and R_b, and the voltage step width by the software contrast control is determined by the resistance value of R_b.

The reference voltage V_{REG} and current source I_{REF} built into the SED1560 Series are kept constant against voltage variations.

However, IC manufacturing dispersion and variations due to temperatures are caused as shown below.

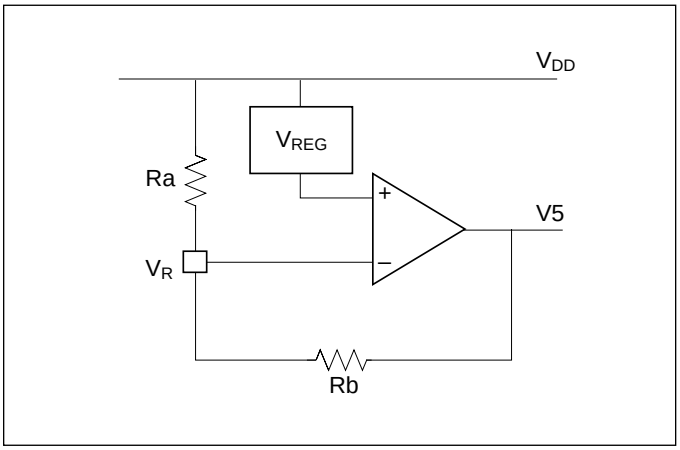
V_{REG} =	2.5V ± 0.15V	V_{REG} = –0.17%/°C
I_{REF} =	3.2µA ± 40% (for 16 levels)	I_{REF} = –0.0234 µA/°C
	6.5µA ± 40% (for 32 levels)	I_{REF} = –0.0525 µA/°C

Example of Constant Setting

Conditions: Center value ..... V_{DD} – V5 = 8.5V
Variable voltage width 3.2V
Variable voltage level ..... 32 levels

(1) Determination of R_b.

R_b = V5 variable voltage width / I_{REF}
= 3.2V / 6.5µA
= 492 kΩ



(2) Determination of Ra.

$$R_a = \frac{V_{REG}}{(V5 \text{ minimum set voltage} - V_{REG}) / R_b}$$

$$= \frac{2.5V}{\{(8.5V - 3.2V/2) - 2.5V\} / 492k\Omega}$$

$$= 280\ k\Omega$$

(3) Temperature dependency of V5 when V_{REG} = 2.5V and I_{REF} = 6.5μA (32 levels).

V5 minimum set voltage (V5 min) = 8.5V – 3.2V/2 = 6.9V

T_a = 25°C

V5 max = V5 minimum set voltage + $R_b \times I_{REF}$
= 6.9V + 492kΩ × 6.5 μA
= 10.1V .....①

V5 typ = (V5 max + V5 min) / 2
= (10.1V + 6.9V) / 2
= 8.5V .....②

T_a = –10°C

V5 min = $(1 + R_b / R_a) \times V_{REG}$ (T_a = –10°C)
= (1 + 492kΩ / 280kΩ) × 2.5V × {1 + (–0.17%/°C) × (–10°C – 25°C)}
= 7.3V ..... ③

V5 max = V5 min + $R_b \times I_{REF}$ (T_a = –10°C)
= 7.3V + 492kΩ × {6.5μA + (–0.0525 μA/°C) × (–10°C – 25°C)}
= 11.4V ..... ④

V5 typ = (V5 max + V5 min) / 2
= (11.4V + 7.3V) / 2
= 9.35V ..... ⑤

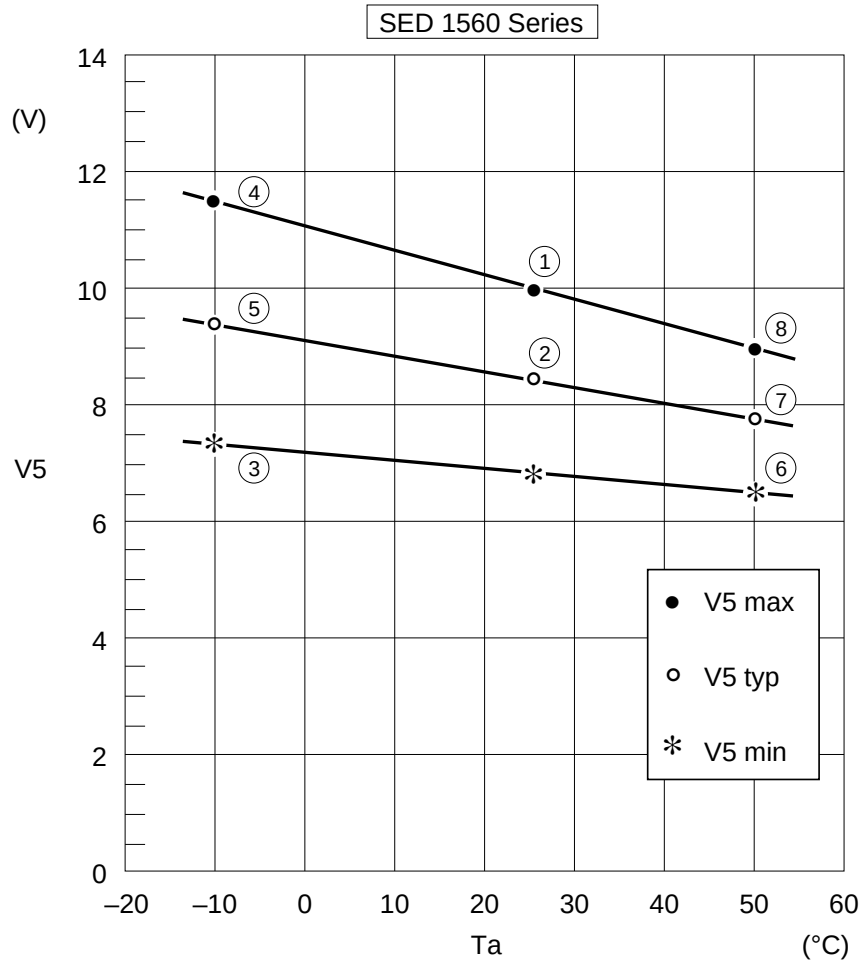
T_a = 50°C

V5 min = $(1 + R_b / R_a) \times V_{REG}$ (T_a = 50°C)
= (1 + 492kΩ / 280kΩ) × 2.5V × {1 + (–0.17%/°C) × (50°C – 25°C)}
= 6.6V ..... ⑥

V5 max = V5 min + $R_b \times I_{REF}$ (T_a = 50°C)
= 6.6V + 492kΩ × {6.5μA + (–0.0525 μA/°C) × (50°C – 25°C)}
= 9.15V ..... ⑦

V5 typ = (V5 max + V5 min) / 2
= (9.15V + 6.6V) / 2
= 7.9V ..... ⑧

- To set the number of variable voltage levels to 16, specify I_{REF} = 3.2µA.
- Margin calculation is performed by considering the dispersion of V_{REG} and V_{REF} according to the same procedure as (3). From this margin calculation, it is made clear that the center value of V5 is affected by variations of V_{REG} and I_{REF}.
- Accordingly, it is necessary to set the electronic contrast control register value to (D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0) or (0, 1, 1, 1, 1) and adjust the R_a value to the optimum contrast.
- The voltage step width by the electronic contrast control is changed by the dispersion of I_{REF}. It is necessary to consider that supposing that 0.2V/STEP is set by TYP value, the maximum variation of 0.12V to 0.28V occurs.



Example of V5 voltage when using SED1560 Series electronic contrast control

Since the I_{REF} is a simplified constant current source, when using the electronic contrast control function, it becomes necessary to make adjustment to the optimum contrast as given in the above item (4), with each of the IC chips, using the R_a as a variable resistor.

When not using the software contrast adjustment control function, set the register to (D3, D2, D1, D0) = (0, 0, 0, 0) using the $\overline{RES}$ signal or by means of the software contrast adjustment control register setting command.

4.26 LIQUID CRYSTAL VOLTAGE GENERATING CIRCUIT

A V5 potential is resistively divided within the IC to cause V1, V2, V3 and V4 potentials needed for driving of liquid crystals. The V1, V2, V3 and V4 potentials are further converted in the impedance by the voltage follower before being supplied to the liquid crystal driving circuit.

The liquid crystal driving voltage is fixed with each type (see Table 4.8).

As shown in Figure 4.13, it needs to connect, externally, 5 units of voltage stabilizing capacitors C2 to the liquid crystal power terminals. When selecting such capacitor C2, make actual liquid crystal displays matching to the display capacity of the liquid crystal display panel, before determining the capacitance as the constant value for voltage stabilization.

Table 4.8

Type	Liquid Crystal Driving Voltage
SED1560	1/9 of the bias voltage
SED1561	1/7 of the bias voltage
SED1562	1/5 of the bias voltage

Table 4.9 Reference Setting Value

Reference set values:

SED1560 ..... V5 ≈ –11 ~ –13V
SED1561 ..... V5 ≈ –7 ~ –9V
SED1562 ..... V5 ≈ –5 ~ –7V (Variable)

	SED1560	SED1561	SED1562
C1	0.47μF~	0.47μF~	0.47μF~
C2	1.0μF~	0.47μF~	0.47μF~
	1.0μF~	0.47μF~	0.47μF~
R1	1MΩ	700KΩ	500KΩ
R2	200KΩ	200KΩ	200KΩ
R3	4MΩ	1.6MΩ	700KΩ
LCD SIZE	32 × 51 mm	16 × 67 mm	8 × 75 mm
DOT	64 × 102	32 × 134	16 × 150

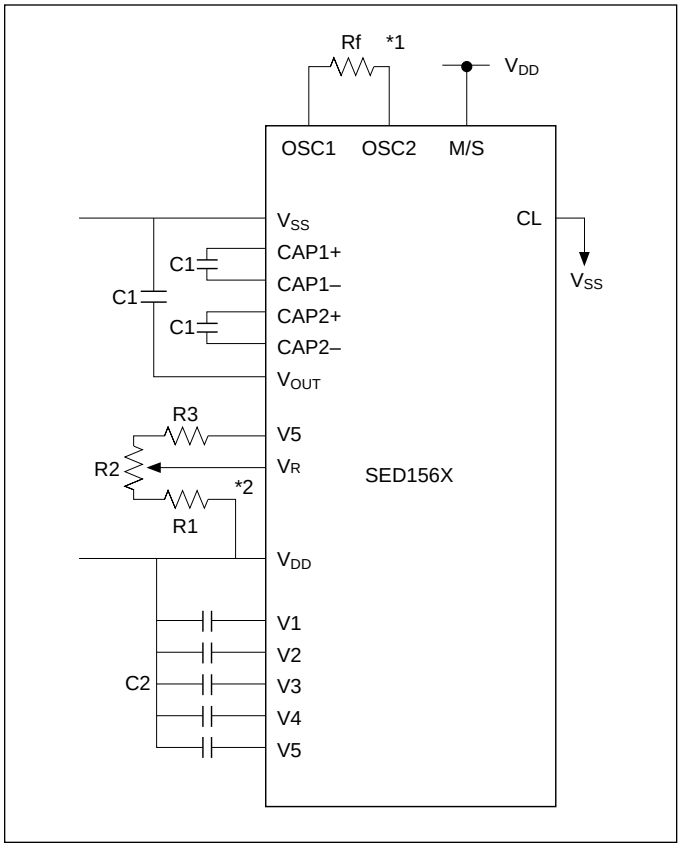


Figure 4.13
When the built-in power supply is used

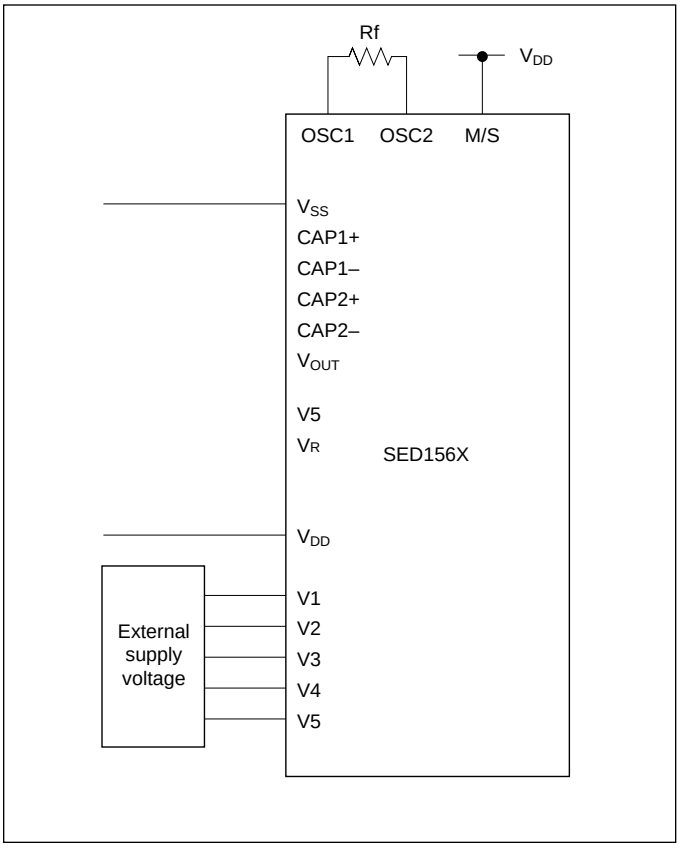


Figure 4.14
When external LCD power supply is used

*1 Connect oscillator feedback resistor R_f as short as possible and place it close to the IC for preventing a malfunction.

*2 Use short wiring or shielded cables for the V_R pin due to high input impedance.

*3 Determine C1 and C2 depending on the size of the LCD panel driven. You must set these values so that the LCD driving voltage becomes stable. Set (T1, T2) = (H, L) and supply an external voltage to V_{OUT}. Display the LCD heavy load pattern and determine C2 so that the LCD driving voltages (V1 to V5) become stable. However, it is necessary to make every C2 capacitance value equal. Then, set (T1, T2) = (L, L) and determine C1.

*4 The “LCD SIZE” indicates the vertical and horizontal length of the LCD panel display area.

4.27 RESET

When power is turned ON, the SED1560 Series is initialized on the rising edge of $\overline{RES}$. Initial settings are as follows:

1. Display : OFF
2. Display mode : Normal
3. *n*-line inversion : OFF
4. Duty cycle : 1/64
5. ADC select : Normal
6. Read/write modify : OFF
7. On-chip power supply : OFF
8. Serial interface register : Cleared
9. Display initial line register : Line 1
10. Column address counter : 0
11. Page address register : Page 0
12. Output selection circuit : Case 6
13. *n*-line inversion register : 16
14. Software contrast setting : zero

The $\overline{RES}$ pin should be connected to the microprocessor reset terminal so that both devices are reset at the same time. $\overline{RES}$ must be LOW for at least 1 μs to correctly reset the SED1560 Series. Normal operation starts 1 μs after the rising edge on $\overline{RES}$.

If the SED1560 Series is not properly initialized when power is turned ON, it can lock itself into a state that cannot be cancelled.

When the Reset command is used, only initial settings 9 to 14 are active.

5.0
Commands

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5.1 COMMAND SUMMARY

A0, $\overline{RD}$ and $\overline{WR}$ identify the data bus commands. Interpretation and execution of commands are synchronized to the internal clock. Since a busy check is normally not needed, commands can be processed at high speed. When the serial interface is used, the order of data entry is D7 to D0.

Table 5.1

Command	Code											Description
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OFF	0	1	0	1	0	1	0	1	1	1	D	Turns the display ON and OFF. D = 0 OFF D = 1 ON
Initial display line	0	1	0	0	1	Display line address						Sets the display RAM line address for COM0.
Page address set	0	1	0	1	0	1	1	Page address				Sets the RAM page address register.
Column address set (upper four bits)	0	1	0	0	0	0	1	Column address upper four bits				Sets the column address register upper four bits.
Column address set (lower four bits)	0	1	0	0	0	0	0	Column address lower four bits				Sets the column address register lower four bits.
Read status	0	0	1	Status				0	0	0	0	Reads out status information.
Write display data	1	1	0	Write data								Writes to display RAM.
Read display data	1	0	1	Read data								Reads from display RAM.
Select ADC	0	1	0	1	0	1	0	0	0	0	D	Sets the display RAM segment output. D = 0 Normal D = 1 Inverse
Normal/inverse display	0	1	0	1	0	1	0	0	1	1	D	Sets the LCD display mode. D = 0 Normal D = 1 Inverse
Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	D	Sets the segments display mode. D = 0 Normal D = 1 All display segments ON
Select duty	0	1	0	1	0	1	0	1	0	0	D	Sets the LCD controller duty (1). D = 0, D=1 See Table 5.3
Duty + 1	0	1	0	1	0	1	0	1	0	1	D	Sets the LCD controller duty (2). D = 0 Normal D = 1 Duty + 1
Set *n*-line inversion	0	1	0	0	0	1	1	Number of inverted items				Sets the number of inverted lines in the inversion register for the inversion controller.
Cancel *n*-line inversion	0	1	0	0	0	1	0	0	0	0	0	Cancels line inversion display mode.
Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Sets modified read mode. The column address counter is not incremented when reading.
End	0	1	0	1	1	1	0	1	1	1	0	Cancels modified read mode.
Power-on completion	0	1	0	1	1	1	0	1	1	0	1	Completes the turn-on sequence of built-in power supply
Reset	0	1	0	1	1	1	0	0	0	1	0	Resets the internal registers.
Output status set	0	1	0	1	1	0	0	Output status				Sets the common and segment output status register.
LCD power supply ON/OFF	0	1	0	0	0	1	0	0	1	0	D	Turns the power supply ON and OFF. D = 0 OFF D = 1 ON
Software contrast setting	0	1	0	1	0	0	Electronic contrast control resistance value					Setting the V5 output voltage to the electronic contrast control register.
Power save												A complex command to turn off the display and light all indicators.

5.2 COMMAND DEFINITIONS

5.2.1 Display ON/OFF

Alternately turns the display ON and OFF.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	0	1	0	1	1	1	D

Note:
D = 0 Display OFF
D = 1 Display ON

5.2.2 Initial Display Line

Loads the RAM line address of the initial display line, COM0, into the initial display line register. The RAM display data becomes the top line of the LCD screen. It is followed by the higher number lines in ascending order, corresponding to the duty cycle. The screen can be scrolled using this command by incrementing the line address.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	0	1	A5	A4	A3	A2	A1	A0

A5	A4	A3	A2	A1	A0	Line Address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
↓						↓
1	1	1	1	1	0	62
1	1	1	1	1	1	63

5.2.3 Page Address Set

Loads the RAM page address from the microprocessor into the page address register. A page address, along with a column address, defines a RAM location for writing or reading display data. When the page address is changed, the display status is not affected.

Page address 8 is a special use RAM area for the indicator. Only D0 is available for data exchange.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Page
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

5.2.4 Column Address Set

Loads the RAM column address from the microprocessor into the column address register. The column address is divided into two parts—4 high-order bits and 4 low-order bits.

When the microprocessor reads or writes display data to or from RAM, column addresses are automatically incremented, starting with the address stored in the column address register and ending with address 166.

The page address is not incremented automatically.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	0	0	0	1	A7	A6	A5	A4

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
↓								↓
1	0	1	0	0	1	0	1	165

5.2.5 Read Status

Indicates to the microprocessor the SED1560 Series status conditions.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	1	BUSY	ADC	ON/ OFF	RE- SET	0	0	0	0

- **BUSY** - Indicates whether or not the SED1560 Series will accept a command. If BUSY is 1, the device is currently executing a command or is resetting, and no new commands can be accepted. If BUSY is 0, a new command can be accepted. It is not necessary for the microprocessor to check the status of this bit if enough time is allowed for the last cycle to be completed.
- **ADC** - Indicates the relationship between RAM column addresses and the segment drivers. If ADC is 1, the relationship is normal and column address *n* corresponds to segment driver *n*. If ADC is 0, the relationship is inverted and column address (165 – *n*) corresponds to segment driver *n*.
- **ON/OFF** - Indicates whether the display is ON or OFF. If ON/OFF is 1, the display is OFF. If ON/OFF is 0, the display is ON. Note that this is the opposite of the Display ON/OFF command.
- **RESET** - Indicates whether initialization is in process as the result of RES or the Reset command.

5.2.6 Write Display Data

Writes bytes of display data from the microprocessor to the RAM location specified by the column address and page address registers. The column address is incremented automatically so that the microprocessor can continuously write data to the addressed page.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	1	0	Write data							

5.2.7 Read Display Data

Sends bytes of display data to the microprocessor from the RAM location specified by the column address and page address registers. The column address is incremented automatically so that the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register.

Display data cannot be read through the serial interface.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	0	1	Read data							

5.2.8 Select ADC

Selects the relationship between the RAM column addresses and the segment drivers. When reading or writing display data, the column address is incremented as shown in Figure 5.4.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	0	1	0	0	0	0	D

Note:

D = 0 Rotate right (normal direction)

D = 1 Rotate left (reverse direction)

The output pin relationship can also be changed by the microprocessor. There are very few restrictions on pin assignments when constructing an LCD module.

5.2.9 Normal/Inverse Display

Determines whether the data in RAM is displayed normally or inverted.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	0	1	0	0	1	1	D

Note:

D = 0 LCD segment is ON when RAM data is 1 (normal).

D = 1 LCD segment is ON when RAM data is 0 (inverse).

5.2.10 Display All Points ON/OFF

Turns all LCD points ON independently of the display data in RAM. The RAM contents are not changed.

This command has priority over the normal/inverse display command.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	0	1	0	0	1	0	D

Note:

D = 0 Normal display status

D = 1 All display segments ON

If this command is received when the display status is OFF, the Power Save command is executed.

5.2.11 Select Duty

Selects the LCD driver duty.

Since this is independent from the contents of the output status register, the duty must be selected according to the LCD output status.

In multi-chip configuration, the master and slave devices must have the same duty.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	0	1	0	1	0	0	D

Table 5.2

Model	D	Duty
SED1560	0	1/48
	1	1/64
SED1561	0	1/24
	1	1/32
SED1562	0	1/16
	1	1/16

5.2.12 Duty + 1

Increases the duty by 1. If 1/48 or 1/64 duty is selected in the SED1560, for example, 1/49 or 1/65 is set, respectively, and COM1 functions as either the COM48 or COM64 output. The display line always accesses the RAM area corresponding to page address 8, D0. (Refer to Figure 5.4.)

In multi-chip configuration, the Duty + 1 command must be executed to both the master and slave sides.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	0	1	0	1	0	1	D

Table 5.3

Model	D	Duty
SED1560	0	1/48 or 1/64
	1	1/49 or 1/65
SED1561	0	1/24 or 1/32
	1	1/25 or 1/33
SED1562	0	1/16
	1	1/17

5.2.13 Set *n*-line Inversion

Selects the number of inverse lines for the LCD AC controller. The value of *n* is set between 2 and 16 and is stored in the *n*-line inversion register.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	0	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Number of Inverted Lines
0	0	0	0	—
0	0	0	1	2
0	0	1	0	3
↓				↓
1	1	1	0	15
1	1	1	1	16

5.2.14 Cancel *n*-line Inversion

Cancels *n*-line inversion and restores the normal 2-frame AC control. The contents of the *n*-line inversion register are not changed.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	0	0	1	0	0	0	0	0

5.2.15 Modify Read

Following this command, the column address is no longer incremented automatically by a Read Display Data command. The column address is still incremented by the Write Display Data command. This mode is cancelled by the End command. The column address is then returned to its value prior to the Modify Read command. This command makes it easy to manage the duplication of data from a particular display area for features such as cursor blinking.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	1	1	0	0	0	0	0

Note: the Column Address Set command cannot be used in modify-read mode.

5.2.16 End

Cancels the modify read mode. The column address prior to the Modify Read command is restored.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	1	1	0	1	1	1	0

5.2.17 Reset

Resets the initial display line, column address, page address, and *n*-line inversion registers to their initial values. This command does not affect the display data in RAM.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	1	1	0	0	0	1	0

The reset command does not initialize the LCD power supply. Only hardware $\overline{RES}$ can be used to initialize the power supplies.

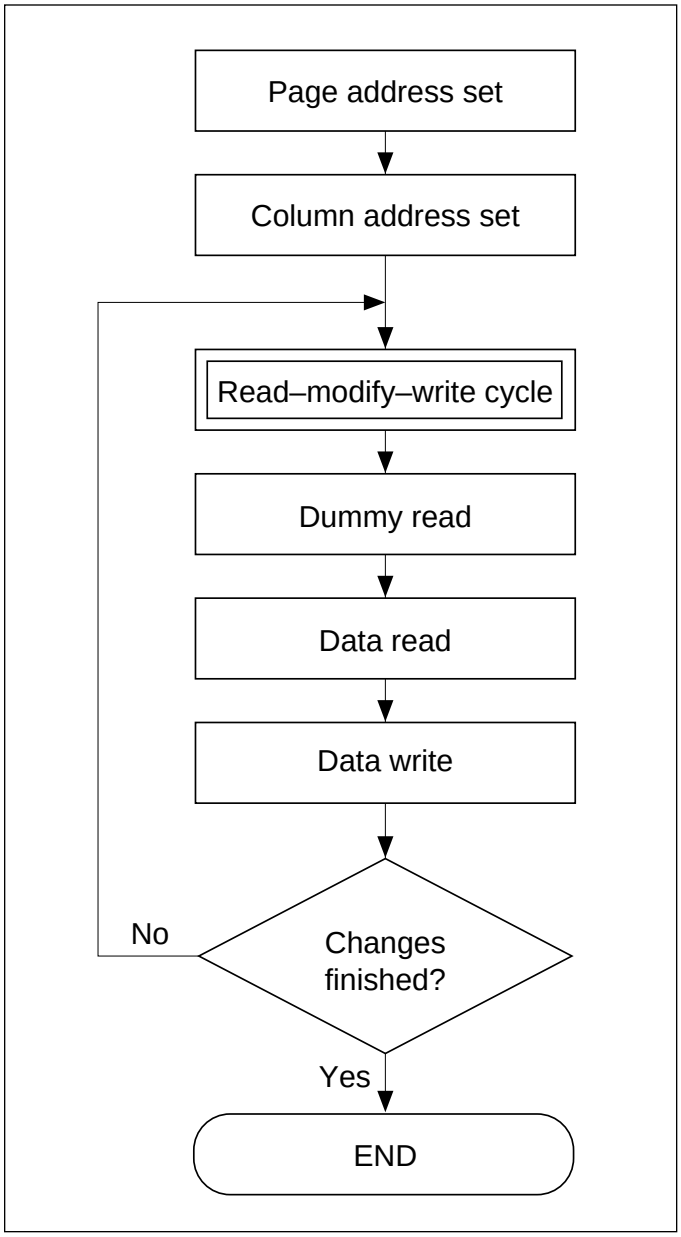


Figure 5.1
Command sequence for cursor blinking

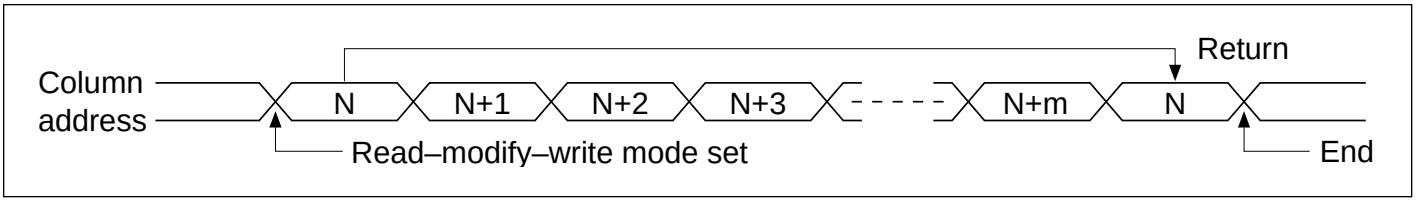


Figure 5.2

5.2.18 Output Status Set

Selects the common or segment output state of the LCD driver dual outputs. The A3 bit selects the scan direction of the outputs.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	1	0	0	A3	A2	A1	A0

5.2.19 Output Status Register

Available only in the SED1560 and SED1561.

This command selects the role of the COM/SEG dual pins and determines the LCD driver output status.

The COM output scanning direction can be selected by setting A3 to “H” or “L”. For details, refer to the Output Status Circuit in each function description.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	1	0	0	A3	A2	A1	A0

A3: Selection of the COM output scanning direction

Table 5.4

A2 A1 A0	**Output Status**	**Number of COM/SEG Output Pins**	**Remarks**
0 0 0	Case 6	SEG 166	Applies to the SED1560/61
0 0 1	Case 5	SEG 134, COM 32	Applies to the SED1561
0 1 0	Case 4	SEG 134, COM 32	
0 1 1	Case 3	SEG 134, COM 32	
1 0 0	Case 2	SEG 102, COM 64	Applies to the SED1560
1 0 1	Case 1	SEG 102, COM 64	
1 1 0	Case 6	SEG 166	Applies to the SED1560/61
1 1 1	Case 6	SEG 166	

5.2.20 LCD Power Supply ON/OFF

Turns the SED1560 Series LCD power supply ON or OFF. When the power supply is ON, the voltage converter, the voltage regulator circuit and the voltage followers are operating. In order for the converter to function, the oscillator must also be operating.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	0	0	1	0	0	1	0	0
					2			4		OFF

Note:

D = 0 Supply OFF (24H)

D = 1 Supply ON (25H)

When an external power supply is used with the SED1560 Series, the internal supply must be OFF.

If the SED1560 Series is used in a multiple-chip configuration, an external power supply that meets the specifications of the LCD panel must be used. An SED1560 Series operating as a slave must have its internal power supply turned OFF.

Sequence in the Built-In Power ON/OFF Status

To turn on internal power supply, execute the following built-in power supply ON sequence. To turn off internal power supply, execute the power save sequence as shown in the following power supply OFF status.

Accordingly, to turn on internal power supply again after turn it off (power save), execute the “Power Save Clear Sequence” that is described below.

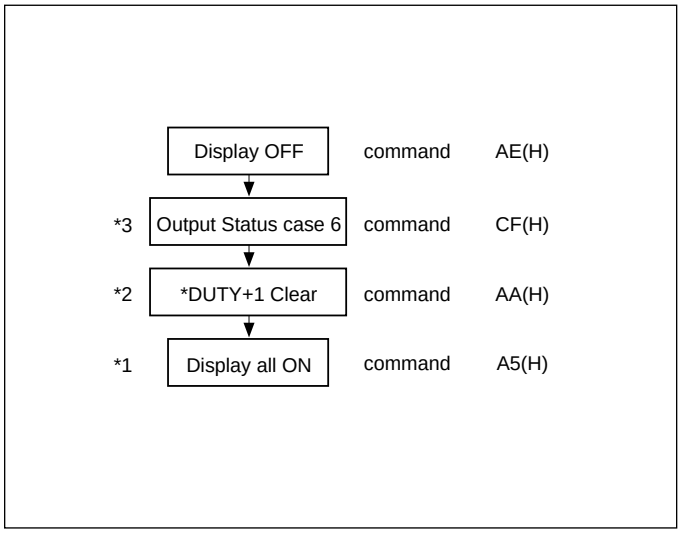
Sequence in the Power Save Status

Power Save and Power Save Clear must be executed according to the following sequence.

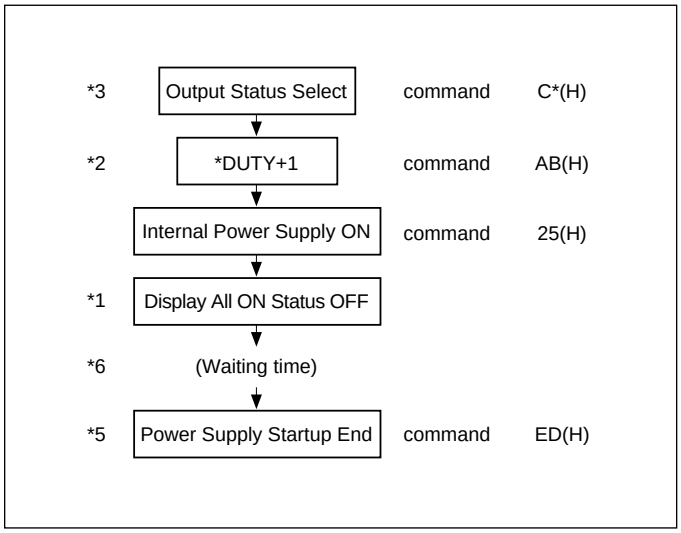
To give a liquid crystal driving voltage level by the externally-installed resistance dividing circuit, the current flowing in this resistance must be cut before or concurrently with putting the SED1560 Series into the power save status so that it may be fixed to the floating or V_{DD} level.

When using an external power supply, likewise, its function must be stopped before or concurrently with putting the SED1560 Series into the power save status so that it may be fixed to the floating or V_{DD} level. In a configuration in which an exclusive common driver such as SED1630 is combined with the SED1560 Series, it is necessary to stop the external power supply function after putting all the common output into non-selection level.

Power Save Sequence



Power Save Clear Sequence



*1. In the power save sequence, the power save status is provided after the display all ON command. In the power save clear sequence, the power save status is cleared after the display all ON status OFF command.

*2. When the COMI pin is not used, it is not necessary to enter the DUTY + 1 command and DUTY + 1 clear command.

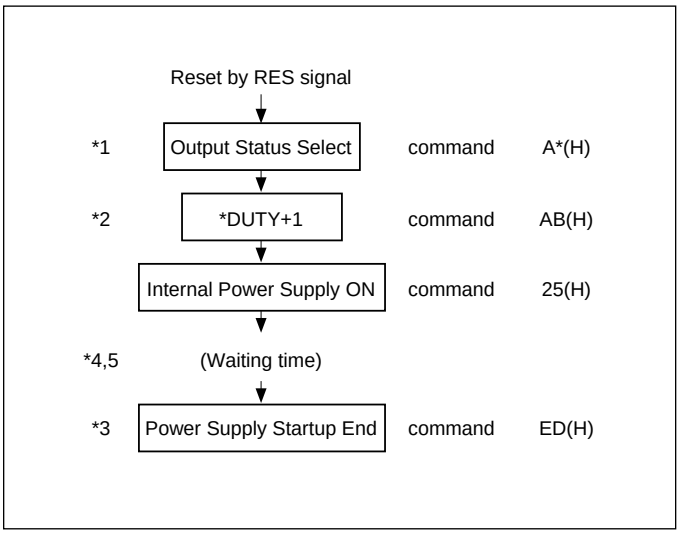
*3. In the SED1562, it is not necessary to execute a command to decide an output status.

*4. The display ON command can be executed anywhere if it is later than the display all ON status OFF command.

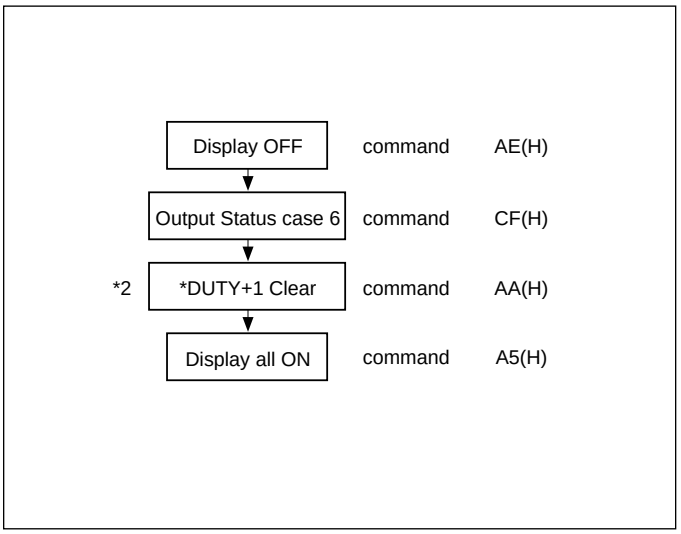
*5. When internal power supply startup end command is not executed, current is consumed stationarily. Internal power supply startup end command must always be used in a pair with internal power supply ON command.

*6. The waiting time depends on the externally-installed capacitance C2 (refer to Table 5.9). After the waiting time shown in the graph above (see bottom of previous page), the power supply can be started surely.

Internal Power Supply ON Status



Internal Power Supply OFF Status



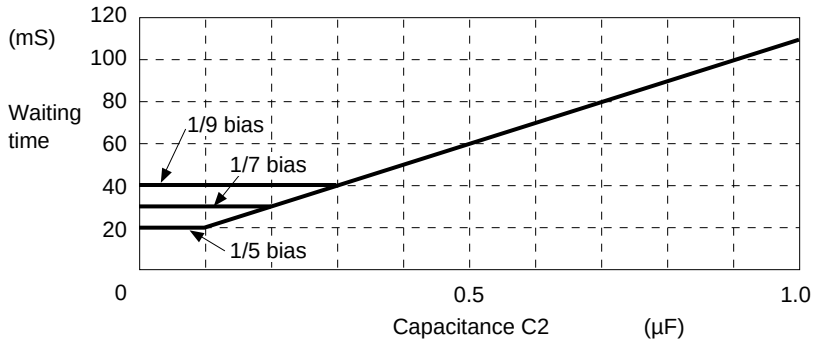
*1. Regarding the SED1562, it is not necessary to execute a command to decide an output status.

*2. When the COMI pin is not used, it is not necessary to enter the DUTY + 1 and DUTY + 1 Clear commands.

*3. When the built-in power supply startup end command is not executed, current is consumed stationarily. Internal power supply startup end command must always be used in a pair with internal power supply ON command.

*4. The waiting time depends on the externally-installed capacitance C2 (refer to Table 5.9). After the waiting time shown in the graph below, the power supply can be started surely.

*5. Within the waiting time in internal power supply ON status, any command other than internal power supply control commands such as Power Save, and display ON/OFF command, display normal rotation/reverse command, display all ON command, output status select command and DUTY + 1 clear command can accept another command without any problem. RAM read and write operations can be freely performed.



V5 voltage conditions
1/9 bias V5 = –6.0 to –16.0 V
1/7 bias V5 = –5.0 to –12.0 V
1/5 bias V5 = –4.5 to –8.0 V

5.3 SOFTWARE CONTRAST CONTROL REGISTER

Through these commands, the liquid crystal driving voltage V5 is output from the voltage regulation circuit of the built-in liquid crystal power supply, in order to adjust the contrast of the liquid crystal display.

By setting data to the 5-bit register, one of the 32 voltage statuses may be selected for the liquid crystal driving voltage V5. External resistors are used for setting the voltage regulation range of the V5. For details refer to the paragraph of the voltage regulation circuit in the clause for the explanation of functions.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	0	0	A4	A3	A2	A1	A0

A4	A3	A2	A1	A0	| V5 |
0	0	0	0	0	Small (as the absolute value)
↓					↓
1	1	1	1	1	Large (as the absolute value)

When not using the electronic contrast control function, set to (0, 0, 0, 0).

5.3.1 Power Save (Complex Command)

If the Display All Points ON command is specified in the display OFF state, the system enters the power save status, reducing the power consumption to approximate the static power consumption value. The internal state in the power save status is as follows:

(a) The oscillator and power supply circuits are stopped.

(b) The LCD driver is stopped and segment and common driver outputs output the V_{DD} level.

(c) An input of an external clock is inhibited and OSC2 enters the high-impedance state.

(d) The display data and operation mode before execution of the power save command are held.

(e) All LCD driver voltages are fixed to the V_{DD} level.

The power save mode is cancelled by entering either the Display ON command or the Display All Points OFF command (display operation state). When external voltage driver resistors are used to supply the LCD driver voltage level, the current through them must be cut off by the power save signal.

If an external power supply is used, it must be turned OFF using the power save signal in the same manner, and voltage levels must be fixed to the floating or V_{DD} level.

5.3.2 Connection between LCD Drivers

The LCD display area can be increased by using the SED1560 Series in a multiple-chip configuration or with the SED1560 Series special common driver (SED1630).

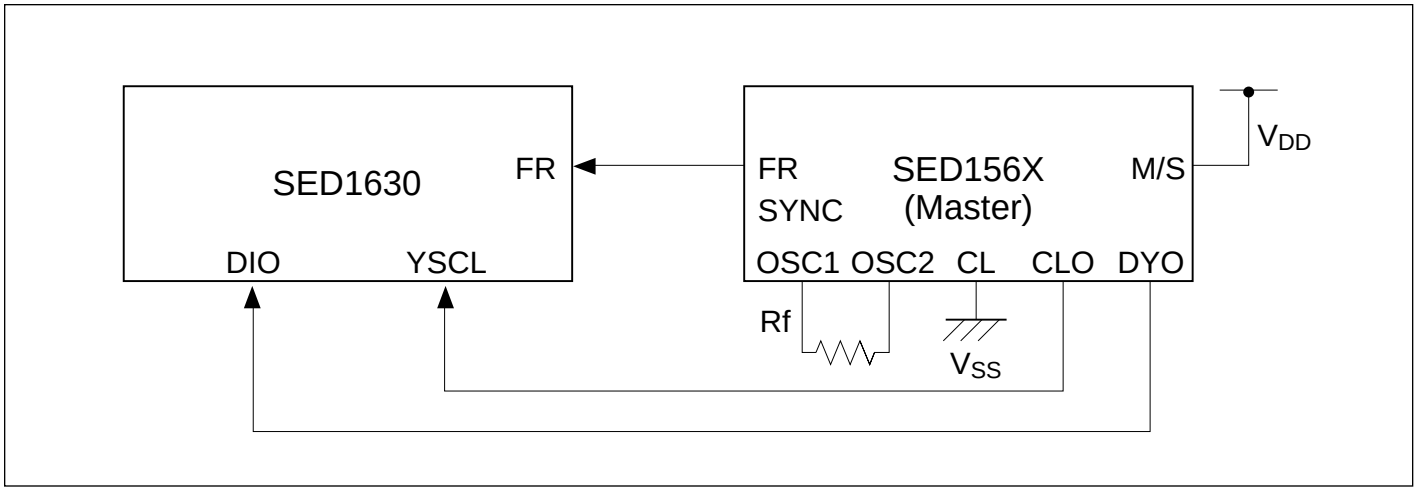


Figure 5.3 Application with external driver: SED156X – SED1630

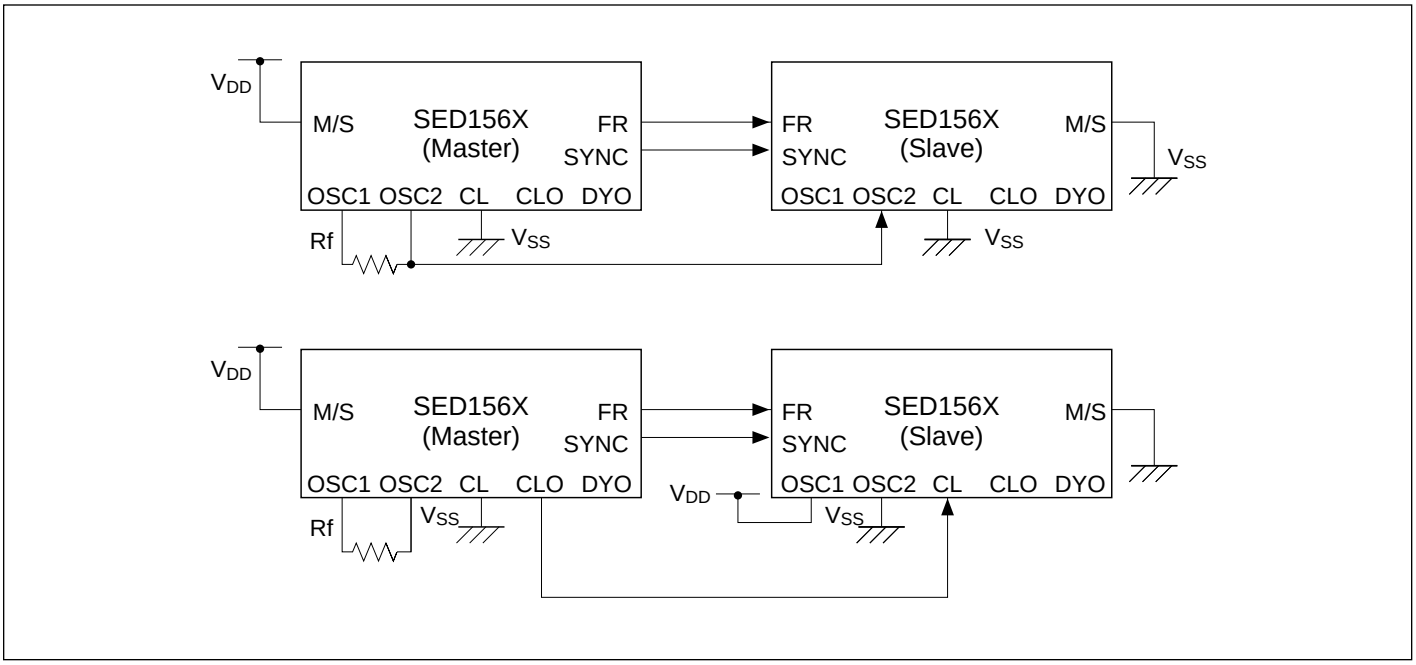


Figure 5.4 SED156X – SED156X (when oscillator circuit is used)

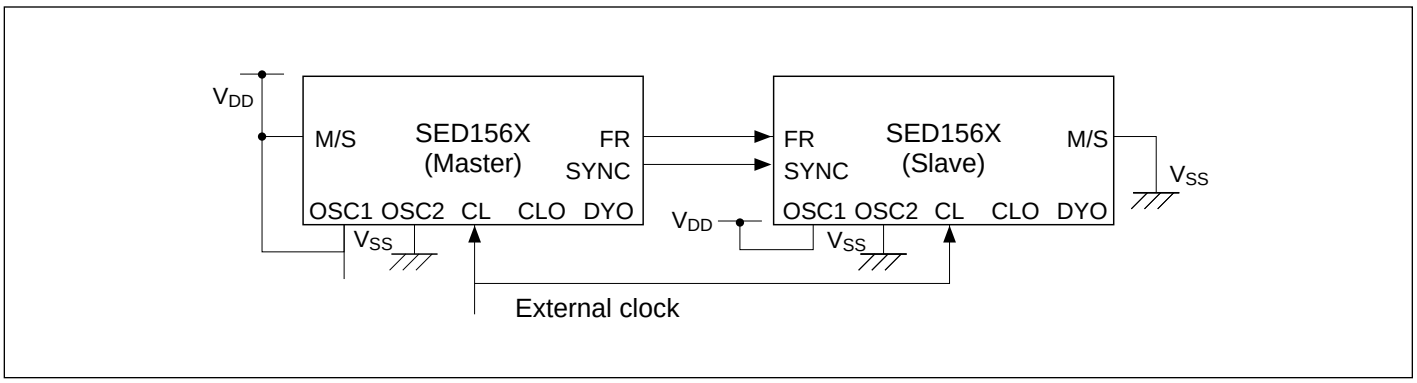


Figure 5.5 SED156X – SED156X (External clock)

5.4 MICROPROCESSOR INTERFACE

The SED1560 Series communicates with a high-speed microprocessor, such as the Intel 80XX family or the Motorola 68XX family, through 8-bit parallel data transfer. The number of connections to the microprocessor can be minimized by using a serial interface. When used in a multiple-chip configuration, the SED1560 Series is controlled by the chip select signals from the microprocessor.

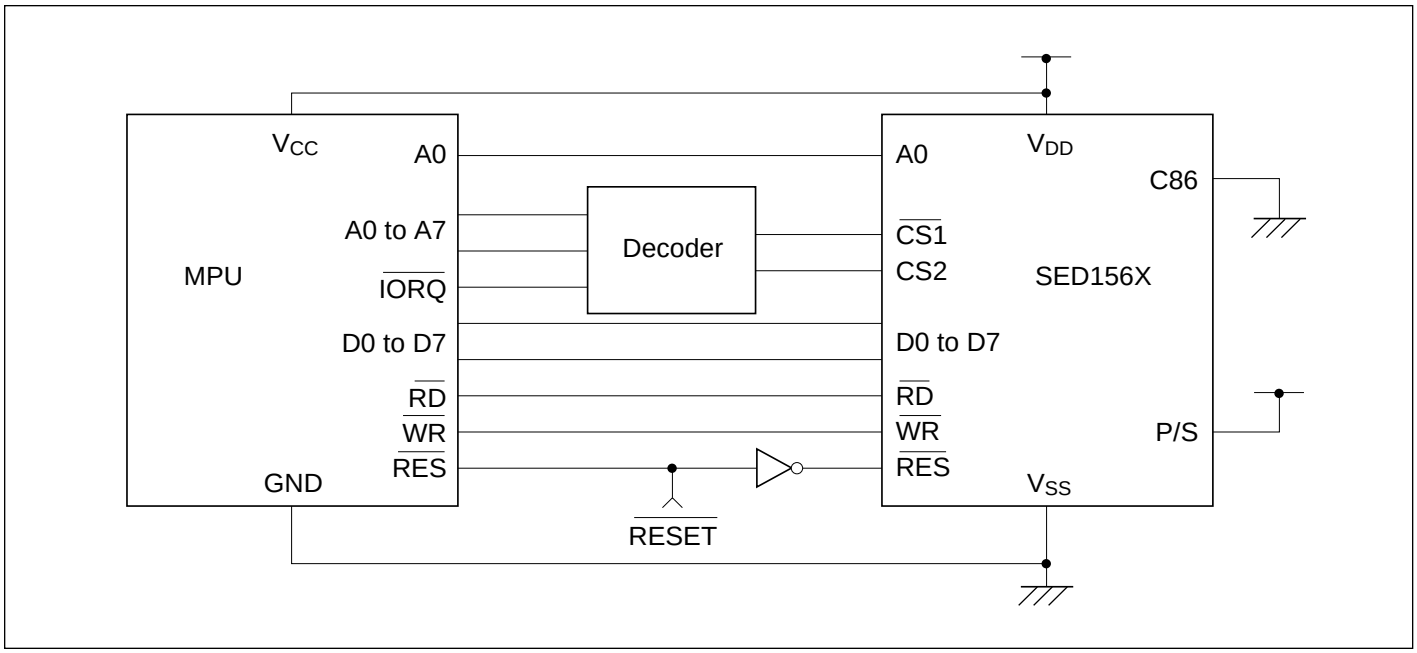


Figure 5.6 8080-series microprocessors

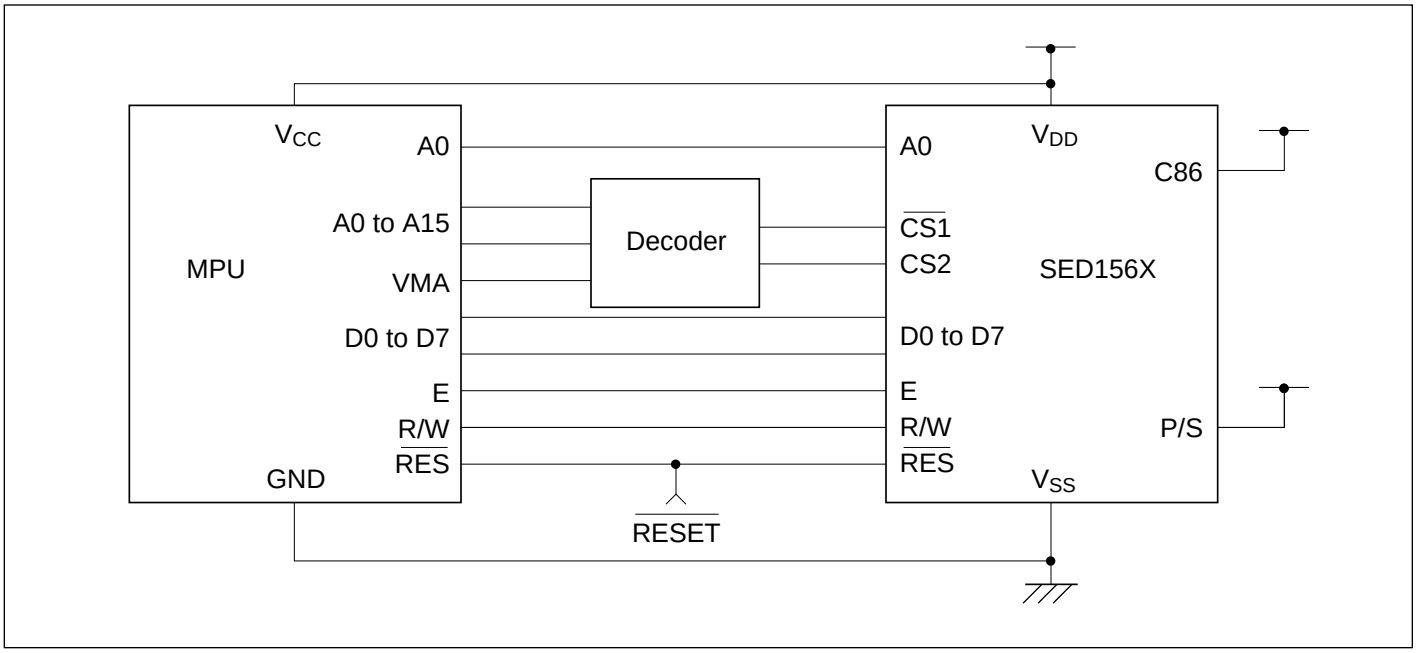


Figure 5.7 6800-series microprocessors

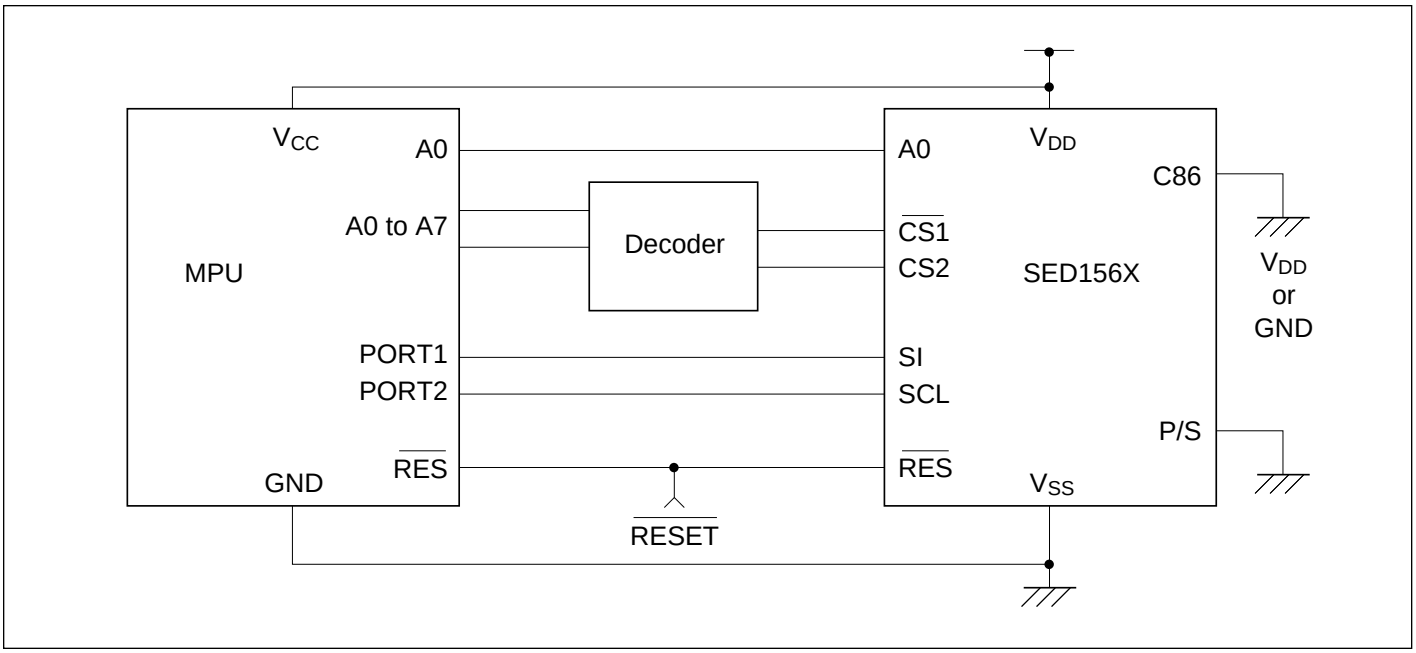


Figure 5.8 Serial interface

5.5 LCD PANEL INTERFACE EXAMPLES

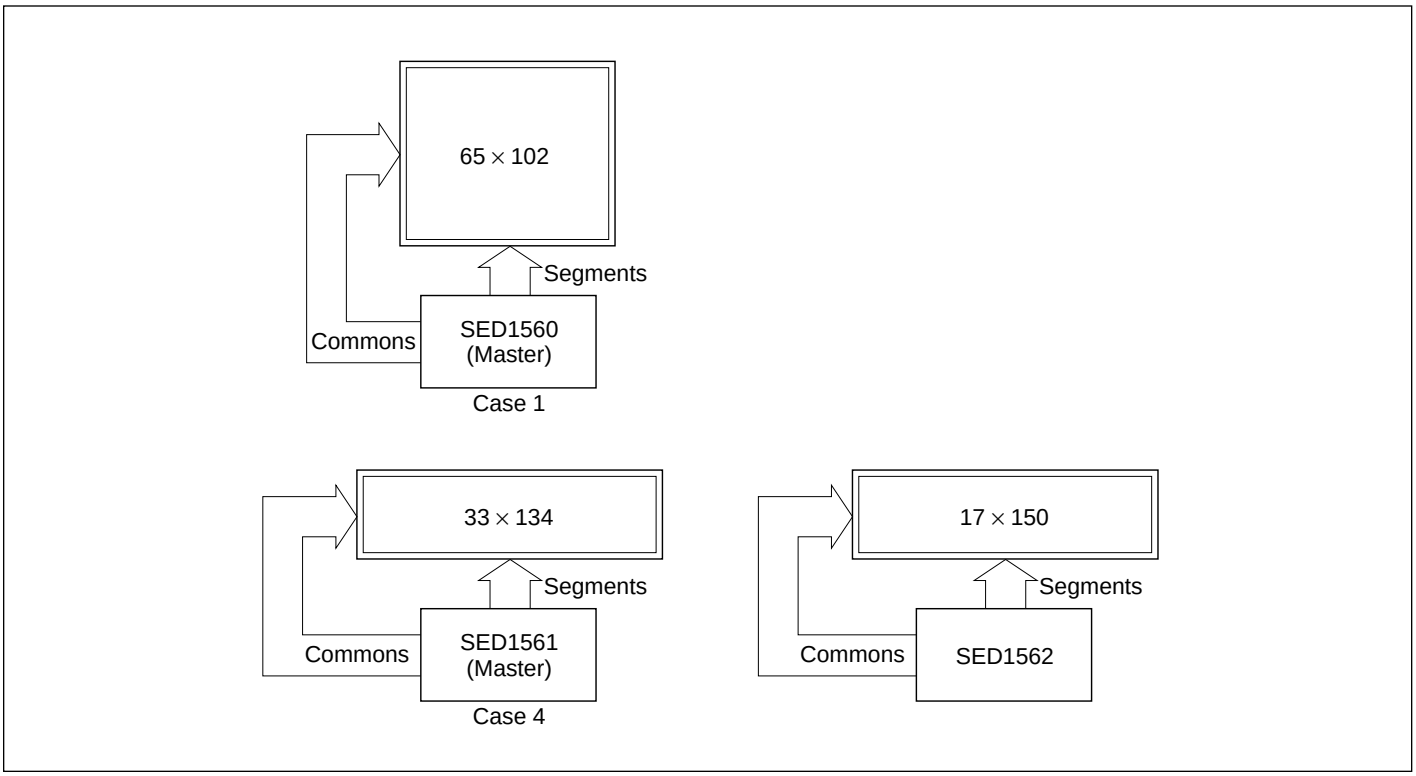


Figure 5.9 Single-chip configurations

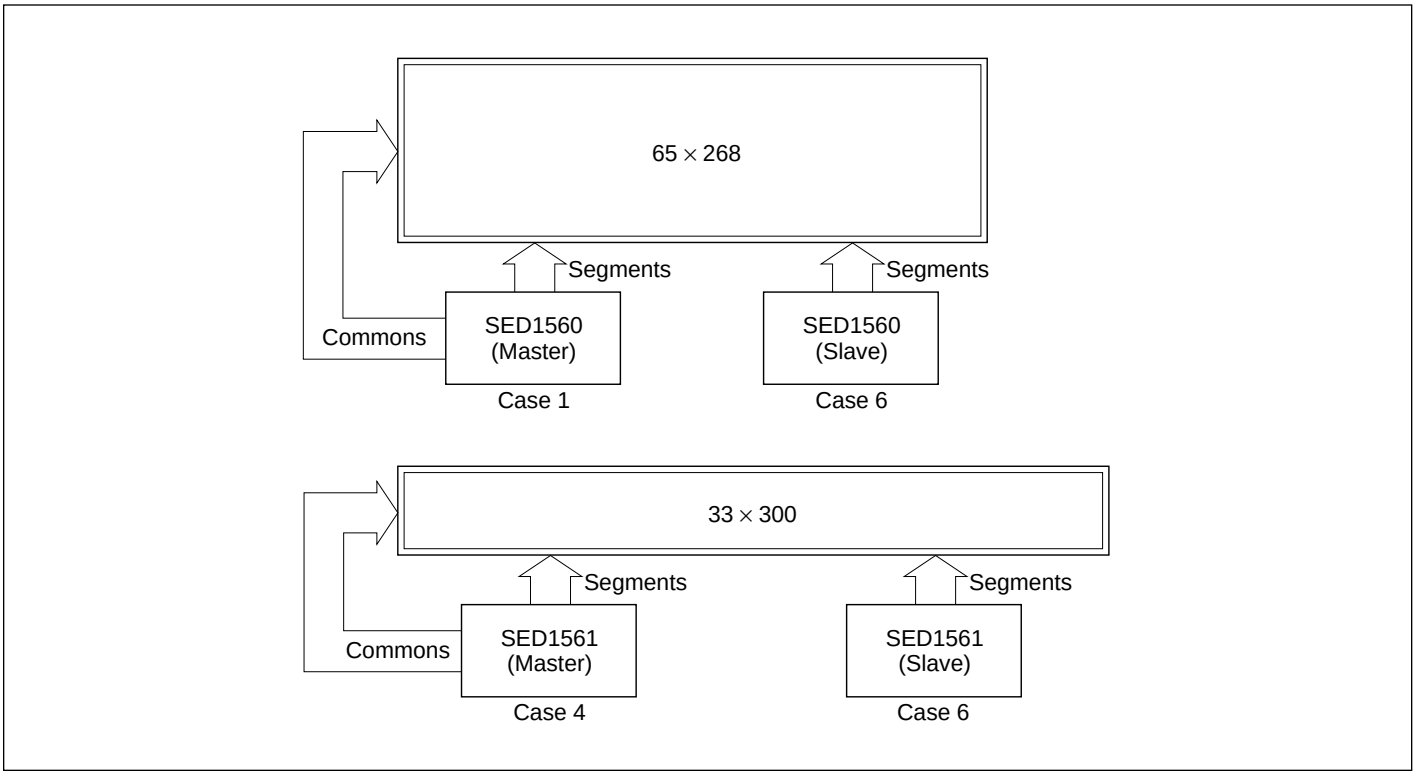


Figure 5.10 Multiple-chip combinations

5.6 SPECIAL COMMON DRIVER CONFIGURATIONS

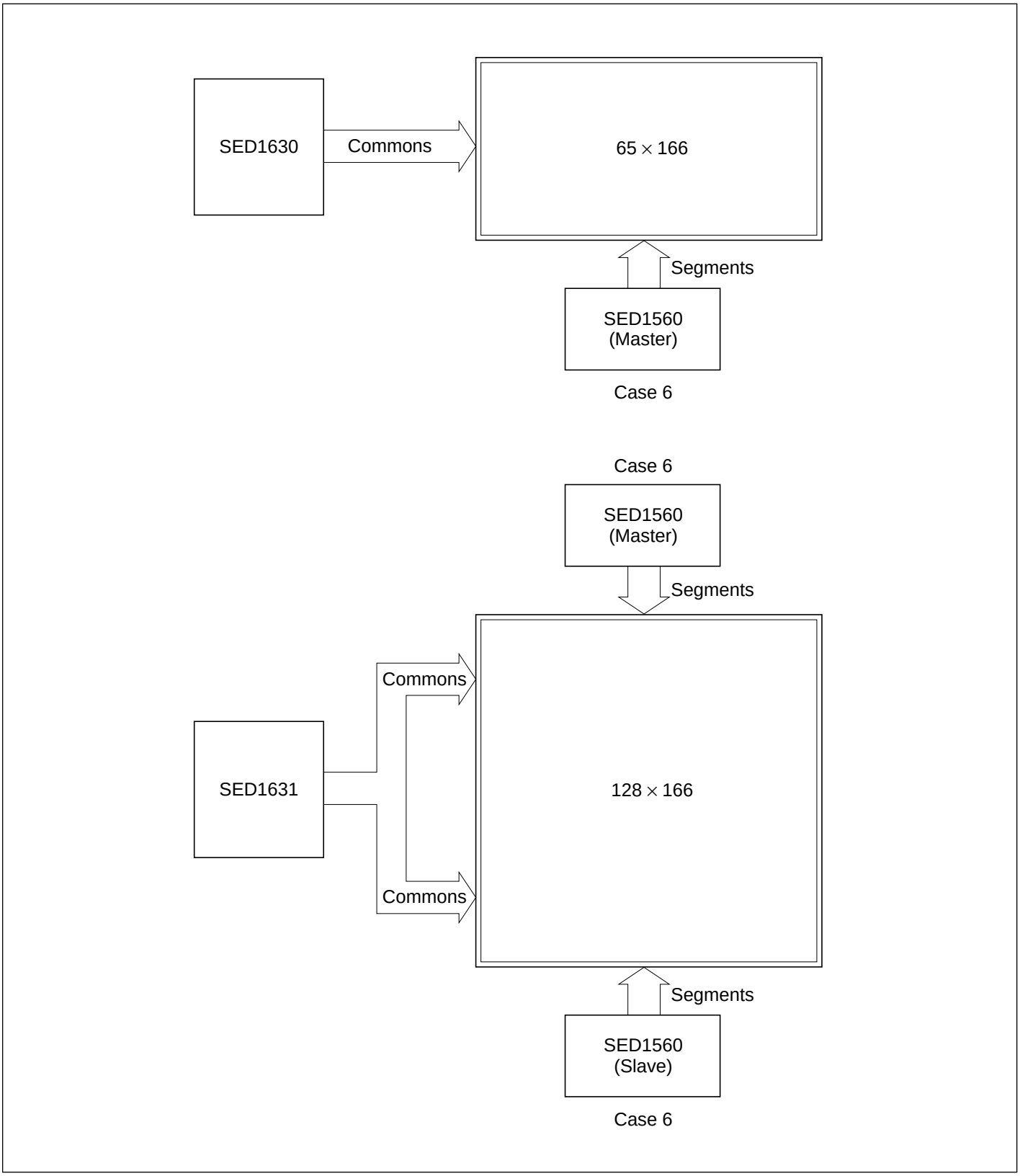


Figure 5.11 Special common driver configurations

6.0
Packaging

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6.1 PAD LAYOUT

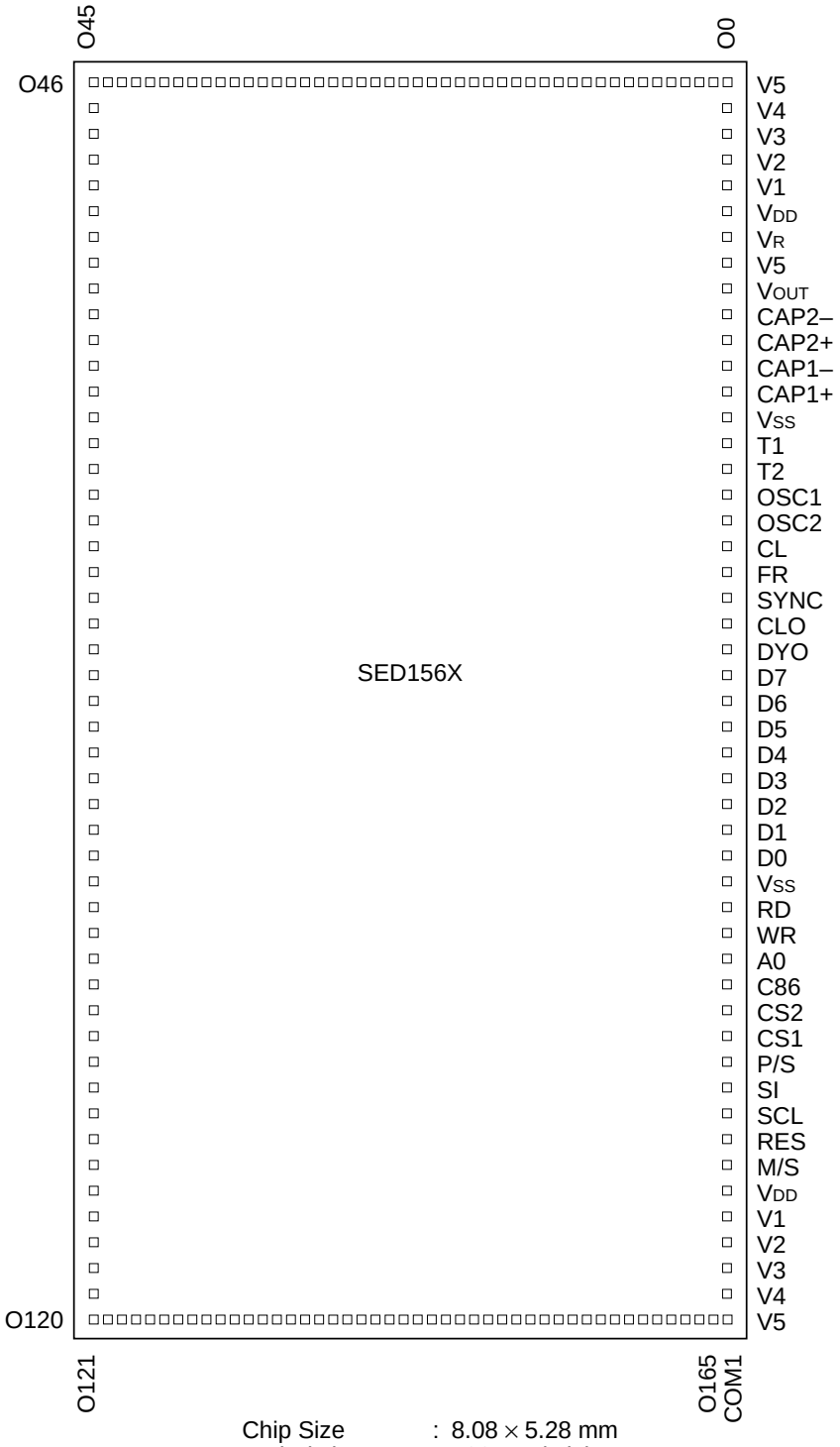


Figure 6.1 Pad layout

Table 6.1 SED1560 Series Pad Center Coordinates

Pad No.	Pin Name	X	Y
1	V5	3640	2487
2	V4	3489	2487
3	V3	3339	2487
4	V2	3188	2487
5	V1	3037	2487
6	V_{DD}	2889	2487
7	M/S	2755	2487
8	$\overline{RES}$	2604	2487
9	SCL	2453	2487
10	SI	2302	2487
11	P/S	2151	2487
12	$\overline{CS1}$	2001	2487
13	CS2	1850	2487
14	C86	1699	2487
15	A0	1548	2487
16	$\overline{WR}$	1397	2487
17	$\overline{RD}$	1247	2487
18	V_{SS}	1077	2487
19	D0	945	2487
20	D1	794	2487
21	D2	643	2487
22	D3	493	2487
23	D4	342	2487
24	D5	191	2487
25	D6	40	2487
26	D7	–111	2487
27	DYO	–261	2487
28	CLO	–412	2487
29	SYNC	–563	2487
30	FR	–714	2487
31	CL	–865	2487
32	OSC2	–1015	2487
33	OSC1	–1166	2487
34	T2	–1317	2487
35	T1	–1468	2487
36	V_{SS}	–1638	2487
37	CAP1+	–1789	2487
38	CAP1–	–1939	2487
39	CAP2+	–2090	2487
40	CAP2–	–2241	2487
41	V_{OUT}	–2392	2487
42	V5*	–2543	2487
43	VR	–2674	2487
44	V_{DD}	–2844	2487
45	V1	–2995	2487
46	V2	–3146	2487
47	V3	–3297	2487
48	V4	–3447	2487
49	V5	–3598	2487
50	O0	–3887	2294
51	O1	–3887	2194
52	O2	–3887	2094
53	O3	–3887	1994
54	O4	–3887	1894
55	O5	–3887	1794
56	O6	–3887	1694
57	O7	–3887	1594
58	O8	–3887	1494
59	O9	–3887	1394
60	O10	–3887	1294
61	O11	–3887	1194
62	O12	–3887	1094
63	O13	–3887	994
64	O14	–3887	894
65	O15	–3887	794
66	O16	–3887	694
67	O17	–3887	594
68	O18	–3887	494
69	O19	–3887	394
70	O20	–3887	294
71	O21	–3887	194
72	O22	–3887	94
73	O23	–3887	–6
74	O24	–3887	–106
75	O25	–3887	–206
76	O26	–3887	–306
77	O27	–3887	–406
78	O28	–3887	–506
79	O29	–3887	–606
80	O30	–3887	–706
81	O31	–3887	–806
82	O32	–3887	–906
83	O33	–3887	–1006
84	O34	–3887	–1106
85	O35	–3887	–1206
86	O36	–3887	–1306
87	O37	–3887	–1406
88	O38	–3887	–1506
89	O39	–3887	–1606
90	O40	–3887	–1706
91	O41	–3887	–1806
92	O42	–3887	–1906
93	O43	–3887	–2006
94	O44	–3887	–2106
95	O45	–3887	–2206
96	O46	–3711	–2487
97	O47	–3611	–2487
98	O48	–3511	–2487
99	O49	–3411	–2487
100	O50	–3311	–2487
101	O51	–3211	–2487
102	O52	–3111	–2487
103	O53	–3011	–2487
104	O54	–2911	–2487
105	O55	–2811	–2487
106	O56	–2711	–2487
107	O57	–2611	–2487
108	O58	–2511	–2487
109	O59	–2411	–2487
110	O60	–2311	–2487
111	O61	–2211	–2487
112	O62	–2111	–2487
113	O63	–2011	–2487
114	O64	–1911	–2487
115	O65	–1811	–2487
116	O66	–1711	–2487
117	O67	–1611	–2487
118	O68	–1511	–2487
119	O69	–1411	–2487
120	O70	–1311	–2487
121	O71	–1211	–2487
122	O72	–1111	–2487
123	O73	–1011	–2487
124	O74	–911	–2487
125	O75	–811	–2487
126	O76	–711	–2487
127	O77	–611	–2487
128	O78	–511	–2487
129	O79	–411	–2487
130	O80	–311	–2487
131	O81	–211	–2487
132	O82	–111	–2487
133	O83	–11	–2487
134	O84	89	–2487
135	O85	189	–2487
136	O86	289	–2487
137	O87	389	–2487
138	O88	489	–2487
139	O89	589	–2487
140	O90	689	–2487
141	O91	789	–2487
142	O92	889	–2487
143	O93	989	–2487
144	O94	1089	–2487
145	O95	1189	–2487
146	O96	1289	–2487
147	O97	1389	–2487
148	O98	1489	–2487
149	O99	1589	–2487
150	O100	1689	–2487
151	O101	1789	–2487
152	O102	1889	–2487
153	O103	1989	–2487
154	O104	2089	–2487
155	O105	2189	–2487
156	O106	2289	–2487
157	O107	2389	–2487
158	O108	2489	–2487
159	O109	2589	–2487
160	O110	2689	–2487
161	O111	2789	–2487
162	O112	2889	–2487
163	O113	2989	–2487
164	O114	3089	–2487
165	O115	3189	–2487
166	O116	3289	–2487
167	O117	3389	–2487
168	O118	3489	–2487
169	O119	3589	–2487
170	O120	3689	–2487
171	O121	3887	–2206
172	O122	3887	–2106
173	O123	3887	–2006
174	O124	3887	–1906
175	O125	3887	–1806
176	O126	3887	–1706
177	O127	3887	–1606
178	O128	3887	–1506
179	O129	3887	–1406
180	O130	3887	–1306
181	O131	3887	–1206
182	O132	3887	–1106
183	O133	3887	–1006
184	O134	3887	–906
185	O135	3887	–806
186	O136	3887	–706
187	O137	3887	–606
188	O138	3887	–506
189	O139	3887	–406
190	O140	3887	–306
191	O141	3887	–206
192	O142	3887	–106
193	O143	3887	–6
194	O144	3887	94
195	O145	3887	194
196	O146	3887	294
197	O147	3887	394
198	O148	3887	494
199	O149	3887	594
200	O150	3887	694
201	O151	3887	794
202	O152	3887	894
203	O153	3887	994
204	O154	3887	1094
205	O155	3887	1194
206	O156	3887	1294
207	O157	3887	1394
208	O158	3887	1494
209	O159	3887	1594
210	O160	3887	1694
211	O161	3887	1794
212	O162	3887	1894
213	O163	3887	1994
214	O164	3887	2094
215	O165	3887	2194
216	COMI	3887	2294

* One V5 output is used for the LCD driver supply voltage; the other is used for the electronic volume control.

6.2 SED1560/1/2 TAB PIN LAYOUT

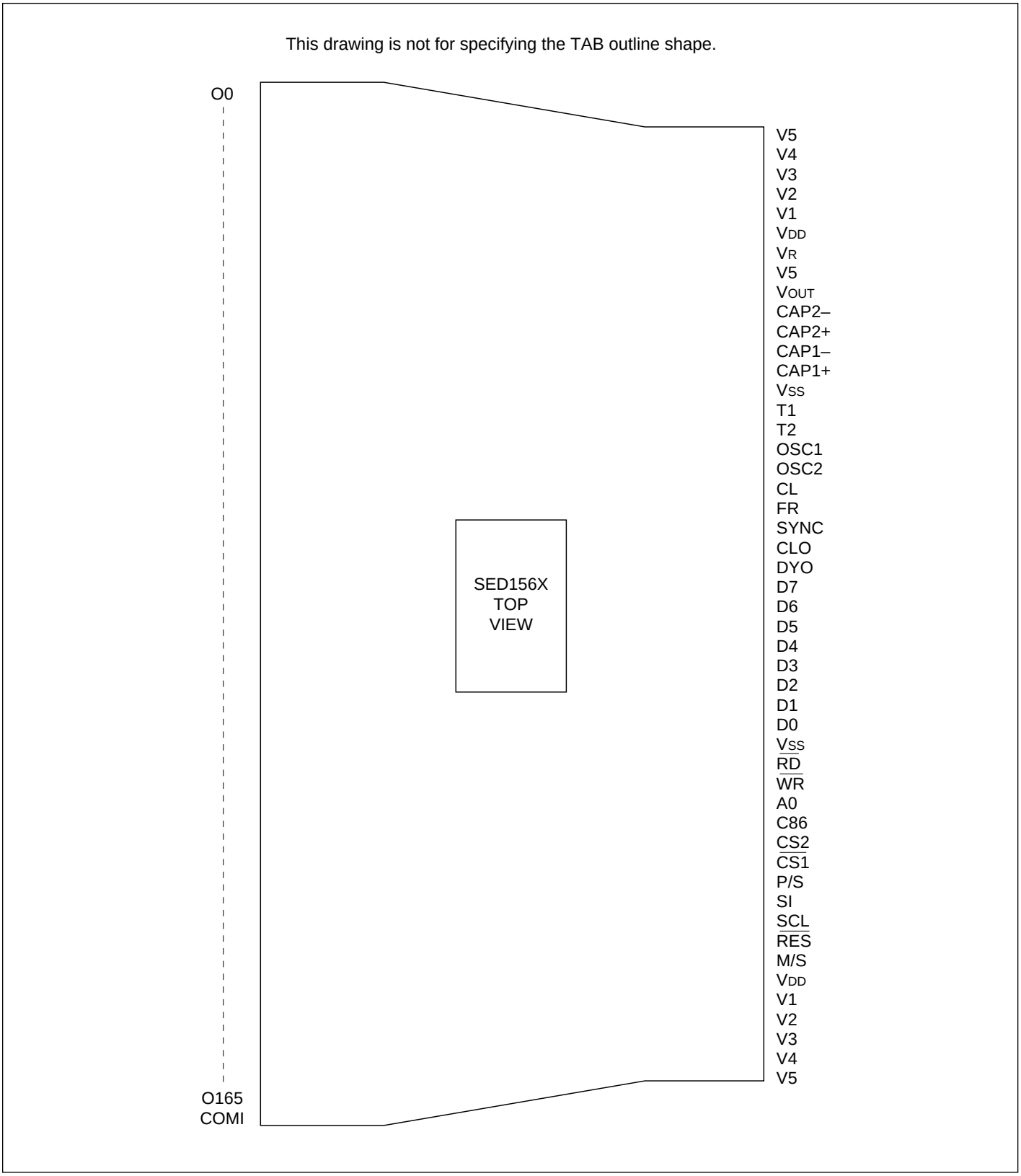
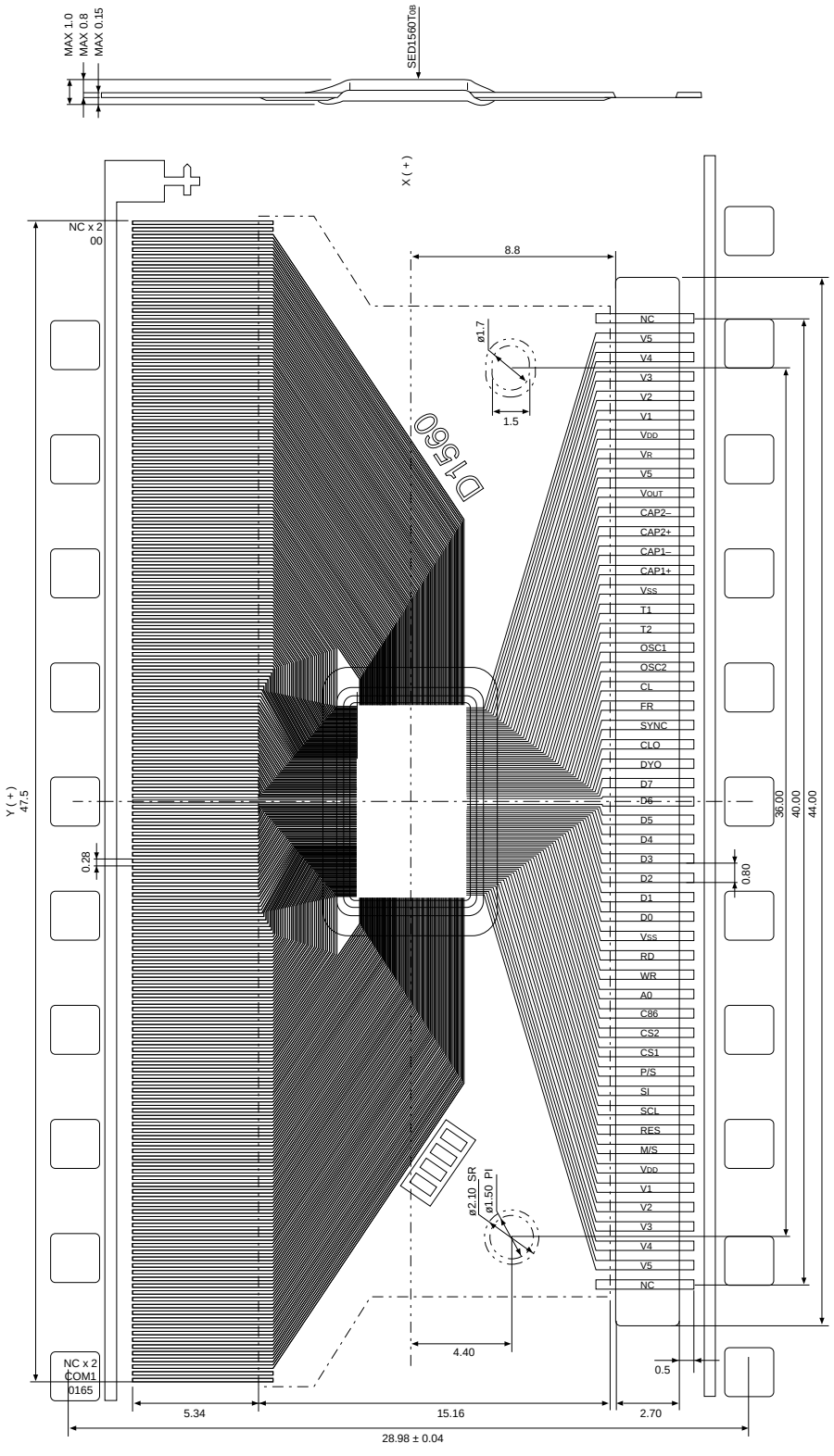


Figure 6.2 SED1560 Series TAB pin layout

6.3 TCP DIMENSIONS (2-SIDED) SED156XT0B



Note 1: Resist position tolerance: ±0.3
2: Product pitch: 52.25mm

Figure 6.3 TCP dimensions (2-sided)

6.4 TCP DIMENSIONS (4-SIDED) SED156XT0A

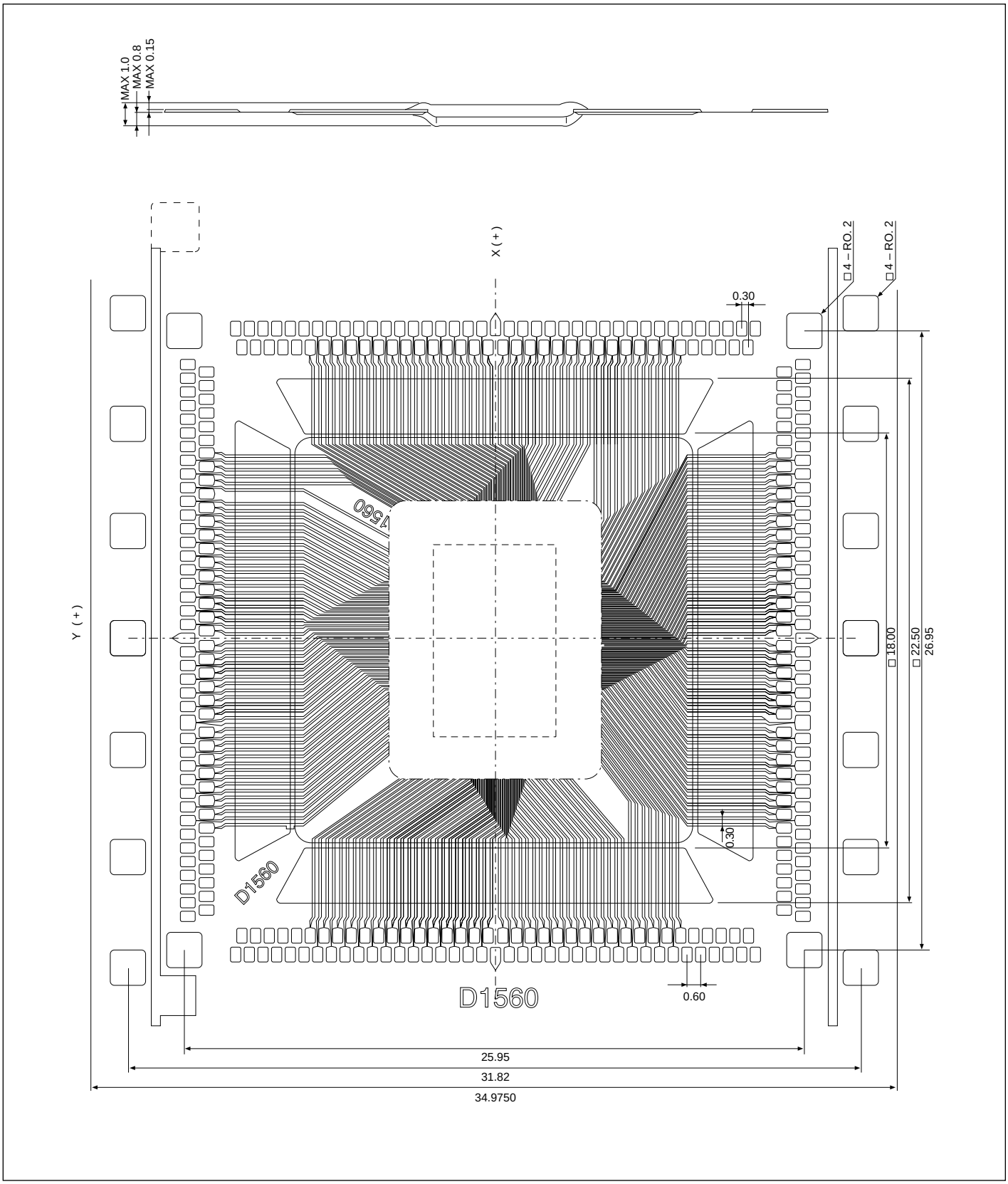


Figure 6.4 TCP dimensions (4-sided)

6.5 TCP DIMENSIONS (SED1561TOC)

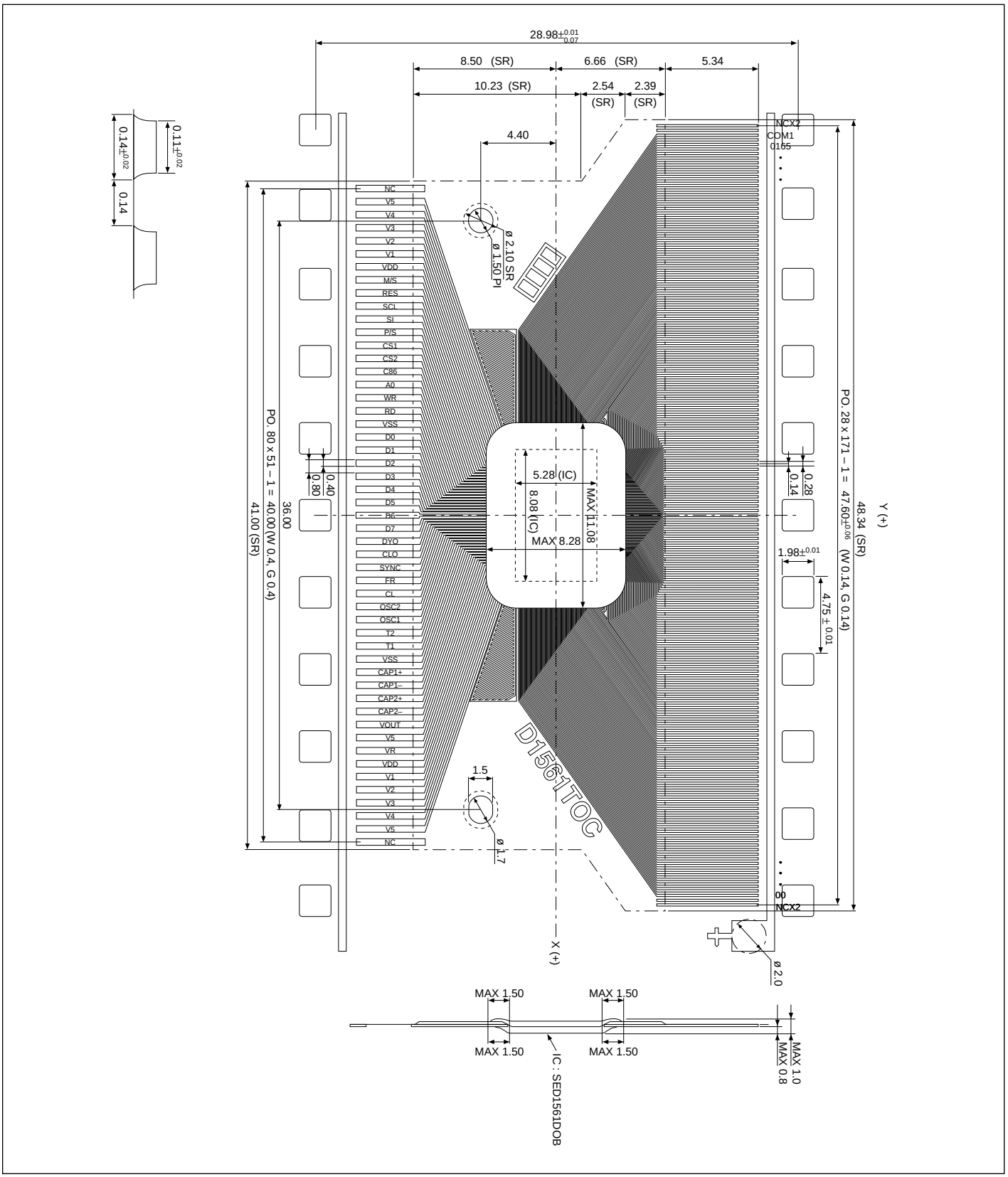


Figure 6.5 TCP dimensions (D1561TOC)

6.6 PAD PROFILE

TBD

6.7 BGA PACKAGE DIMENSIONS

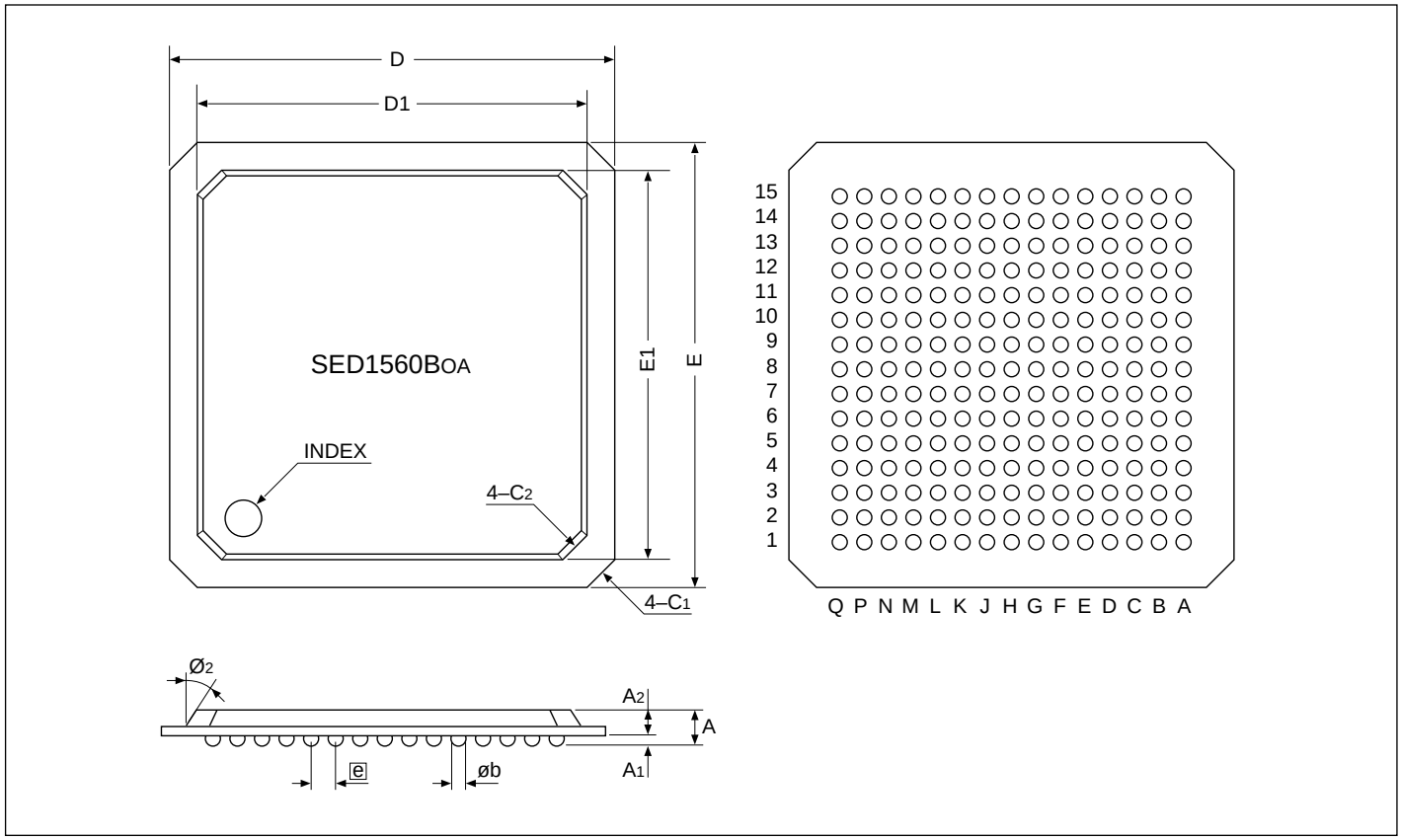


Figure 6.7 Plastic BGA 225pin

Table 6.2 BGA 225pin package dimensions

Symbol	Dimension in Millimeters			Dimension in inches*		
	Min.	Nom.	Max.	Min.	Nom.	Max.
øb	0.6	0.75	0.90	(0.024)	(0.030)	(0.035)
A		2.13			(0.084)	
A1	0.5	0.6	0.7	(0.020)	(0.024)	(0.027)
A2	1.43	1.53	1.63	(0.057)	(0.060)	(0.064)
θ2		25°			(25°)	
C1		1.5			(0.059)	
C2		1.2			(0.047)	
e		1.5			(0.059)	
D1	23.9	24	24.1	(0.941)	(0.945)	(0.948)
E1	23.9	24	24.1	(0.941)	(0.945)	(0.948)
D		27			(1.063)	
E		27			(1.063)	

* for reference

6.8 BGA PIN ASSIGNMENT

SED1560 pad#	SED1560 pin name	BGA225 pin#	SED1560 pad#	SED1560 pin name	BGA225 pin#	SED1560 pad#	SED1560 pin name	BGA225 pin#	SED1560 pad#	SED1560 pin name	BGA225 pin#	N/C
1	V5	B-2	55	05	R-2	109	059	K-10	163	0113	D-12	J-7
2	V4	D-4	56	06	P-3	110	060	M-13	164	0114	B-14	H-7
3	V3	B-1	57	07	K-6	111	061	N-15	165	0115	A-15	G-7
4	V2	C-2	58	08	N-4	112	062	M-14	166	0116	C-13	J-8
5	V1	F-6	59	09	R-3	113	063	J-10	167	0117	A-14	H-8
6	VDD	D-3	60	010	P-4	114	064	L-12	168	0118	B-13	G-8
7	M/S	C-1	61	011	K-7	115	065	M-15	169	0119	E-11	J-9
8	/RES	D-2	62	012	M-5	116	066	L-13	170	0120	C-12	H-9
9	SCL	G-6	63	013	R-4	117	067	L-14	171	0121	A-13	G-9
10	SI	E-4	64	014	N-5	118	068	K-11	172	0122	B-12	
11	P/S	D-1	65	015	P-5	119	069	L-15	173	0123	F-9	
12	/CS1	E-3	66	016	L-6	120	070	K-12	174	0124	D-11	
13	CS2	E-2	67	017	R-5	121	071	K-13	175	0125	A-12	
14	C86	F-5	68	018	M-6	122	072	K-14	176	0126	C-11	
15	A0	E-1	69	019	N-6	123	073	K-15	177	0127	B-11	
16	/WR	F-4	70	020	P-6	124	074	J-12	178	0128	E-10	
17	/RD	F-3	71	021	R-6	125	075	J-13	179	0129	A-11	
18	VSS	F-2	72	022	M-7	126	076	J-14	180	0130	D-10	
19	D0	F-1	73	023	N-7	127	077	J-15	181	0131	C-10	
20	D1	G-4	74	024	P-7	128	078	J-11	182	0132	B-10	
21	D2	G-3	75	025	R-7	129	079	L-8	183	0133	A-10	
22	D3	G-2	76	026	L-7	130	080	K-8	184	0134	D-9	
23	D4	G-1	77	027	M-8	131	081	H-10	185	0135	C-9	
24	D5	G-5	78	028	P-8	132	082	H-11	186	0136	B-9	
25	D6	H-3	79	029	R-8	133	083	H-6	187	0137	A-9	
26	D7	H-1	80	030	N-8	134	084	H-5	188	0138	E-9	
27	DYO	H-2	81	031	L-9	135	085	F-8	189	0139	D-8	
28	CLO	H-4	82	032	R-9	136	086	E-8	190	0140	B-8	
29	SYNC	J-5	83	033	P-9	137	087	H-12	191	0141	A-8	
30	FR	J-1	84	034	N-9	138	088	H-14	192	0142	C-8	
31	CL	J-2	85	035	M-9	139	089	H-15	193	0143	E-7	
32	OSC2	J-3	86	036	R-10	140	090	H-13	194	0144	A-7	
33	OSC1	J-4	87	037	P-10	141	091	G-11	195	0145	B-7	
34	T2	K-1	88	038	N-10	142	092	G-15	196	0146	C-7	
35	T1	K-2	89	039	M-10	143	093	G-14	197	0147	D-7	
36	VSS	K-3	90	040	R-11	144	094	G-13	198	0148	A-6	
37	CAP1+	K-4	91	041	L-10	145	095	G-12	199	0149	B-6	
38	CAP1–	L-1	92	042	P-11	146	096	F-15	200	0150	C-6	
39	CAP2+	K-5	93	043	N-11	147	097	F-14	201	0151	D-6	
40	CAP2–	L-2	94	044	R-12	148	098	F-13	202	0152	A-5	
41	VOUT	L-3	95	045	M-11	149	099	F-12	203	0153	E-6	
42	V5	M-1	96	046	K-9	150	0100	E-15	204	0154	B-5	
43	VR	L-4	97	047	P-12	151	0101	F-11	205	0155	C-5	
44	VDD	J-6	98	048	R-13	152	0102	E-14	206	0156	A-4	
45	V1	M-2	99	049	N-12	153	0103	E-13	207	0157	D-5	
46	V2	N-1	100	050	L-11	154	0104	D-15	208	0158	F-7	
47	V3	M-3	101	051	P-13	155	0105	E-12	209	0159	B-4	
48	V4	L-5	102	052	R-14	156	0106	G-10	210	0160	A-3	
49	V5	N-2	103	053	N-13	157	0107	D-14	211	0161	C-4	
50	00	P-1	104	054	R-15	158	0108	C-15	212	0162	E-5	
51	01	N-3	105	055	P-14	159	0109	D-13	213	0163	B-3	
52	02	R-1	106	056	M-12	160	0110	F-10	214	0164	A-2	
53	03	P-2	107	057	P-15	161	0111	C-14	215	0165	C-3	
54	04	M-4	108	058	N-14	162	0112	B-15	216	COMI	A-1	

6.9 SED1560TQA OL DIMENSIONS

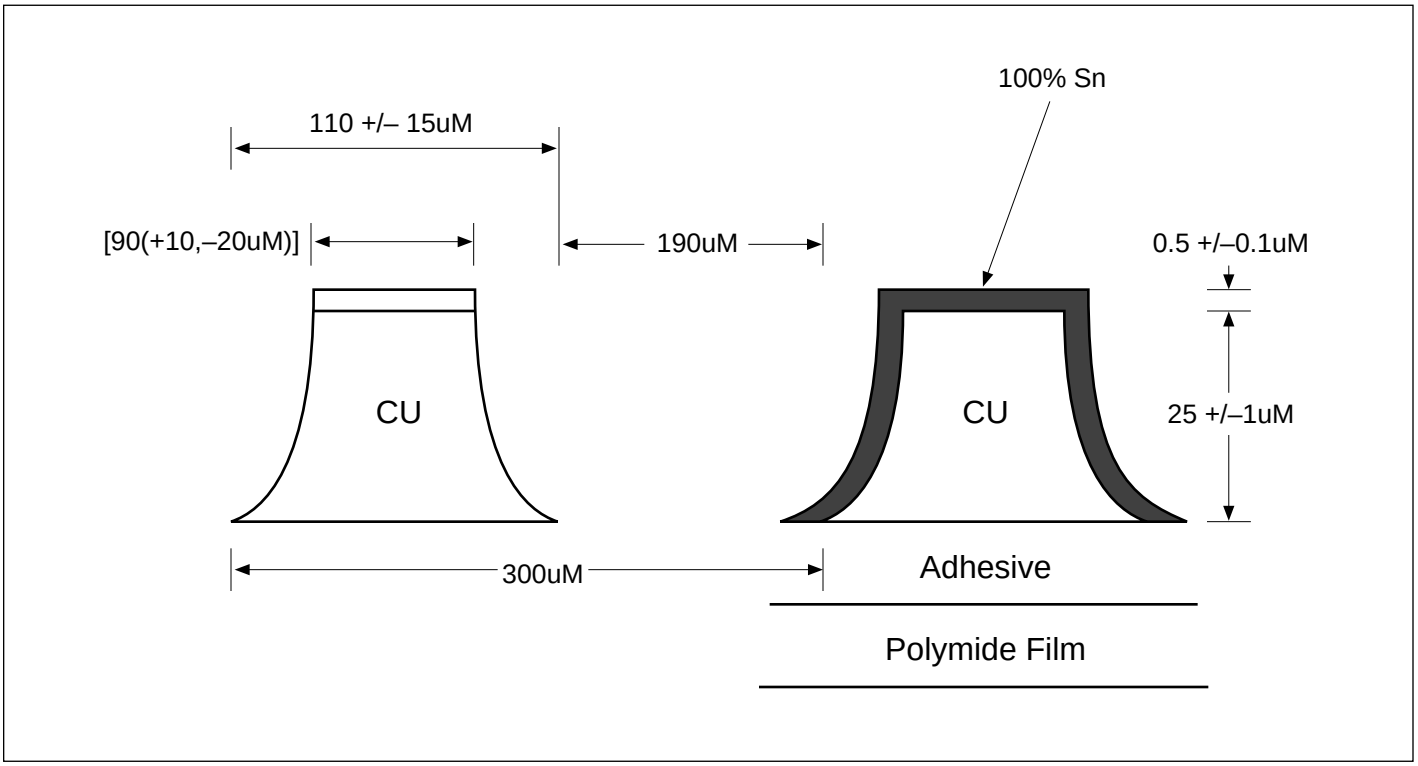


Figure 6.8 SED1560TQA OL Dimensions

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