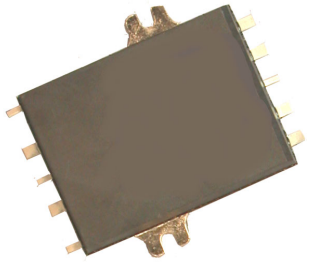
SDM-09060-B1F
SDM-09060-B1FY

RoHS Compliant & Green Package

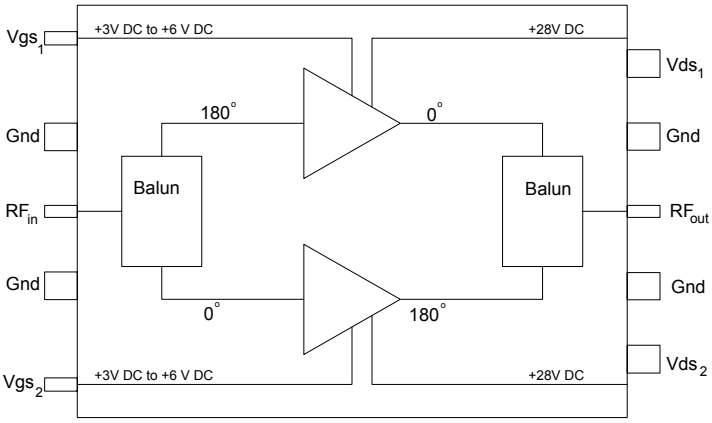
925-960 MHz Class AB
65W Power Amplifier Module



Product Description

Sirenza Microdevices' **SDM-09060-B1F** 65W power module is a robust impedance matched, single-stage, push-pull Class AB amplifier module suitable for use as a power amplifier driver or output stage. The power transistors are fabricated using Sirenza's latest, high performance LDMOS process. It is a drop-in, no-tune solution for high power applications requiring high efficiency, excellent linearity, and unit-to-unit repeatability. It is internally matched to 50 ohms.

Functional Block Diagram



Case Flange = Ground

Product Features

- **Available in RoHS compliant packaging**
- **50 Ω RF impedance**
- **65W Output P_{1dB}**
- **Single Supply Operation : Nominally 28V**
- **High Gain: 17 dB at 942 MHz**
- **High Efficiency : 44% at 942 MHz**
- **ESD Protection: JEDEC Class 2 (2000V HBM)**

Applications

- **Base Station PA driver**
- **Repeater**
- **CDMA**
- **GSM / EDGE**

Key Specifications

Symbol	Parameter	Units	Min.	Typ.	Max.
Frequency	Frequency of Operation	MHz	925	-	960
P_{1dB}	Output Power at 1dB Compression, 943 MHz	W	60	65	-
Gain	Gain at 60W PEP, 942MHz and 943MHz	dB	16	17	-
Gain Flatness	Peak-to-Peak Gain Variation, 60W PEP, 925 - 960MHz	dB	-	0.3	0.5
Efficiency	Drain Efficiency at 60W PEP, 942MHz and 943MHz	%	32	34	-
Efficiency	Drain Efficiency at 60W CW, 942MHz	%		44	-
IRL	Input Return Loss 60W PEP Output Power, 925 - 960MHz	dB	-	-15	-12
IMD	3rd Order IMD Product, 60W PEP, 942MHz and 943MHz	dBc	-	-31	-27
Delay	Signal Delay from Pin 3 to Pin 8	nS	-	4.0	-
Phase Linearity	Deviation from Linear Phase (Peak-to-Peak)	Deg	-	0.5	-
R_{TH}	Thermal Resistance (Junction to Case)	°C/W		1.5	
Test Conditions $Z_{in} = Z_{out} = 50\Omega$, $V_{DD} = 28.0V$, $I_{DQ1} = I_{DQ2} = 300mA$, $T_{Flange} = 25°C$					

Quality Specifications

Parameter	Description	Unit	Typical
ESD Rating	Human Body Model	Volts	2000
MTTF	200°C Channel	Hours	1.2×10^6

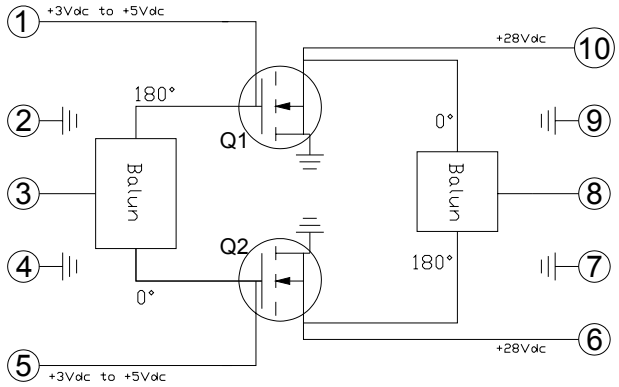
303 S. Technology Court,
Broomfield, CO 80021
Phone: (800) SMI-MMIC

http://www.sirenza.com
EDS-104211Rev D

Pin Description

Pin #	Function	Description
1	V_{GS1}	LDMOS FET Q1 gate bias. V_{GSTH} 3.0 to 5.0 VDC. See Notes 2, 3 and 4
2,4,7,9	Ground	Module Topside ground.
3	RF Input	Module RF input. This pin is internally connected to DC ground. Do not apply DC voltages to the RF leads. Care must be taken to protect against video transients that may damage the active devices.
5	V_{GS2}	LDMOS FET Q2 gate bias. V_{GSTH} 3.0 to 5.0 VDC. See Notes 2, 3 and 4
6	V_{D2}	LDMOS FET Q2 drain bias. See Note 1.
8	RF Output	Module RF output. This pin is internally connected to DC ground. Do not apply DC voltages to the RF leads. Care must be taken to protect against video transients that may damage the active devices.
10	V_{D1}	LDMOS FET Q1 drain bias. See Note 1.
Flange	Ground	Baseplate provides electrical ground and a thermal transfer path for the device. Proper mounting assures optimal performance and the highest reliability. See Sirenza applications note AN-054 Detailed Installation Instructions for Power Modules.

Simplified Device Schematic



Case Flange = Ground

Absolute Maximum Ratings

Parameters	Value	Unit
Drain Voltage (V_{DD})	35	V
RF Input Power	+37	dBm
Load Impedance for Continuous Operation Without Damage	5:1	VSWR
Control (Gate) Voltage, VDD = 0 VDC	15	V
Output Device Channel Temperature	+200	ºC
Operating Temperature Range	-20 to +90	ºC
Storage Temperature Range	-40 to +100	ºC

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation see typical setup values specified in the table on page one.

Note 1:
Internal RF decoupling is included on all bias leads. No additional bypass elements are required, however some applications may require energy storage on the V_D leads to accommodate modulated signals.

Note 2:
Gate voltage must be applied to V_{GS} leads simultaneously with or after application of drain voltage to prevent potentially destructive oscillations. Bias voltages should never be applied to a module unless it is properly terminated on both input and output.

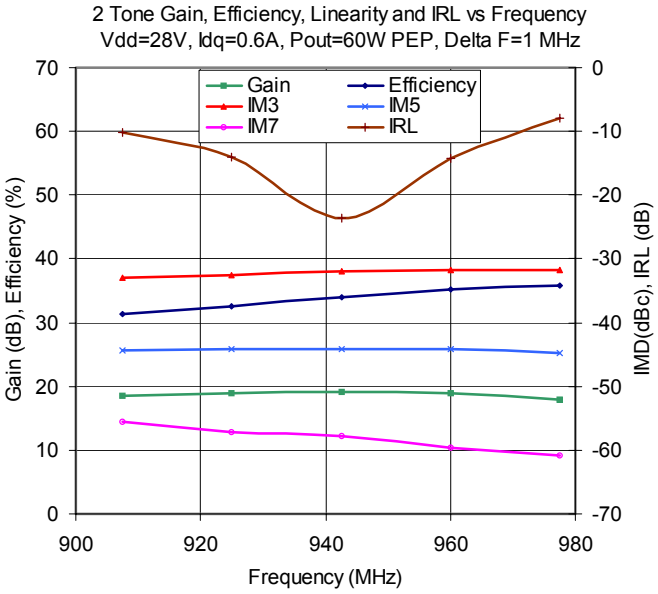
Note 3:
The required V_{GS} corresponding to a specific I_{DQ} will vary from module to module and may differ between V_{GS1} and V_{GS2} on the same module by as much as ±0.10 volts due to the normal die-to-die variation in threshold voltage for LDMOS transistors.

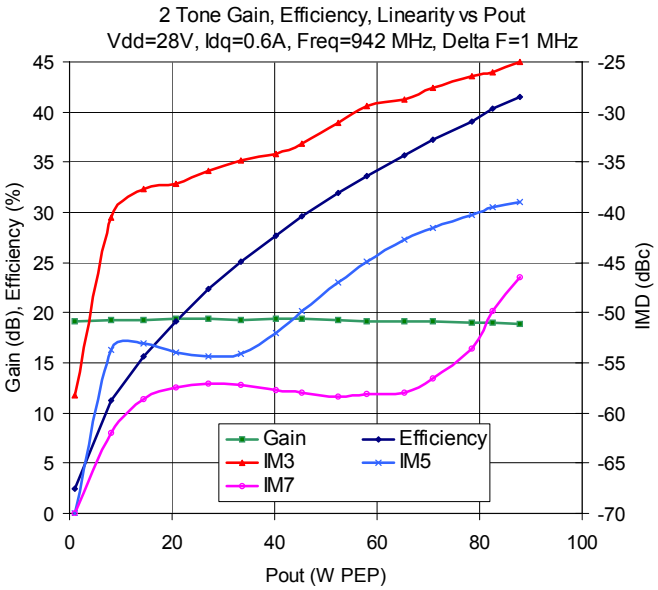
Note 4:
The threshold voltage (V_{GSTH}) of LDMOS transistors varies with device temperature. External temperature compensation may be required. See Sirenza application notes AN-067 LDMOS Bias Temperature Compensation.

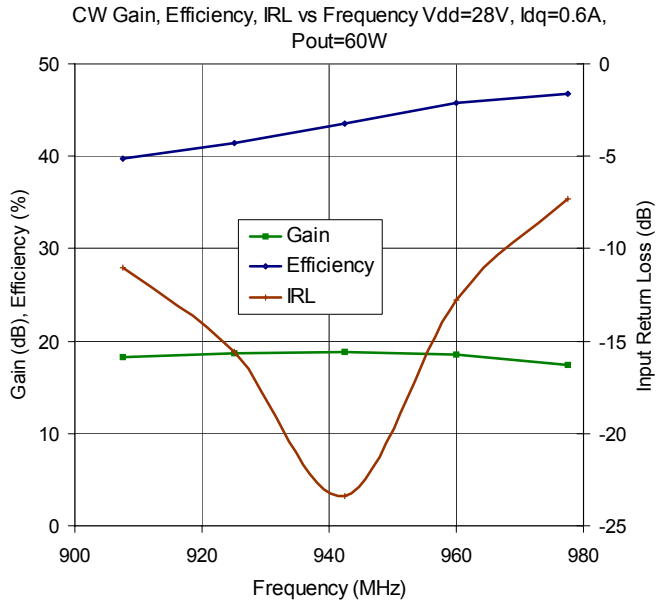
Note 5:
This module was designed to have it's leads hand soldered to an adjacent PCB. The maximum soldering iron tip temperature should not exceed 700° C, and the soldering iron tip should not be in direct contact with the lead for longer than 10 seconds. Refer to app note AN054 (www.sirenza.com) for further installation instructions.

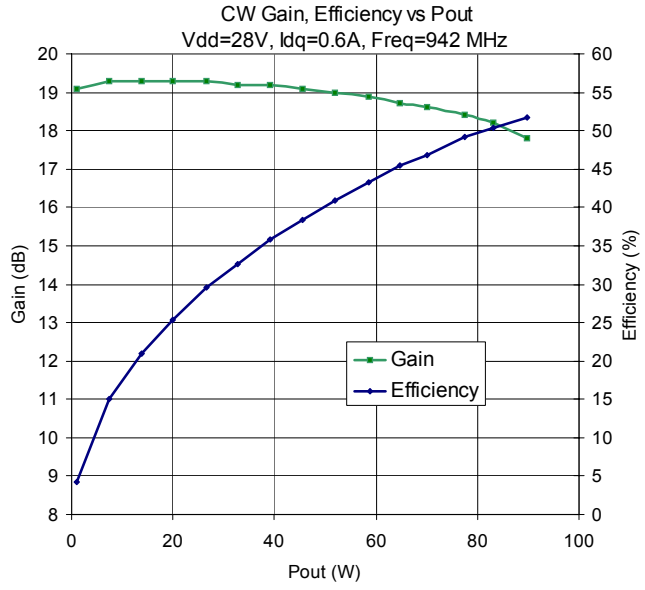
Caution: ESD Sensitive
Appropriate precaution in handling, packaging and testing devices must be observed.

Typical Performance Curves

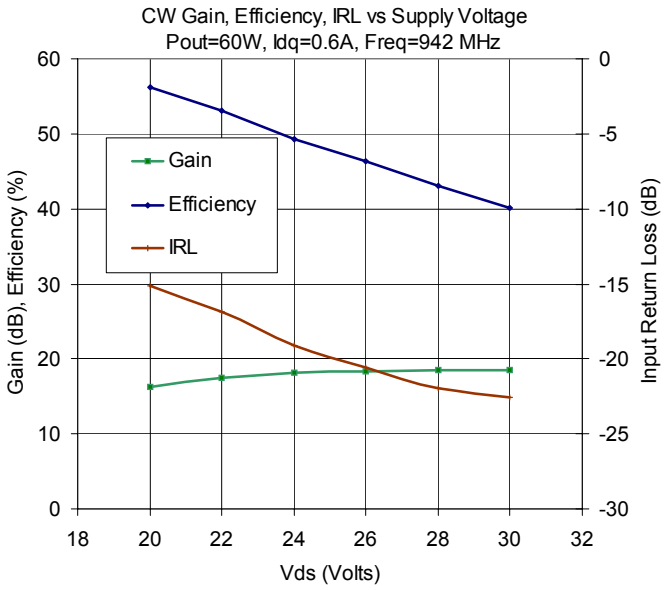


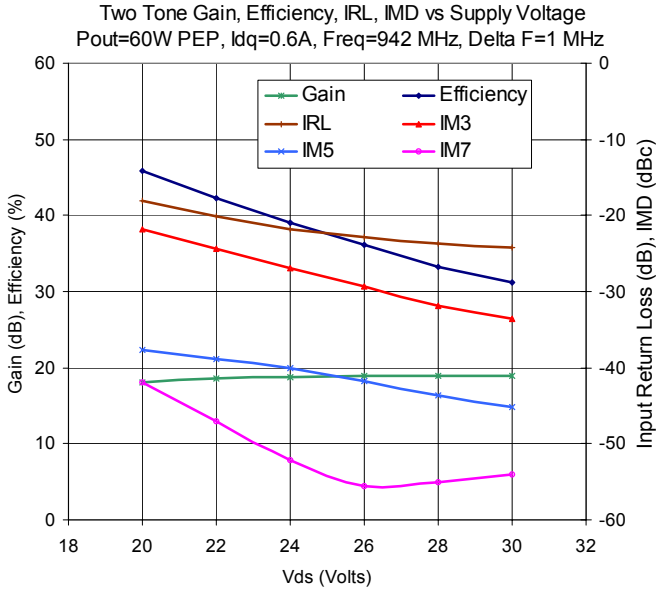


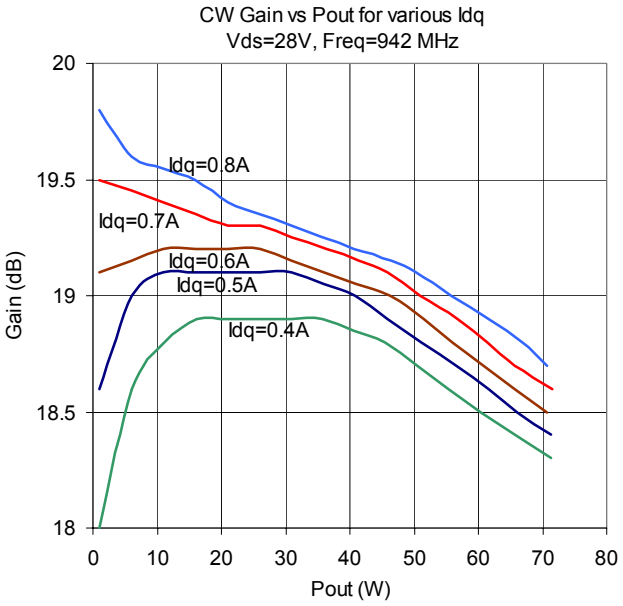


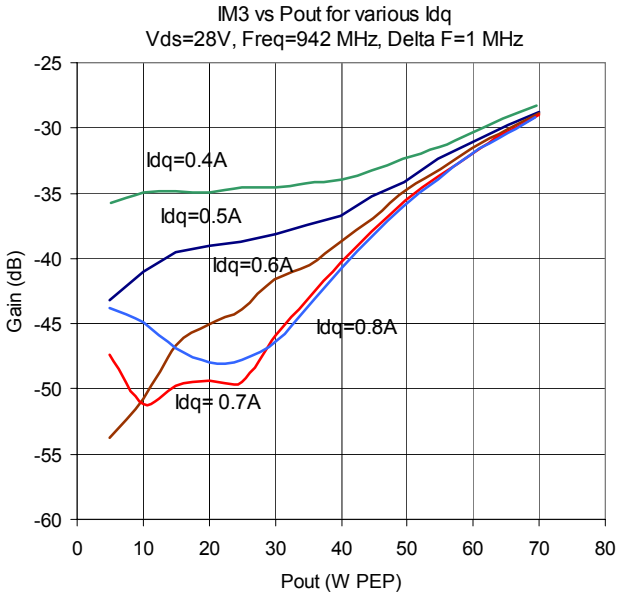


Typical Performance Curves (cont'd)



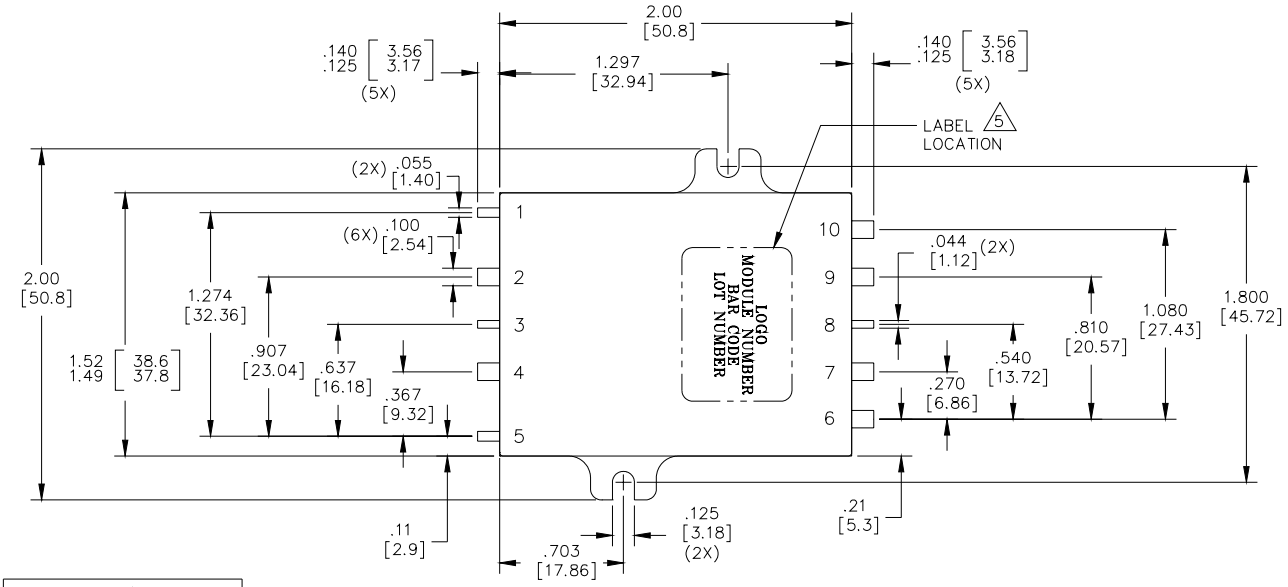




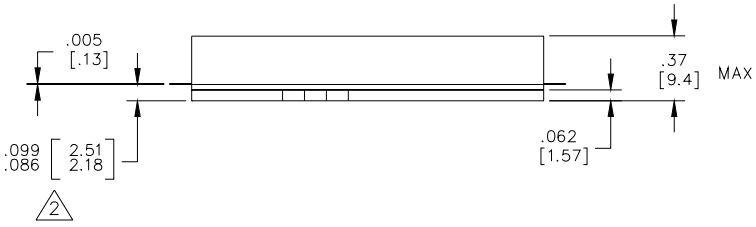


Note:
Evaluation test fixture information available on Sirenza Website, referred to as SDM-EVAL.

Package Outline Drawing



LEAD IDENTIFICATION	
Lead No.	Function
1	Bias 1
2	Ground
3	Input
4	Ground
5	Bias 2
6	V_{DD2}
7	Ground
8	Output
9	Ground
10	V_{DD1}
BASE PLATE	Ground



MODULE WEIGHT = 43gm NOMINAL

NOTES: UNLESS OTHERWISE SPECIFIED

1. INTERPRET DRAWING PER ANSI Y14.5..
2. MEASURE FROM THE BOTTOM OF THE LEADS.
3. DIMENSIONS ARE INCHES[MM].
4. LEAD IDENTIFICATION IS FOR REFERENCE ONLY.
5. ORIENTATION OF LABEL IS TO BE AS SHOWN.

Note:
Refer to Application note AN054, “Detailed Installation Instructions for Power Modules” for detailed mounting information.