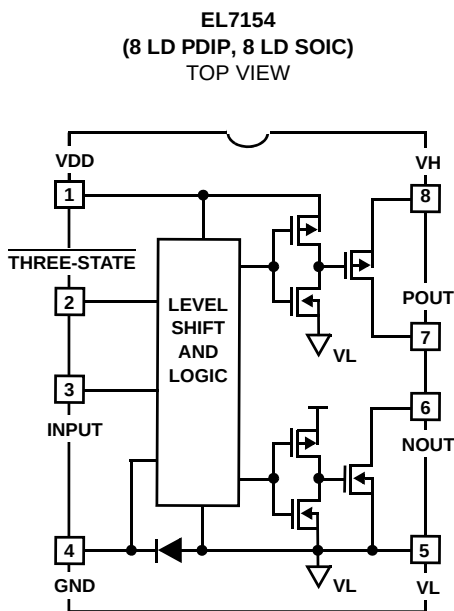


## High Speed, Monolithic Pin Driver

The EL7154 three-state pin driver is particularly well suited for ATE and level shifting applications. The 4A peak drive capability, makes the EL7154 an excellent choice when driving high speed capacitive lines.

The P-Channel MOSFET is completely isolated from the power supply, providing a high degree of flexibility. Pin (7) can be grounded, and the output can be taken from pin (8) when a "source follower" output is desired. The N-Channel MOSFET has an isolated drain, but shares a common bus with pre-drivers and level shifter circuits. This is necessary to ensure that the N-Channel device can turn off effectively when  $V_L$  goes below GND. In some power-FET and IGBT applications, negative drive is desirable to insure effective turn-off. The EL7154 can be used in these applications by returning  $V_L$  to a moderate negative potential.

## Pinout



## Truth Table

| THREE-STATE | INPUT | P <sub>OUT</sub> | N <sub>OUT</sub> |
|-------------|-------|------------------|------------------|
| 0           | 0     | Open             | Open             |
| 0           | 1     | Open             | Open             |
| 1           | 0     | HIGH             | Open             |
| 1           | 1     | Open             | LOW              |

Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047, #5,352,578, #5,352,389, #5,351,012, #5,374,898

## Features

- Comparatively low cost
- Three-State output
- 3V and 5V Input compatible
- Clocking speeds up to 10MHz
- 20ns Switching/delay time
- 4A Peak drive
- Isolated drains
- Low output impedance: 2.5Ω
- Low quiescent current: 5mA
- Wide operating voltage: 4.5V to 16V
- Isolated P-Channel device
- Separate ground and  $V_L$  pins
- Pb-free plus anneal available (RoHS compliant)

## Applications

- Loaded circuit board testers
- Digital testers
- Level shifting below GND
- IGBT drivers
- CCD drivers

**Ordering Information**

| PART NUMBER                 | PART MARKING | TAPE AND REEL | PACKAGE                 | PKG. DWG. # |
|-----------------------------|--------------|---------------|-------------------------|-------------|
| EL7154CN                    | EL7154CN     | -             | 8 Ld PDIP               | MDP0031     |
| EL7154CNZ                   | EL7154CN Z   | -             | 8 Ld PDIP*<br>(Pb-free) | MDP0031     |
| EL7154CS                    | 7154CS       | -             | 8 Ld SOIC               | MDP0027     |
| EL7154CS-T7                 | 7154CS       | 7"            | 8 Ld SOIC               | MDP0027     |
| EL7154CS-T13                | 7154CS       | 13"           | 8 Ld SOIC               | MDP0027     |
| EL7154CSZ<br>(See Note)     | 7154CSZ      | -             | 8 Ld SOIC<br>(Pb-free)  | MDP0027     |
| EL7154CSZ-T7<br>(See Note)  | 7154CSZ      | 7"            | 8 Ld SOIC<br>(Pb-free)  | MDP0027     |
| EL7154CSZ-T13<br>(See Note) | 7154CSZ      | 13"           | 8 Ld SOIC<br>(Pb-free)  | MDP0027     |

\*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

**Nominal Operating Voltage Range**

| PIN               | MIN  | MAX |
|-------------------|------|-----|
| $V_L$             | -3   | 0   |
| $V_{DD}$ to $V_L$ | 5    | 15  |
| $V_H$ to $V_L$    | 2    | 15  |
| $V_{DD}$ to $V_H$ | -0.5 | 15  |
| $V_{DD}$          | 5    | 15  |

**Absolute Maximum Ratings** ( $T_A = +25^\circ\text{C}$ )

Supply ( $V_{DD}$  to  $V_L$ ;  $V_H$  to  $V_L$ ,  $V_H$  to GND),  
 $V_+$  to  $V_H$  ..... 16.5V  
 $V_L$  to GND ..... -5V  
Input Pins ..... -0.3V below  $V_L$  to +0.3V above  $V_{DD}$   
Peak Output Current ..... 4A

**Thermal Information**

Storage Temperature Range ..... -65°C to +150°C  
Ambient Operating Temperature ..... -40°C to +85°C  
Operating Junction Temperature ..... +125°C  
Power Dissipation  
SOIC ..... 570mW  
PDIP\* ..... 1050mW  
Pb-free reflow profile ..... see link below  
<http://www.intersil.com/pbfree/Pb-FreeReflow.asp>  
\*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**IMPORTANT NOTE:** All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_J = T_C = T_A$

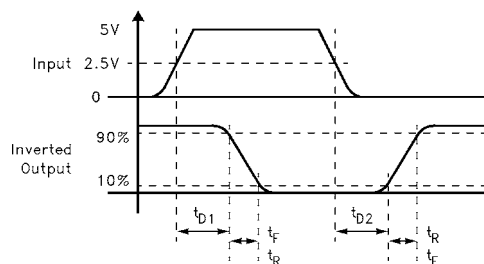
**DC Electrical Specifications**  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +12\text{V}$ ,  $V_H = +12\text{V}$ ,  $V_L = -3\text{V}$ , unless otherwise specified.

| PARAMETER           | DESCRIPTION               | TEST CONDITIONS           | MIN | TYP | MAX | UNITS         |
|---------------------|---------------------------|---------------------------|-----|-----|-----|---------------|
| <b>INPUT</b>        |                           |                           |     |     |     |               |
| $V_{IH}$            | Logic "1" Input Voltage   |                           | 2.4 |     |     | V             |
| $I_{IH}$            | Logic "1" Input Current   | $V_{IH} = V_{DD}$         |     | 0.1 | 10  | $\mu\text{A}$ |
| $V_{IL}$            | Logic "0" Input Voltage   |                           |     |     | 0.6 | V             |
| $I_{IL}$            | Logic "0" Input Current   | $V_{IL} = 0\text{V}$      |     | 0.1 | 10  | $\mu\text{A}$ |
| $V_{HVS}$           | Input Hysteresis          |                           |     | 0.3 |     | V             |
| <b>OUTPUT</b>       |                           |                           |     |     |     |               |
| $R_{OH}$            | Pull-Up Resistance        | $I_{OUT} = -100\text{mA}$ |     | 1.5 | 4   | $\Omega$      |
| $R_{OL}$            | Pull-Down Resistance      | $I_{OUT} = +100\text{mA}$ |     | 2   | 4   | $\Omega$      |
| $I_{OUT}$           | Output Leakage Current    | $V_{DD}/\text{GND}$       |     | 0.2 | 10  | $\mu\text{A}$ |
| $I_{PK}$            | Peak Output Current       | Source/Sink               |     | 4.0 |     | A             |
| $I_{DC}$            | Continuous Output Current | Source/Sink               | 200 |     |     | mA            |
| <b>POWER SUPPLY</b> |                           |                           |     |     |     |               |
| $I_S$               | Power Supply Current      | Inputs = $V_{DD}$         |     | 1   | 2.5 | mA            |
| $V_S$               | Operating Voltage         |                           | 4.5 |     | 16  | V             |
| $I_G$               | Current to GND (Pin 4)    |                           |     | 1   | 10  | $\mu\text{A}$ |
| $I_H$               | Off Leakage at $V_H$      | Pin 8 = 0V                |     | 1   | 10  | $\mu\text{A}$ |

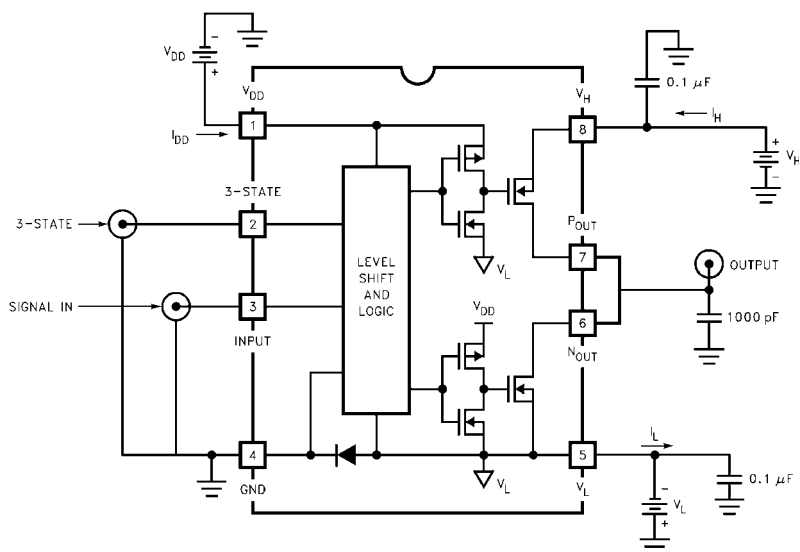
**AC Electrical Specifications**  $T_A = +25^\circ\text{C}$  unless otherwise specified

| PARAMETER                                                                                                | DESCRIPTION         | TEST CONDITIONS       | MIN | TYP | MAX | UNITS |
|----------------------------------------------------------------------------------------------------------|---------------------|-----------------------|-----|-----|-----|-------|
| <b>SWITCHING CHARACTERISTICS (<math>V_{DD} = V_H = 12\text{V}</math>; <math>V_L = -3\text{V}</math>)</b> |                     |                       |     |     |     |       |
| $t_R$                                                                                                    | Rise Time           | $C_L = 100\text{pF}$  |     | 4   | 25  | ns    |
|                                                                                                          |                     | $C_L = 2000\text{pF}$ |     | 20  |     |       |
| $t_F$                                                                                                    | Fall Time           | $C_L = 100\text{pF}$  |     | 4   | 25  | ns    |
|                                                                                                          |                     | $C_L = 2000\text{pF}$ |     | 20  |     |       |
| $t_{D-1}$                                                                                                | Turn-Off Delay Time | $C_L = 2000\text{pF}$ |     | 20  | 25  | ns    |
| $t_{D-2}$                                                                                                | Turn-On Delay Time  | $C_L = 2000\text{pF}$ |     | 10  | 25  | ns    |
| $t_{D-1}$                                                                                                | Three-State Delay   |                       |     |     | 25  | ns    |
| $t_{D-2}$                                                                                                | Three-State Delay   |                       |     |     | 25  | ns    |

## Timing Table



## Standard Test Configuration



## Typical Performance Curves

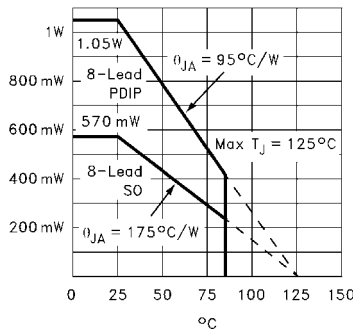


FIGURE 1. MAX POWER DERATING CURVES

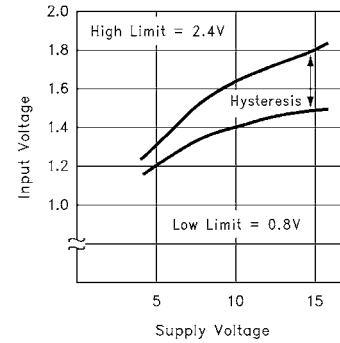


FIGURE 2. SWITCH THRESHOLD vs SUPPLY VOLTAGE

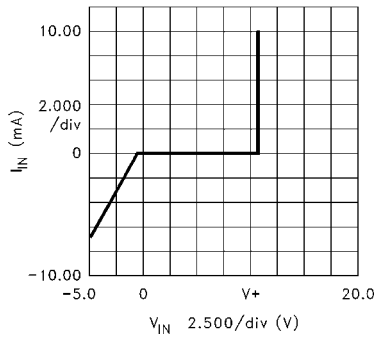


FIGURE 3. INPUT CURRENT vs VOLTAGE

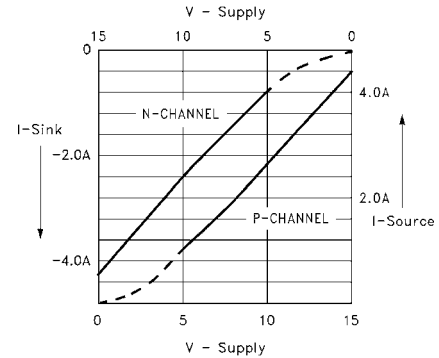


FIGURE 4. PEAK DRIVE vs SUPPLY VOLTAGE

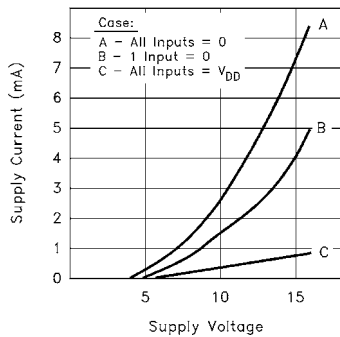


FIGURE 5. QUIESCENT SUPPLY CURRENT

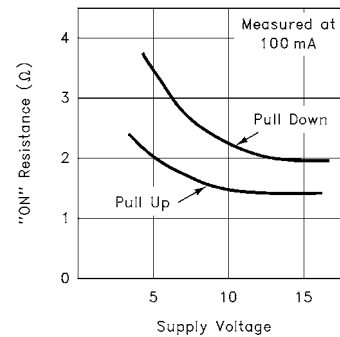


FIGURE 6. "ON" RESISTANCE vs SUPPLY VOLTAGE

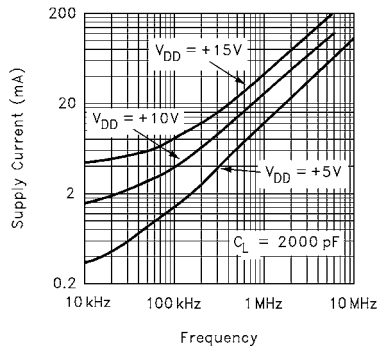


FIGURE 7. AVERAGE SUPPLY CURRENT vs VOLTAGE AND FREQUENCY

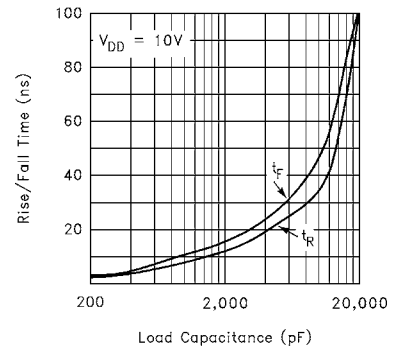


FIGURE 8. RISE/FALL TIME vs LOAD

## Typical Applications

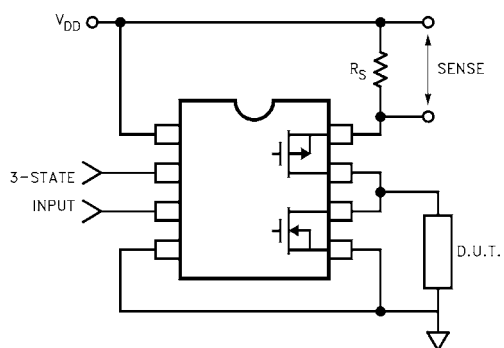


FIGURE 9. PIN DRIVER

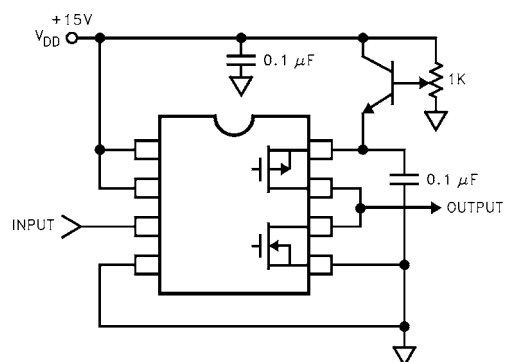


FIGURE 10. ADJUSTABLE AMPLITUDE PULSE GENERATOR

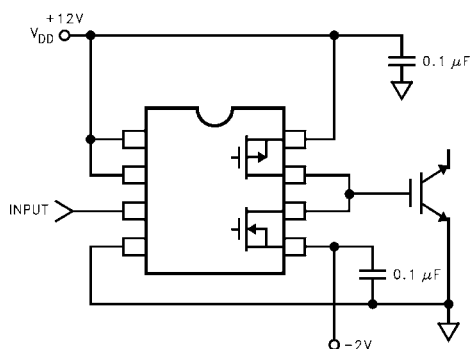


FIGURE 11. IGBT DRIVER WITH NEGATIVE SWING

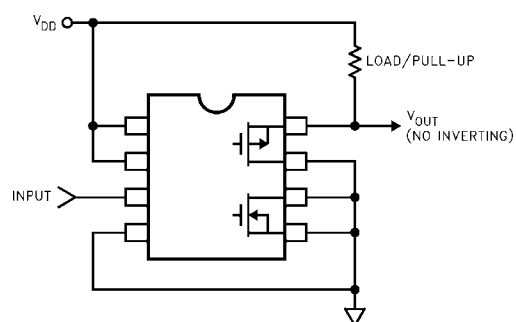


FIGURE 12. PMDS FOLLOWER

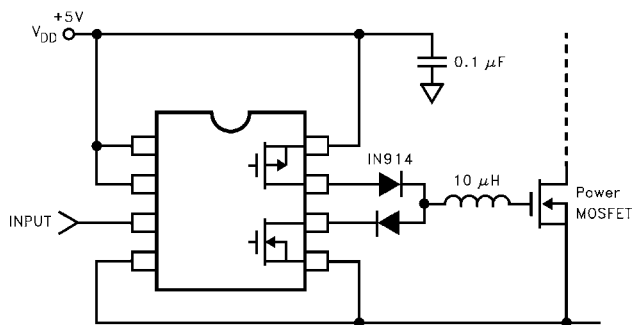
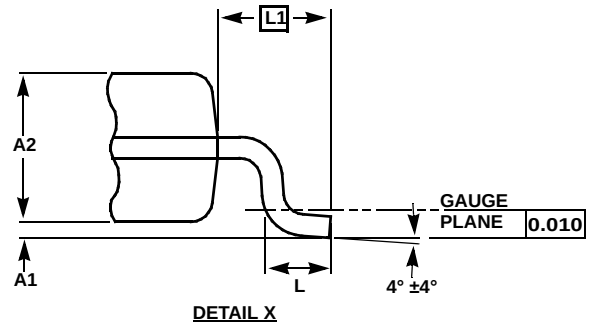
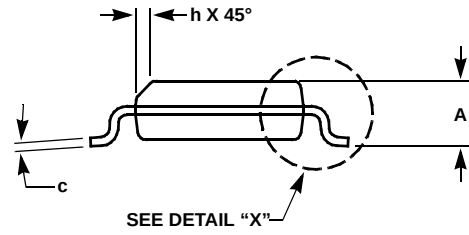
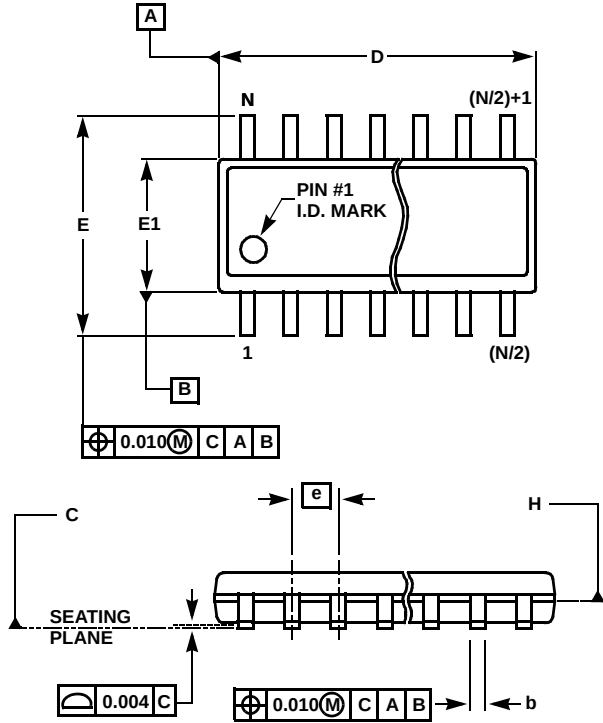


FIGURE 13. RESONANT GATE DRIVER

# Small Outline Package Family (SO)



## MDP0027

### SMALL OUTLINE PACKAGE FAMILY (SO)

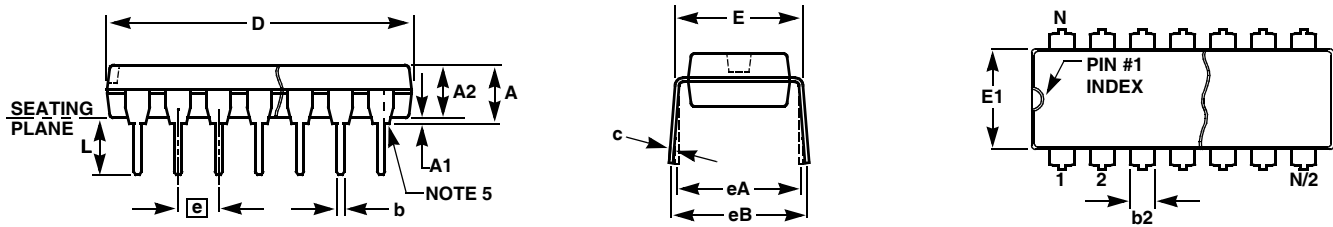
| SYMBOL | INCHES |       |                  |                           |                  |                  |                  | TOLERANCE   | NOTES |
|--------|--------|-------|------------------|---------------------------|------------------|------------------|------------------|-------------|-------|
|        | SO-8   | SO-14 | SO16<br>(0.150") | SO16 (0.300")<br>(SOL-16) | SO20<br>(SOL-20) | SO24<br>(SOL-24) | SO28<br>(SOL-28) |             |       |
| A      | 0.068  | 0.068 | 0.068            | 0.104                     | 0.104            | 0.104            | 0.104            | MAX         | -     |
| A1     | 0.006  | 0.006 | 0.006            | 0.007                     | 0.007            | 0.007            | 0.007            | $\pm 0.003$ | -     |
| A2     | 0.057  | 0.057 | 0.057            | 0.092                     | 0.092            | 0.092            | 0.092            | $\pm 0.002$ | -     |
| b      | 0.017  | 0.017 | 0.017            | 0.017                     | 0.017            | 0.017            | 0.017            | $\pm 0.003$ | -     |
| c      | 0.009  | 0.009 | 0.009            | 0.011                     | 0.011            | 0.011            | 0.011            | $\pm 0.001$ | -     |
| D      | 0.193  | 0.341 | 0.390            | 0.406                     | 0.504            | 0.606            | 0.704            | $\pm 0.004$ | 1, 3  |
| E      | 0.236  | 0.236 | 0.236            | 0.406                     | 0.406            | 0.406            | 0.406            | $\pm 0.008$ | -     |
| E1     | 0.154  | 0.154 | 0.154            | 0.295                     | 0.295            | 0.295            | 0.295            | $\pm 0.004$ | 2, 3  |
| e      | 0.050  | 0.050 | 0.050            | 0.050                     | 0.050            | 0.050            | 0.050            | Basic       | -     |
| L      | 0.025  | 0.025 | 0.025            | 0.030                     | 0.030            | 0.030            | 0.030            | $\pm 0.009$ | -     |
| L1     | 0.041  | 0.041 | 0.041            | 0.056                     | 0.056            | 0.056            | 0.056            | Basic       | -     |
| h      | 0.013  | 0.013 | 0.013            | 0.020                     | 0.020            | 0.020            | 0.020            | Reference   | -     |
| N      | 8      | 14    | 16               | 16                        | 20               | 24               | 28               | Reference   | -     |

Rev. M 2/07

#### NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

## Plastic Dual-In-Line Packages (PDIP)



### MDP0031

#### PLASTIC DUAL-IN-LINE PACKAGE

| SYMBOL | INCHES |        |        |        |        | TOLERANCE     | NOTES |
|--------|--------|--------|--------|--------|--------|---------------|-------|
|        | PDIP8  | PDIP14 | PDIP16 | PDIP18 | PDIP20 |               |       |
| A      | 0.210  | 0.210  | 0.210  | 0.210  | 0.210  | MAX           |       |
| A1     | 0.015  | 0.015  | 0.015  | 0.015  | 0.015  | MIN           |       |
| A2     | 0.130  | 0.130  | 0.130  | 0.130  | 0.130  | ±0.005        |       |
| b      | 0.018  | 0.018  | 0.018  | 0.018  | 0.018  | ±0.002        |       |
| b2     | 0.060  | 0.060  | 0.060  | 0.060  | 0.060  | +0.010/-0.015 |       |
| c      | 0.010  | 0.010  | 0.010  | 0.010  | 0.010  | +0.004/-0.002 |       |
| D      | 0.375  | 0.750  | 0.750  | 0.890  | 1.020  | ±0.010        | 1     |
| E      | 0.310  | 0.310  | 0.310  | 0.310  | 0.310  | +0.015/-0.010 |       |
| E1     | 0.250  | 0.250  | 0.250  | 0.250  | 0.250  | ±0.005        | 2     |
| e      | 0.100  | 0.100  | 0.100  | 0.100  | 0.100  | Basic         |       |
| eA     | 0.300  | 0.300  | 0.300  | 0.300  | 0.300  | Basic         |       |
| eB     | 0.345  | 0.345  | 0.345  | 0.345  | 0.345  | ±0.025        |       |
| L      | 0.125  | 0.125  | 0.125  | 0.125  | 0.125  | ±0.010        |       |
| N      | 8      | 14     | 16     | 18     | 20     | Reference     |       |

Rev. C 2/07

#### NOTES:

1. Plastic or metal protrusions of 0.010" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.
4. Dimension eB is measured with the lead tips unconstrained.
5. 8 and 16 lead packages have half end-leads as shown.

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Intersil Corporation's quality certifications can be viewed at [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

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