



## STS5PF30L

P-channel 30V - 0.045Ω - 5A SO-8  
STripFET™ Power MOSFET

### General features

| Type      | V <sub>DSS</sub> | R <sub>DS(on)</sub> | I <sub>D</sub> |
|-----------|------------------|---------------------|----------------|
| STS5PF30L | 30V              | <0.055Ω             | 5A             |

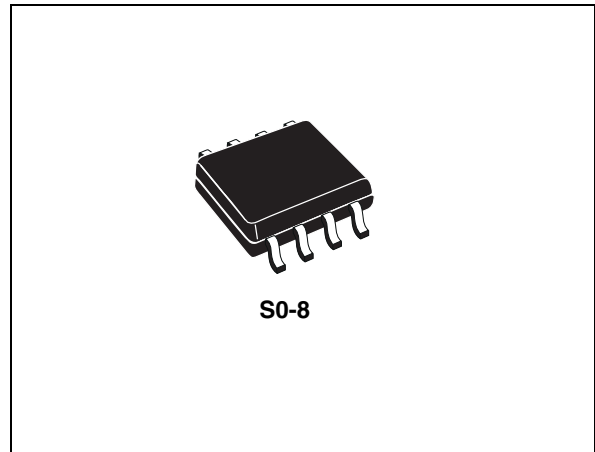
- Conduction losses reduced
- Switching losses reduced
- Low threshold drive
- Standard outline for easy automated surface mount assembly

### Description

This Power MOSFET is the latest development of STMicroelectronics unique “single feature size™” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

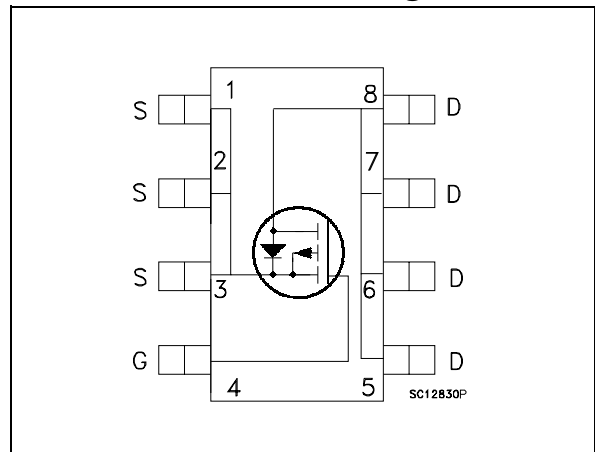
### Applications

- Switching application



SO-8

### Internal schematic diagram



### Order code

| Part number | Marking | Package | Packaging   |
|-------------|---------|---------|-------------|
| STS5PF30L   | S5PF30L | SO-8    | Tape & reel |

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol         | Parameter                                                    | Value      | Unit             |
|----------------|--------------------------------------------------------------|------------|------------------|
| $V_{DS}$       | Drain-source voltage ( $v_{gs} = 0$ )                        | 30         | V                |
| $V_{GS}$       | Gate- source voltage                                         | $\pm 16$   | V                |
| $I_D$          | Drain current (continuous) at $T_C = 25^\circ\text{C}$       | 5          | A                |
| $I_D$          | Drain current (continuous) at $T_C = 100^\circ\text{C}$      | 4          | A                |
| $I_{DM}^{(1)}$ | Drain current (pulsed)                                       | 20         | A                |
| $P_{TOT}$      | Total dissipation at $T_C = 25^\circ\text{C}$ dual operating | 2.5        | W                |
| $T_J$          | Junction temperature                                         | -55 to 150 | $^\circ\text{C}$ |
| $T_{stg}$      | Storage temperature range                                    | 150        | $^\circ\text{C}$ |

1. Pulse width limited by safe operating area

**Note:** For the *p*-channel Power MOSFET actual polarity of voltages and current has to be reversed

**Table 2. Thermal data**

|             |                                                        |     |                    |
|-------------|--------------------------------------------------------|-----|--------------------|
| $R_{thj-a}$ | <sup>(1)</sup> Thermal resistance junction-ambient Max | 50  | $^\circ\text{C/W}$ |
| $T_L$       | Maximum lead temperature for soldering purpose         | 300 | $^\circ\text{C}$   |

1. Mounted on FR-4 board ( $t \leq 10\text{sec}$ )

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}\text{C}$  unless otherwise specified)

**Table 3. On/off states**

| Symbol        | Parameter                                           | Test conditions                                                                               | Min. | Typ.           | Max.           | Unit                           |
|---------------|-----------------------------------------------------|-----------------------------------------------------------------------------------------------|------|----------------|----------------|--------------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage                      | $I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0$                                                 | 30   |                |                | V                              |
| $I_{DSS}$     | Zero gate voltage<br>Drain current ( $V_{GS} = 0$ ) | $V_{DS} = \text{Max rating}$<br>$V_{DS} = \text{Max rating}$ ,<br>$T_C = 125^{\circ}\text{C}$ |      |                | 1<br>10        | $\mu\text{A}$<br>$\mu\text{A}$ |
| $I_{GSS}$     | Gate-body leakage<br>current ( $V_{DS} = 0$ )       | $V_{GS} = \pm 16\text{V}$                                                                     |      |                | $\pm 100$      | nA                             |
| $V_{GS(th)}$  | Gate threshold voltage                              | $V_{DS} = V_{GS}$ , $I_D = 250\mu\text{A}$                                                    | 1    | 1.6            | 2.5            | V                              |
| $R_{DS(on)}$  | Static drain-source on<br>resistance                | $V_{GS} = 10\text{V}$ , $I_D = 2.5\text{A}$<br>$V_{GS} = 4.5\text{V}$ , $I_D = 2.5\text{A}$   |      | 0.045<br>0.065 | 0.055<br>0.075 | $\Omega$<br>$\Omega$           |

**Table 4. Dynamic**

| Symbol         | Parameter                       | Test conditions                                                                        | Min. | Typ. | Max. | Unit |
|----------------|---------------------------------|----------------------------------------------------------------------------------------|------|------|------|------|
| $g_{fs}^{(1)}$ | Forward transconductance        | $V_{DS} = 15\text{V}$ , $I_D = 2.5\text{A}$                                            |      | 10   |      | S    |
| $C_{iss}$      | Input capacitance               | $V_{DS} = 25\text{V}$ , $f = 1\text{ MHz}$ ,<br>$V_{GS} = 0$                           |      | 1350 |      | pF   |
| $C_{oss}$      | Output capacitance              |                                                                                        |      | 490  |      | pF   |
| $C_{rss}$      | Reverse transfer<br>capacitance |                                                                                        |      | 130  |      | pF   |
| $Q_g$          | Total gate charge               | $V_{DD} = 24\text{V}$ , $I_D = 5\text{A}$ ,<br>$V_{GS} = 5\text{V}$<br>(see Figure 14) |      | 12.5 | 16   | nC   |
| $Q_{gs}$       | Gate-source charge              |                                                                                        |      | 5    |      | nC   |
| $Q_{gd}$       | Gate-drain charge               |                                                                                        |      | 3    |      | nC   |

1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5.

**Table 5. Switching times**

| Symbol                | Parameter                        | Test conditions                                                                                           | Min. | Typ.      | Max. | Unit     |
|-----------------------|----------------------------------|-----------------------------------------------------------------------------------------------------------|------|-----------|------|----------|
| $t_{d(on)}$<br>$t_r$  | Turn-on delay time<br>Rise time  | $V_{DD}=15\text{ V}$ , $I_D=2.5\text{ A}$ ,<br>$R_G=4.7\Omega$ , $V_{GS}=4.5\text{ V}$<br>(see Figure 13) |      | 25<br>35  |      | ns<br>ns |
| $t_{d(off)}$<br>$t_f$ | Turn-off Delay Time<br>Fall Time | $V_{DD}=15\text{ V}$ , $I_D=2.5\text{ A}$ ,<br>$R_G=4.7\Omega$ , $V_{GS}=4.5\text{ V}$<br>(see Figure 13) |      | 125<br>35 |      | ns<br>ns |

**Table 6. Source drain diode**

| Symbol                            | Parameter                                                                    | Test conditions                                                                                                                        | Min | Typ.            | Max | Unit          |
|-----------------------------------|------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|-----|-----------------|-----|---------------|
| $I_{SD}$                          | Source-drain current                                                         |                                                                                                                                        |     |                 | 5   | A             |
| $I_{SDM}^{(1)}$                   | Source-drain current (pulsed)                                                |                                                                                                                                        |     |                 | 20  | A             |
| $V_{SD}^{(2)}$                    | Forward on voltage                                                           | $I_{SD} = 5\text{ A}$ , $V_{GS} = 0$                                                                                                   |     |                 | 1.2 | V             |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse recovery time<br>Reverse recovery charge<br>Reverse recovery current | $I_{SD} = 5\text{ A}$ , $V_{DD} = 15\text{ V}$<br>$di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$T_j = 150^\circ\text{C}$<br>(see Figure 15) |     | 45<br>36<br>1.6 |     | ns<br>nC<br>A |

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

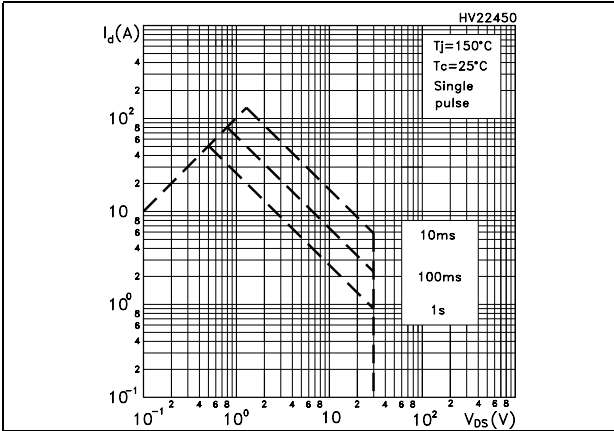


Figure 2. Thermal impedance

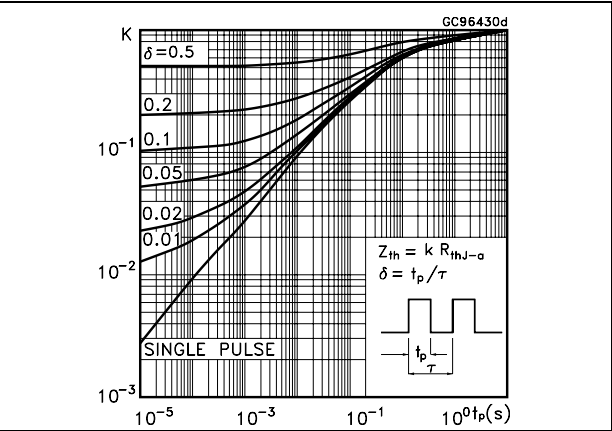


Figure 3. Output characteristics

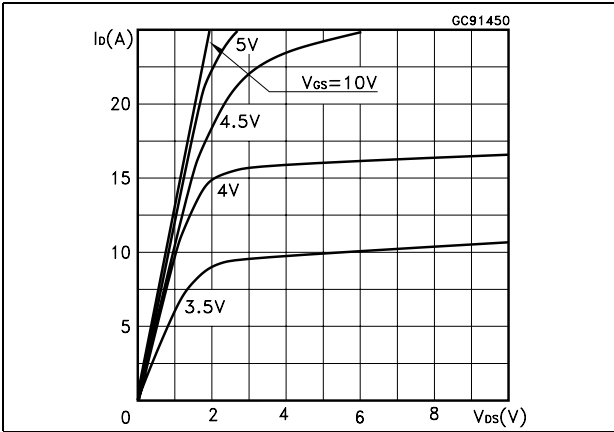


Figure 4. Transfer characteristics

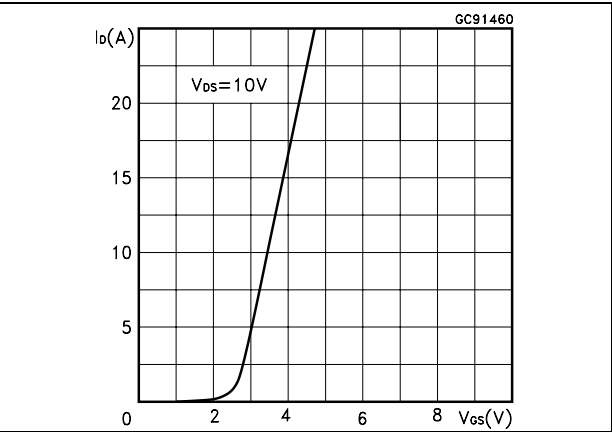


Figure 5. Transconductance

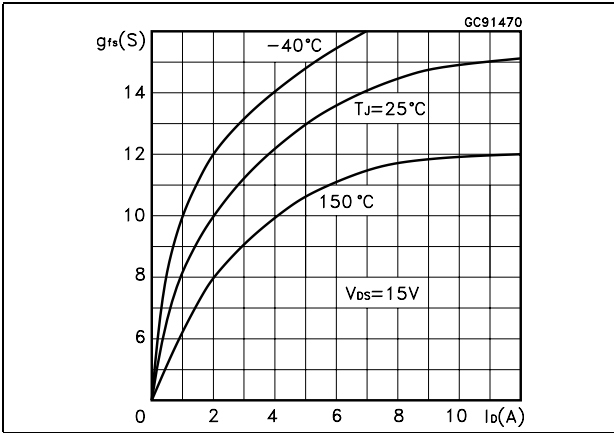


Figure 6. Static drain-source on resistance

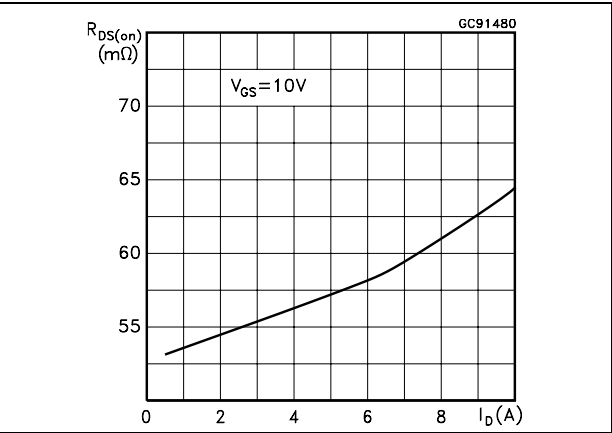


Figure 7. Gate charge vs gate-source voltage    Figure 8. Capacitance variations

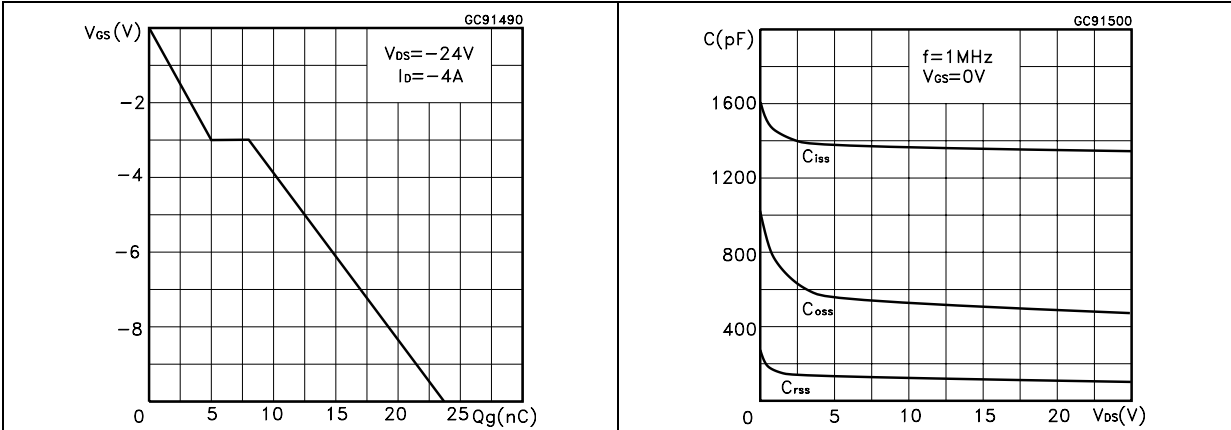


Figure 9. Normalized gate threshold voltage vs temperature    Figure 10. Normalized on resistance vs temperature

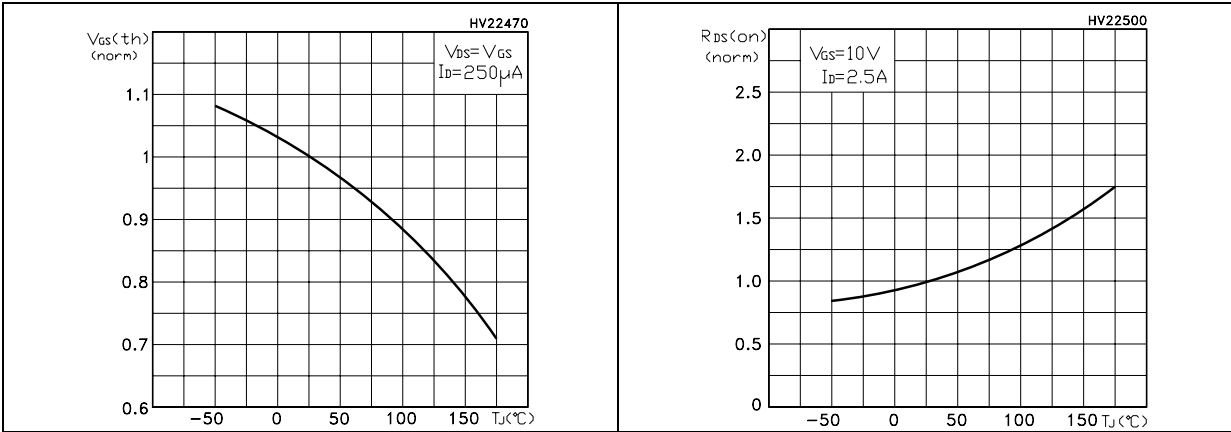
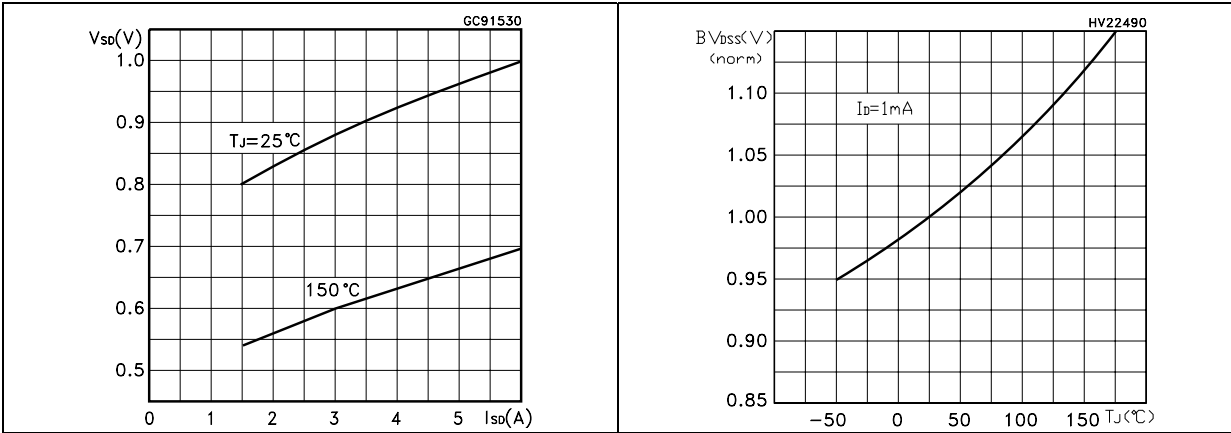


Figure 11. Source-drain diode forward characteristics    Figure 12. Normalized  $BV_{DSS}$  vs temperature



### 3 Test circuit

Figure 13. Switching times test circuit for resistive load

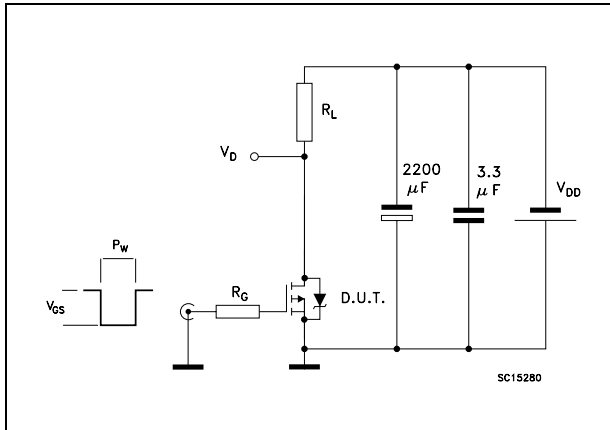


Figure 14. Gate charge test circuit

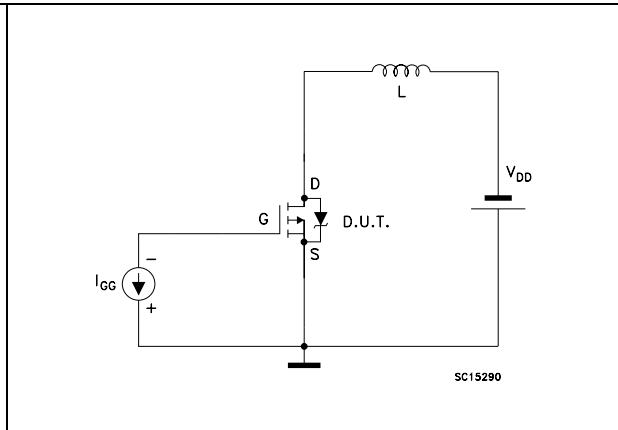
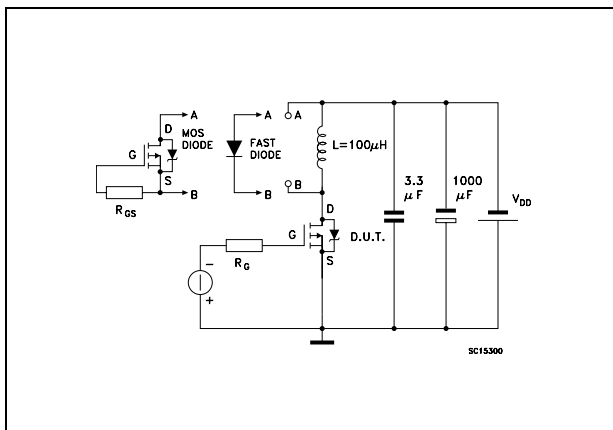


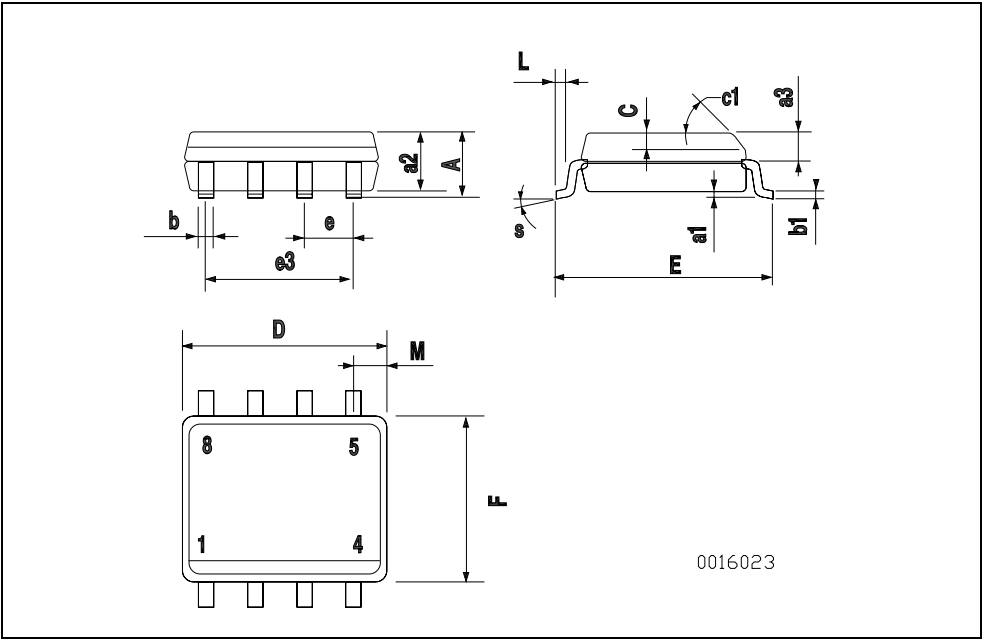
Figure 15. Test circuit for diode recovery behavior



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

| SO-8 MECHANICAL DATA |           |      |      |       |       |       |
|----------------------|-----------|------|------|-------|-------|-------|
| DIM.                 | mm.       |      |      | inch  |       |       |
|                      | MIN.      | TYP  | MAX. | MIN.  | TYP.  | MAX.  |
| A                    |           |      | 1.75 |       |       | 0.068 |
| a1                   | 0.1       |      | 0.25 | 0.003 |       | 0.009 |
| a2                   |           |      | 1.65 |       |       | 0.064 |
| a3                   | 0.65      |      | 0.85 | 0.025 |       | 0.033 |
| b                    | 0.35      |      | 0.48 | 0.013 |       | 0.018 |
| b1                   | 0.19      |      | 0.25 | 0.007 |       | 0.010 |
| C                    | 0.25      |      | 0.5  | 0.010 |       | 0.019 |
| c1                   | 45 (typ.) |      |      |       |       |       |
| D                    | 4.8       |      | 5.0  | 0.188 |       | 0.196 |
| E                    | 5.8       |      | 6.2  | 0.228 |       | 0.244 |
| e                    |           | 1.27 |      |       | 0.050 |       |
| e3                   |           | 3.81 |      |       | 0.150 |       |
| F                    | 3.8       |      | 4.0  | 0.14  |       | 0.157 |
| L                    | 0.4       |      | 1.27 | 0.015 |       | 0.050 |
| M                    |           |      | 0.6  |       |       | 0.023 |
| S                    | 8 (max.)  |      |      |       |       |       |



## 5 Revision history

**Table 7. Revision history**

| <b>Date</b> | <b>Revision</b> | <b>Changes</b>                    |
|-------------|-----------------|-----------------------------------|
| 06-Feb-2007 | 4               | The document has been reformatted |

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