SONET/SDH/ATM 155 MBIT/S QUAD TRANSCEIVER S3029

FEATURES

- Complies with ANSI, Bellcore, and ITU-T specifications for jitter tolerance, jitter generation
- Five on-chip high frequency PLLs with internal loop filters for clock recovery
- Supports clock recovery for STS-3/STM-1 (155.52 Mbit/s) NRZ data
- Clock Multiplier PLL for transmit clock generation
- 19.44 or 51.84 MHz reference frequency
- Lock detect—monitors run length and frequency
- Low-jitter differential interface
- 3.3V supply
- Available in a 64-pin TQFP package
- Compatible with IgT WAC-413 ATM Quad-UNI processor

GENERAL DESCRIPTION

The function of the S3029 clock synthesis and recovery unit is to derive high speed timing signals for SONET/SDH-based equipment. The S3029 is implemented using AMCC's proven Phase Locked Loop (PLL) technology.

The S3029 receives four STS-3/STM-1 scrambled NRZ signals and recovers the clock from the data and generates a 155 MHz transmit clock. The chip outputs a differential PECL bit clock and retimed data. Figure 1 shows a typical network application.

The S3029 utilizes five on-chip PLLs which consist of a phase detector, a loop filter, and a voltage controlled oscillator (VCO). The phase detector compares the phase relationship between the VCO output and the serial data input. A loop filter converts the phase detector output into a smooth DC voltage, and the DC voltage is input to the VCO whose frequency is varied by this voltage. A block diagram is shown in Figure 2. There is a single clock multiplier PLL which generates a 155 MHz transmit clock from a 19.44 or 51.84 MHz input.

Figure 1. System Block Diagram

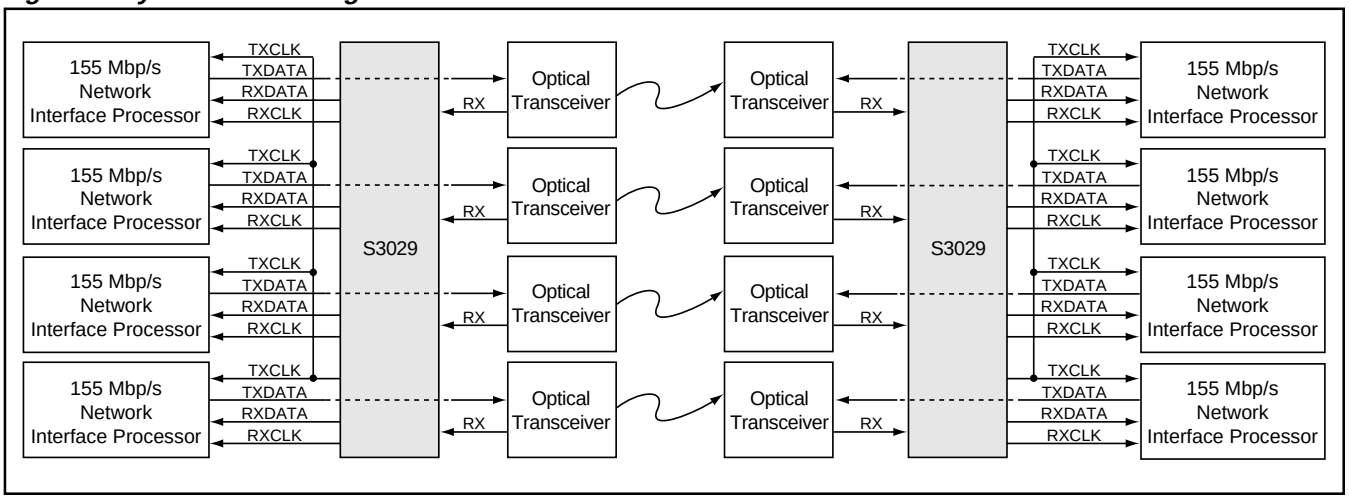
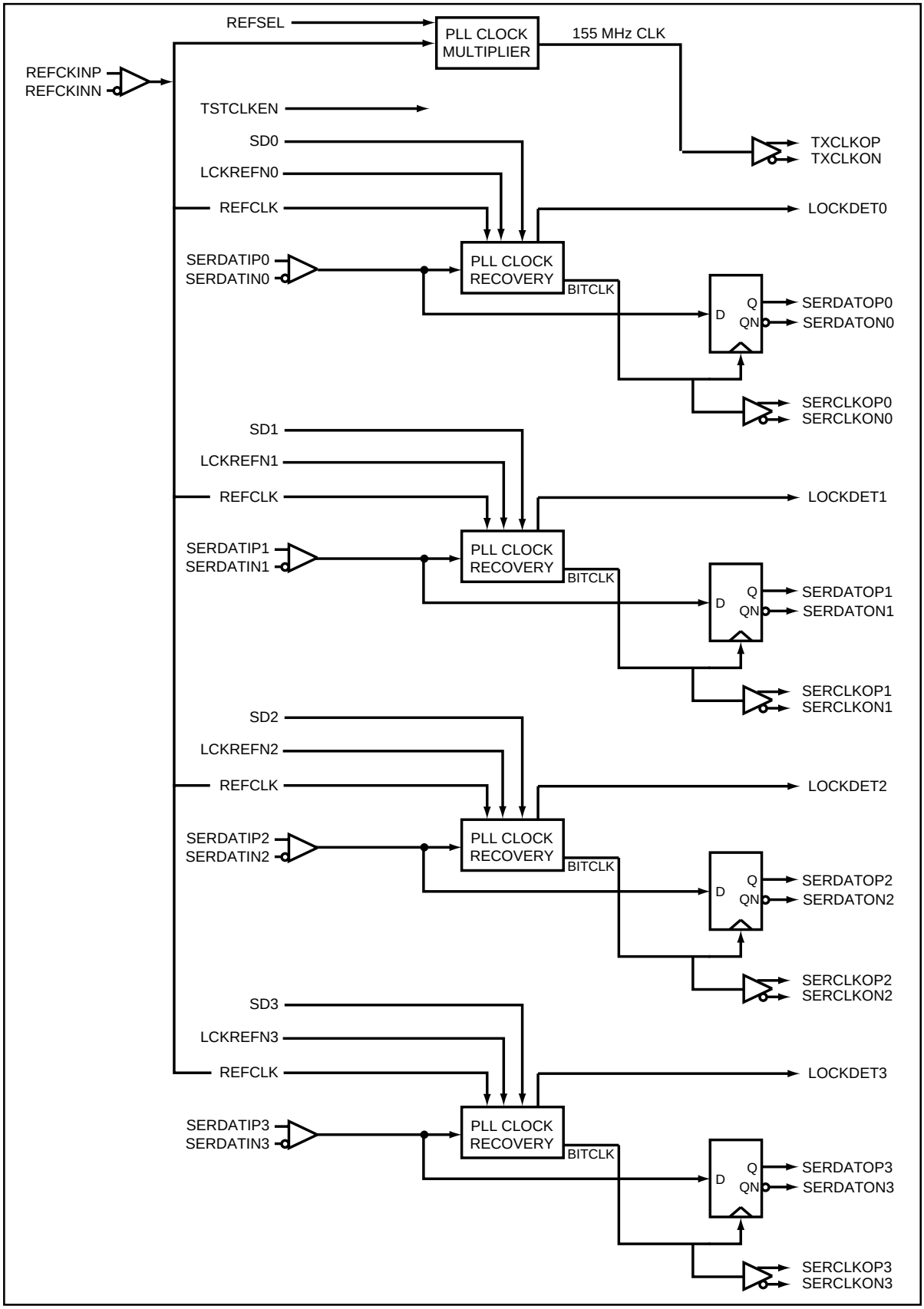


Figure 2. Functional Block Diagram



S3029 OVERVIEW

The S3029 supports clock recovery for the STS-3/ STM-1 data rate. The LVPECL differential serial data is input to the chip and clock recovery is performed on the incoming data stream. An external reference clock is required to minimize the PLL lock time and provide a stable output clock source in the absence of serial input data. Retimed data and clock are output from the S3029.

CHARACTERISTICS

Performance

The S3029 PLL complies with the minimum jitter tolerance for clock recovery proposed for SONET/SDH equipment defined by the T1X1.6/91-022 document, when used with differential inputs and outputs as shown in Figure 3.

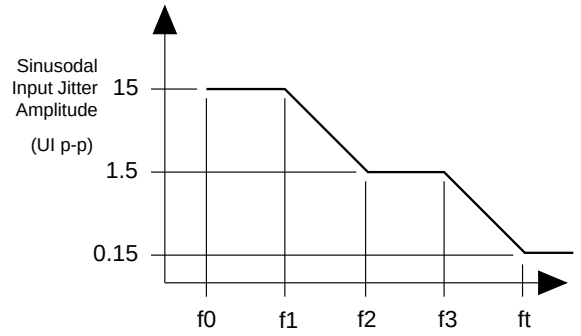
Input Jitter Tolerance

Input jitter tolerance is defined as the peak to peak amplitude of sinusoidal jitter applied on the input signal that causes an equivalent 1 dB optical/electrical power penalty. SONET input jitter tolerance requirements are shown in Figure 3. The measurement condition is the input jitter amplitude which causes an equivalent of 1 dB power penalty.

Serial Data Output Set-up and Hold Time

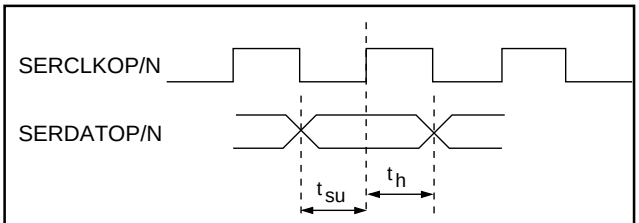
The output set-up and hold times are represented by the waveforms shown in Figure 4.

Figure 3. Input Jitter Tolerance Specification



OC/STS Level	f0 (Hz)	f1 (Hz)	f2 (Hz)	f3 (kHz)	ft (kHz)
3	10	30	300	6.5	75

Figure 4. Clock Output to Data Transition Delay



	Output Frequency
	155.52 MHz
SERDATOP/N Setup Time	2.5 ns
SERDATOP/N Hold Time	2.5 ns

Table 1.

REFSEL	Reference Clock Frequency (MHz)
0	19.44 MHz
1	51.84 MHz

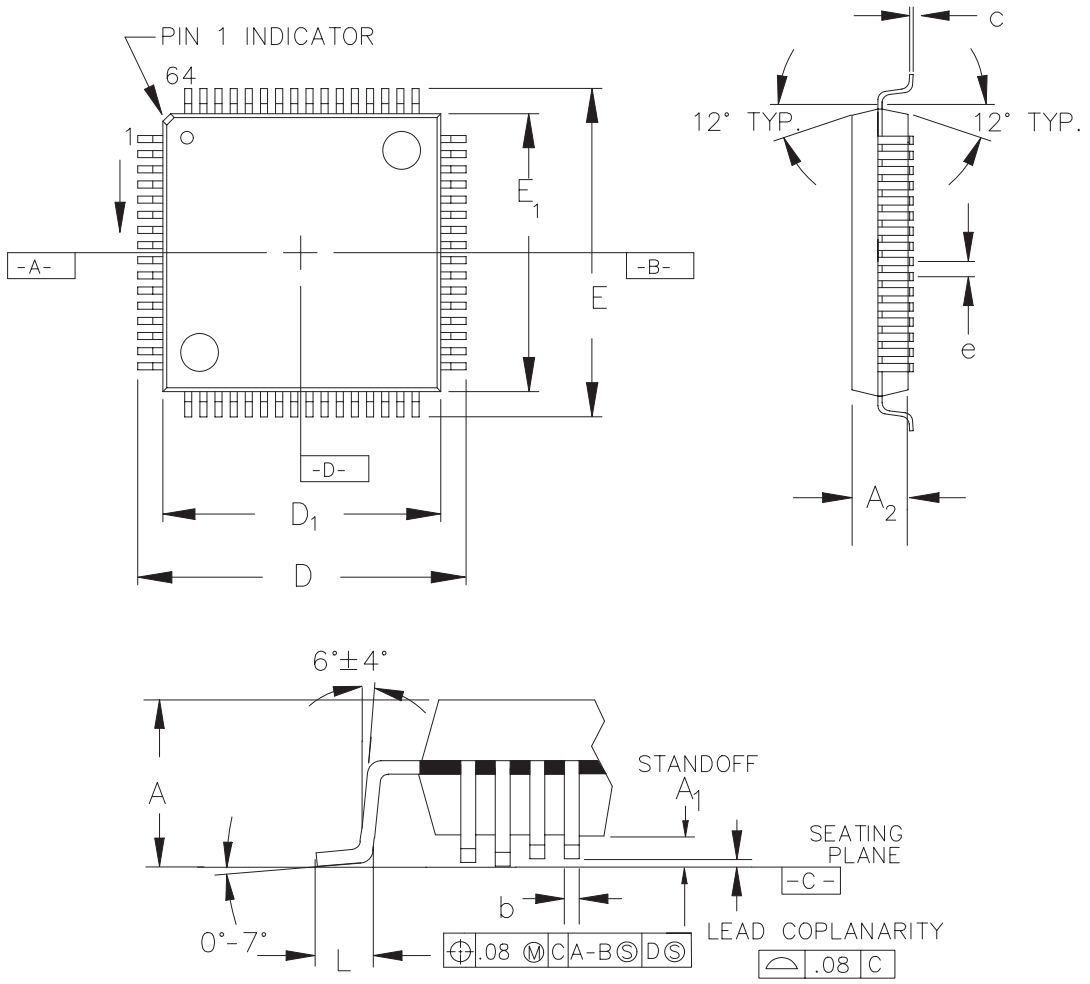
S3029 Transceiver Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
REFCKINP/N	Diff. LVPECL	I	53,54	Reference Clock. 19.44 or 51.84 MHz input used to generate the 155 MHz transmit clock. This input is also used as the reference for the internal bit clock in the absence of serial data or during reset in clock recovery mode.
SERDATIP/N0 SERDATIP/N1 SERDATIP/N2 SERDATIP/N3	Diff. LVPECL	I	1,2 7,8 15,16 22,21	Serial Data In. Clock is recovered from the transitions on these inputs.
TSTCLKEN	LVTTL	I	3	Test Clock Enable. Active High. Used during production test to bypass the VCO in the PLL. Tie to ground for normal operation.
SD0 SD1 SD2 SD3	LVPECL	I	56 55 52 51	Signal Detect. Active High. A single-ended 10K ECL input to be driven by the external optical receiver module to indicate detection of received optical power. When SD is inactive, the data on the Serial Data In (SERDATIP/N) pins will be internally forced to a constant zero, LOCKDET forced low, and the PLL forced to lock to the REFCK input. When SD is active, data on the SERDATIP/N pins will be processed normally. This pin has an internal 1KΩ pull-down.
LCKREFN0 LCKREFN1 LCKREFN2 LCKREFN3	LVTTL	I	64 63 60 59	Lock to Reference. Active Low. When active, this input will force the CRU to lock to the local reference clock. This input has an internal 1K pull-up and may be left unconnected if not used.
REFSEL	LVTTL	I	6	Reference Select. This input selects the frequency of the REFCKIN/P. (See Table 1).
LOCKDET0 LOCKDET1 LOCKDET2 LOCKDET3	LVTTL	O	9 14 17 20	Lock Detect. Active High. Clock recovery indicator. Set high when the internal clock recovery has locked onto the incoming datastream. LOCKDET is an asynchronous output. This output is deasserted when LCKREFN is low, or when SD is low; in which case the PLL locks to the reference clock. When the data rate of the SERDATIP/N input is not within the capture range of the PLL, the LOCKDET output will toggle until proper data is restored.
SERDATOP/N0 SERDATOP/N1 SERDATOP/N2 SERDATOP/N3	Diff. LVPECL	O	44,43 40,39 30,29 26,25	Serial Data Out. This signal is the delayed version of the incoming data stream (SERDATI) updated on the falling edge of Serial Clock Out (SERCLKOP).
SERCLKOP/N0 SERCLKOP/N1 SERCLKOP/N2 SERCLKOP/N3	Diff. LVPECL	O	46,45 38,37 32,31 24,23	Serial Clock Out. This signal is phase aligned with Serial Data Out (SERDATO) when Lock Detect (LOCKDET) is High. When Lock Detect is Low, Serial Clock Out is synchronous with Reference Clock (REFCKIN).
TXCLKOP/N	Diff. LVPECL	O	50,49	Transmit Clock Out. This is a 155 MHz clock which can be used by the controller as a clock source for the transmitter logic.

S3029 Transceiver Pin Assignment and Descriptions (continued)

Pin Name	Level	I/O	Pin #	Description
TXoPOW CRUoPOW0 CRUoPOW1 CRUoPOW2 CRUoPOW3	Digital Power	—	48 42 36 34 28	+3.3V (individual decoupling)
TXoGRD CRUoGRD0 CRUoGRD1 CRUoGRD2 CRUoGRD3	Digital Ground	—	47 41 35 33 27	0V (ground)
VCOVCC OPAVCC ACRUPOW0 ACRUPOW1 ACRUPOW2 ACRUPOW3	Analog Power	—	58 62 4 10 12 18	+3.3V via individual Ferrite bead (e.g. Murata BLM32A06) and individual decoupling.
VCOGRD OPAGRD ACRUGRD0 ACRUGRD1 ACRUGRD2 ACRUGRD3	Analog Ground	—	57 61 5 11 13 19	0V (ground)

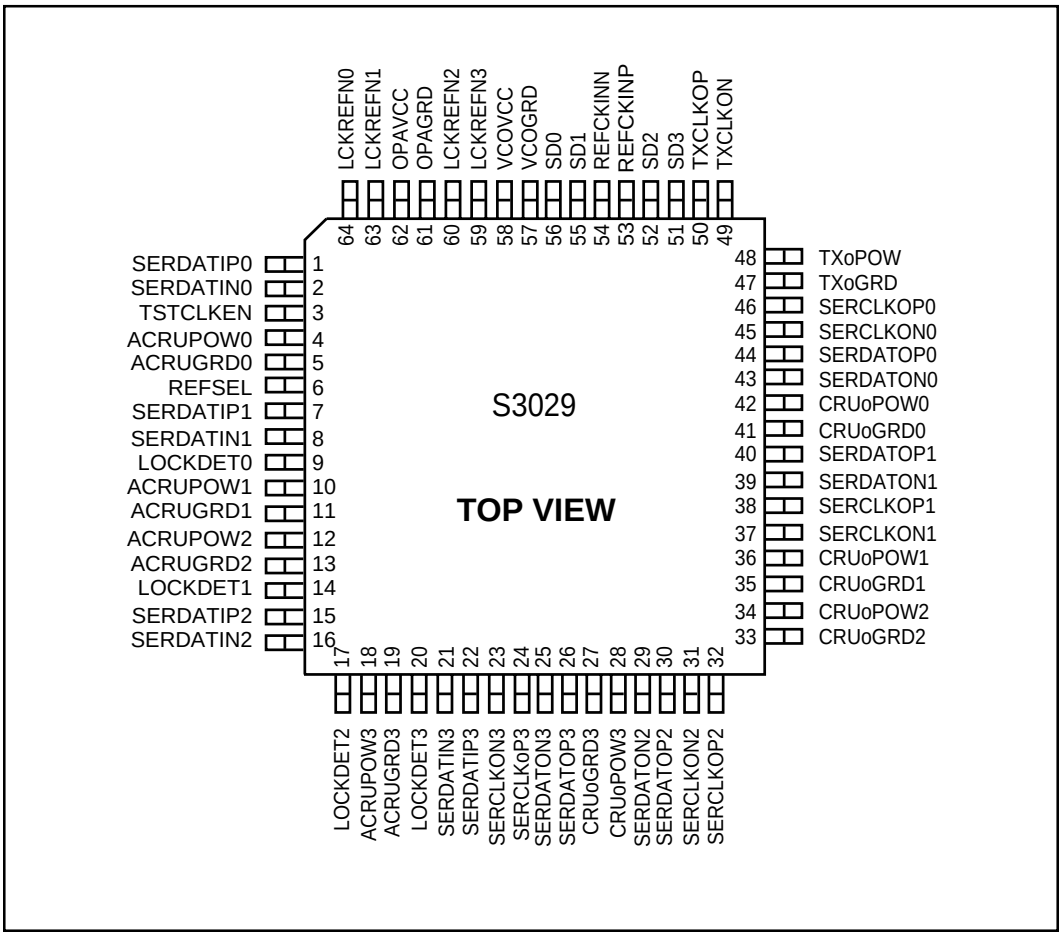
Figure 5. S3029 64 TQFP Package



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	e	b	c
MIN		0.05	1.35	11.80	9.90	11.80	9.90	0.50	0.50 BSC.	0.17	0.127
NOM			1.40	12.00	10.00	12.00	10.00	0.60		0.22	
MAX	1.60	0.15	1.45	12.20	10.10	12.20	10.10	0.75		0.27	0.17

Figure 6. S3029 64 TQFP Pinout



Performance Specifications

Parameter	Min	Typ	Max	Units	Condition
Nominal VCO Center Frequency		155.52		MHz	
Reference Clock Frequency Tolerance	-20		+20	ppm	For SONET OC-3 Transmit Frequency Tolerance
	-100		+100	ppm	For 155 Mbit/s ATM Transmit Frequency Tolerance
OC-3/STS-3					
Capture Range[1]		±200ppm			With respect to fixed reference frequency
Lock Range		+8,-12%			
Clock Output Duty Cycle	40		60	% of UI	
Acquisition Lock Time[1] OC-3/STS-3			64	µsec	With device already powered up and valid REFCLK.
Reference Clock Input Duty Cycle	30		70	% of period	
Reference Clock Rise & Fall Times			2.0	ns	10% to 90% of amplitude
PECL Output Rise & Fall Times			1.5	ns	10% to 90%, 50Ω to VCC-2V equivalent load, 5 pf cap
TXCLKOP/N Jitter Generation		.045	.07	U.I.pp	STM-1: F_3=65 KHz, F_4=1.3 MHz SONET/SDH spec limit = 0.15 U.I.

1 Guaranteed but not tested.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Ambient Temperature under Bias (industrial)	-40		+85	° C
Ambient Temperature under Bias (commercial)	0		+70	° C
Junction Temperature under Bias	-10		+130	° C
Voltage on VCC with Respect to GND	3.14	3.3	3.46	V
Voltage on Any TTL Input Pin	0.0		VCC	V
Voltage on Any PECL Input Pin	VCC -2		VCC	V
PECL Output Source Current (50Ω to Vcc-2V)		14	25	mA
ICC Supply Current		225	276	mA

Absolute Maximum Ratings

Parameter	Min	Typ	Max	Unit
Case Temperature under Bias	-55		+125	° C
Junction Temperature under Bias	-55		+150	° C
Storage Temperature	-65		+150	° C
Voltage on VCC with Respect to GND	-0.5		+7.0	V
Voltage on any TTL Input Pin	-0.5		+5.5	V
Voltage on any PECL Input Pin	VCC -2.0		VCC	V
TTL Output Sink Current			20	mA
TTL Output Source Current			10	mA
High Speed PECL Output Source Current			50	mA
Static Discharge Voltage		500		V

TTL Input/Output DC Characteristics[1]

(T_A = -40°C to +85°C, V_{CC} = 3.3 V ±5%)

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{IL}[2]	Input LOW Voltage	Guaranteed Input LOW Voltage for all inputs		0.8	Volts
V_{IH}[2]	Input HIGH Voltage	Guaranteed Input HIGH Voltage for all inputs	2.0		Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V	-400.0		uA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		50.0	uA
I_I	Input HIGH Current at Max VCC	V_{CC} = MAX, V_{IN} = 3.5V		1.0	mA
I_{OS}	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.5V	-50.0	-5.0	mA
V_{IK}	Input Clamp Diode Voltage	V_{CC} = MIN, I_{IN} = -18.0mA	-1.2		Volts
V_{OL}	TTL Output LOW Voltage	V_{CC} = MIN, I_{OL} = 2mA		0.5	Volts
V_{OH}	TTL Output HIGH Voltage	V_{CC} = MIN, I_{OH} = -.10mA	2.2		Volts

2. These input levels provide a zero–noise immunity and should only be tested in a static, noise-free environment.

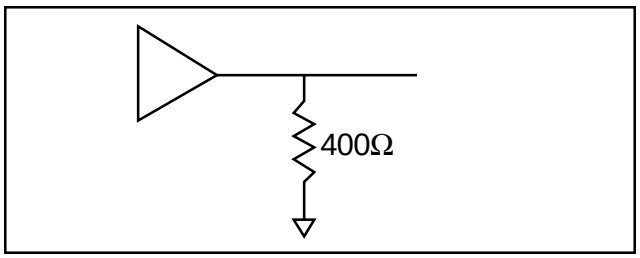
PECL Input/Output DC Characteristics[1,2]

(T_A = -40°C to +85°C, V_{CC} = 3.3V ±5%)

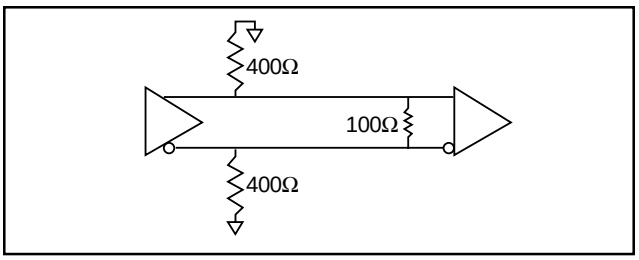
Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IL}	Input LOW Voltage	V_{CC} -2.000		V_{CC} -1.441	Volts	Guaranteed Input LOW Voltage for single-ended inputs
V_{IH}	Input HIGH Voltage	V_{CC} -1.225		V_{CC} -0.570	Volts	Guaranteed Input HIGH Voltage for single-ended inputs
V_{IL}	Input LOW Voltage	V_{CC} -2.000		V_{CC} -0.700	Volts	Guaranteed Input LOW Voltage for differential inputs
V_{IH}	Input HIGH Voltage	V_{CC} -1.750		V_{CC} -0.450	Volts	Guaranteed Input HIGH Voltage for differential inputs
V_{ID}	Input Diff. Voltage	0.200	0.500	1.400	Volts	Differential Input Voltage
I_{IHD}	Diff. Input High Current	-0.500		20.000	µA	V_{ID} = 500mV
I_{ILD}	Diff. Input Low Current	-0.500		20.000	µA	V_{ID} = 500mV
I_{IH}	Single-ended input High Current			4	mA	SD Inputs have internal 1K to GND load resistor.
I_{IL}	Single-ended input LOW Current			4	mA	SD Inputs have internal 1K to GND load resistor.
V_{OL}	Output LOW Voltage	V_{CC} -2.000		V_{CC} -1.300	Volts	400 ohm termination to GND
V_{OH}	Output HIGH Voltage	V_{CC} -1.110		V_{CC} -0.670	Volts	400 ohm termination to GND
V_{OD}	Output Diff. Voltage	0.390		1.000	Volts	Differential Output Voltage

1. These conditions will be met with no airflow.
2. When not used, tie the positive differential PECL pin to V_{CC} and the negative differential PECL pin to ground via a 3.9K resistor.

PECL Output Loading

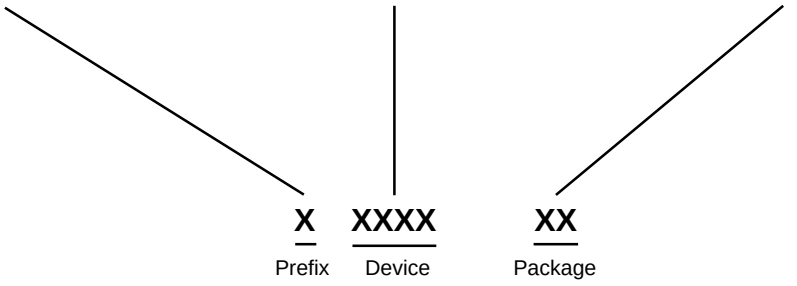


Recommended Termination of Differential PECL Signals



Ordering Information

PREFIX	DEVICE	PACKAGE
S- Integrated Circuit	3029	A – 64 TQFP



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