Freescale Semiconductor
Technical Data

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MPC8360E/MPC8358E PowerQUICC™ II Pro Processor Revision 2.x TBGA Silicon Hardware Specifications

This document provides an overview of the MPC8360E/58E PowerQUICC™ II Pro processor revision 2.x TBGA features, including a block diagram showing the major functional components. This device is a cost-effective, highly integrated communications processor that addresses the needs of the networking, wireless infrastructure and telecommunications markets. Target applications include next generation DSLAMs, network interface cards for 3G basestations (Node Bs), routers, media gateways and high end IADs. The device extends current PowerQUICC II Pro offerings, adding higher CPU performance, additional functionality, faster interfaces and robust interworking between protocols while addressing the requirements related to time-to-market, price, power, and package size. This device can be used for the control plane along with data plane functionality.

For functional characteristics of the processor, refer to the *MPC8360E Integrated Communications Processor Family Reference Manual, Rev. 2*.

To locate any published errata or updates for this document, contact your Freescale sales office.

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1 Overview

This section describes a high-level overview including features and general operation of the MPC8360E/58E PowerQUICC™ II Pro processor. A major component of this device is the e300 core which includes 32 Kbytes of instruction and data cache and is fully compatible with the PowerPC™ 603e instruction set. The new QUICC Engine™ module provides termination, interworking, and switching between a wide range of protocols including ATM, Ethernet, HDLC, and POS. The QUICC Engine module's enhanced interworking eases the transition and reduces investment costs from ATM to IP based systems. The other major features include a dual DDR SDRAM memory controller for the MPC8360E, which allows equipment providers to partition system parameters and data in an extremely efficient way, such as using one 32-bit DDR memory controller for control plane processing and the other for data plane processing. The MPC8358E has a single DDR SDRAM memory controller. The MPC8360E/58E also offers a 32-bit PCI controller, a flexible local bus, and a dedicated security engine.

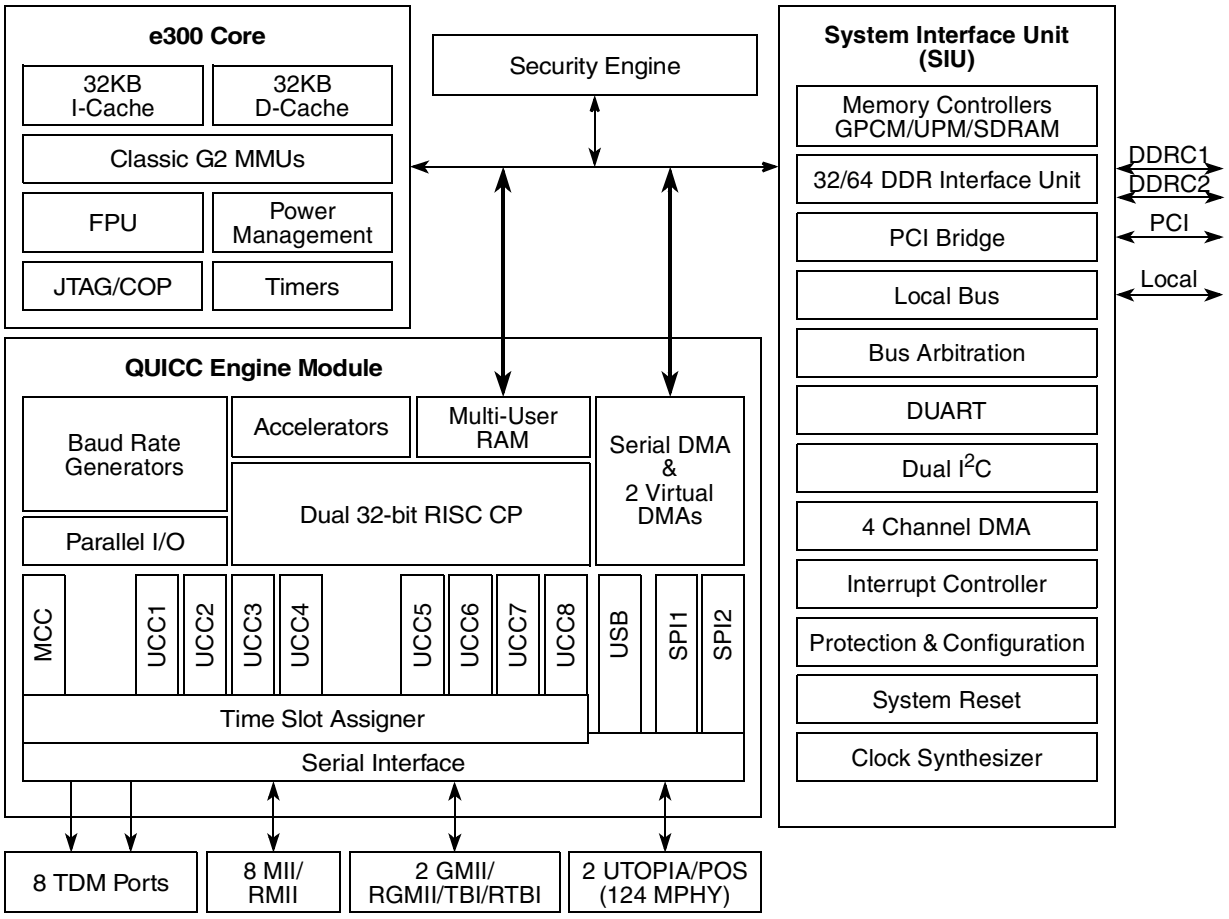


Figure 1. MPC8360E Block Diagram

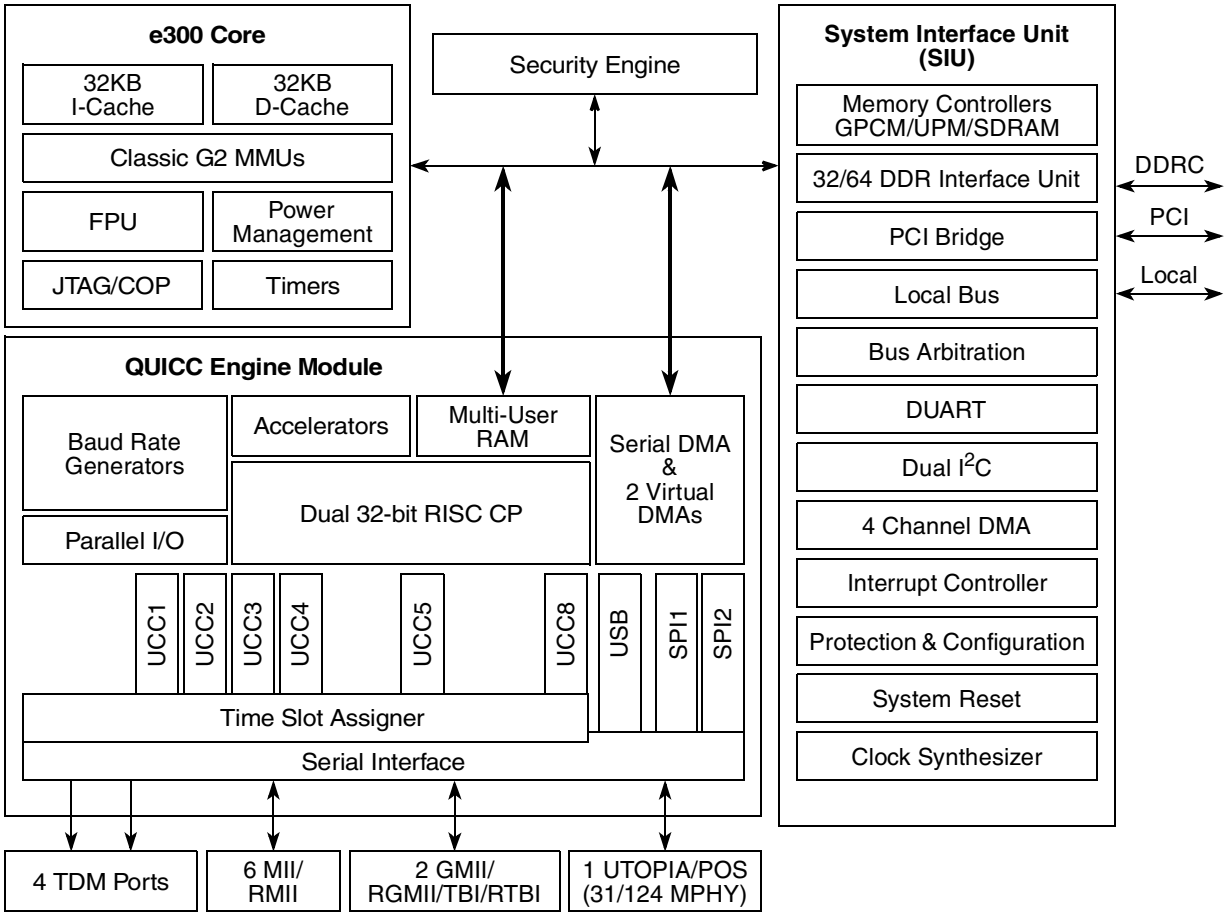


Figure 2. MPC8358E Block Diagram

Major features of the MPC8360E/58E are as follows:

- e300 PowerPC processor core (enhanced version of the MPC603e core)
  - Operates at up to 667 MHz (for the MPC8360E) and 400 MHz (for the MPC8358E)
  - High-performance, superscalar processor core
  - Floating-point, integer, load/store, system register, and branch processing units
  - 32-Kbyte instruction cache, 32-Kbyte data cache
  - Lockable portion of L1 cache
  - Dynamic power management
  - Software-compatible with the Freescale processor families implementing the Power Architecture™ technology
- QUICC Engine unit
  - Two 32-bit RISC controllers for flexible support of the communications peripherals, each operating up to 500 MHz (for the MPC8360E) and 400 MHz (for the MPC8358E)
  - Serial DMA channel for receive and transmit on all serial channels

— QE peripheral request interface (for SEC, PCI, IEEE® Std 1588™)

— Eight universal communication controllers (UCCs) on the MPC8360E and six UCCs on the MPC8358E supporting the following protocols and interfaces (not all of them simultaneously):

- **IEEE** Std. 1588 protocol supported
- 10/100 Mbps Ethernet/IEEE Std. 802.3® CDMA/CS interface through a media-independent interface (MII, RMII, RGMII)[1]
- 1000 Mbps Ethernet/IEEE Std. 802.3 CDMA/CS interface through a media-independent interface (GMII, RGMII, TBI, RTBI) on UCC1 and UCC2
- 9.6K jumbo frames
- ATM full-duplex SAR, up to 622 Mbps (OC-12/STM-4), AAL0, AAL1 and AAL5 in accordance ITU-T I.363.5
- ATM AAL2 CPS, SSSAR, and SSTED up to 155 Mbps (OC-3/STM-1) Mbps full duplex (with 4 CPS packets per cell) in accordance ITU-T I.366.1 and I.363.2
- ATM traffic shaping for CBR, VBR, UBR, and GFR traffic types compatible with ATM forum TM4.1 for up to 64K simultaneous ATM channels
- ATM AAL1 structured and unstructured circuit emulation service (CES 2.0) in accordance with ITU-T I.163.1 and ATM Forum af-vtoa-00-0078.000
- IMA (Inverse Multiplexing over ATM) for up to 31 IMA links over 8 IMA groups in accordance with the ATM forum AF-PHY-0086.000 (Version 1.0) and AF-PHY-0086.001 (Version 1.1)
- ATM Transmission Convergence layer support in accordance with ITU-T I.432
- ATM OAM handling features compatible with ITU-T I.610
- PPP, Multi-Link (ML-PPP), Multi-Class (MC-PPP) and PPP mux in accordance with the following RFCs: 1661, 1662, 1990, 2686 and 3153
- IP support for IPv4 packets including TOS, TTL and header checksum processing
- Ethernet over first mile IEEE Std. 802.3ah®
- Shim header
- Ethernet-to-Ethernet/AAL5/AAL2 inter-working
- L2 Ethernet switching using MAC address or IEEE Std. 802.1P/Q® VLAN tags
- ATM (AAL2/AAL5) to Ethernet (IP) interworking in accordance with RFC2684 including bridging of ATM ports to Ethernet ports
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics
- AAL2 protocol rate up to 4 CPS at OC-3/STM-1 rate
- Packet over Sonet (POS) up to 622-Mbps full-duplex 124 MultiPHY
- POS hardware; microcode must be loaded as an IRAM package
- Transparent up to 70-Mbps full-duplex
- HDLC up to 70-Mbps full-duplex
- HDLC BUS up to 10 Mbps

1. SMII or SGMII media-independent interface is not currently supported

  - Asynchronous HDLC
  - UART
  - BISYNC up to 2 Mbps
  - User-programmable Virtual FIFO size
  - QUICC Multichannel Controller (QMC) for 64 TDM channels
- One multichannel communication controller (MCC) only on the MPC8360E supporting the following:
  - 256 HDLC or transparent channels
  - 128 SS7 channels
  - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces
- Two UTOPIA/POS interfaces on the MPC8360E supporting 124 MultiPHY each (optional 2*128 MultiPHY with extended address) and one UTOPIA/POS interface on the MPC8358E supporting 31/124 MultiPHY
- Two serial peripheral interfaces (SPI); SPI2 is dedicated to Ethernet PHY management
- Eight TDM interfaces on the MPC8360E and four TDM interfaces on the MPC8358E with 1-bit mode for E3/T3 rates in clear channel
- Sixteen independent baud rate generators and 30 input clock pins for supplying clocks to UCC and MCC serial channels (MCC is only available on the MPC8360E)
- Four independent 16-bit timers that can be interconnected as four 32-bit timers
- Interworking functionality:
  - Layer 2 10/100-Base T Ethernet switch
  - ATM-to-ATM switching (AAL0, 2, 5)
  - Ethernet-to-ATM switching with L3/L4 support
  - PPP interworking

- Security engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, 802.11i, iSCSI, and IKE processing. The security engine contains four crypto-channels, a controller, and a set of crypto execution units (EUs).
  - Public key execution unit (PKEU) supporting the following:
    - RSA and Diffie-Hellman
    - Programmable field size up to 2048 bits
    - Elliptic curve cryptography
    - F2m and F(p) modes
    - Programmable field size up to 511 bits
  - Data encryption standard execution unit (DEU)
    - DES, 3DES
    - Two key (K1, K2) or three key (K1, K2, K3)
    - ECB and CBC modes for both DES and 3DES
  - Advanced encryption standard unit (AESU)

- Implements the Rinjdael symmetric key cipher
- Key lengths of 128, 192, and 256 bits, two key
  - ECB, CBC, CCM, and counter modes
- ARC four execution unit (AFEU)
  - Implements a stream cipher compatible with the RC4 algorithm
  - 40- to 128-bit programmable key
- Message digest execution unit (MDEU)
  - SHA with 160-, 224-, or 256-bit message digest
  - MD5 with 128-bit message digest
  - HMAC with either SHA or MD5 algorithm
- Random number generator (RNG)
- Four crypto-channels, each supporting multi-command descriptor chains
  - Static and/or dynamic assignment of crypto-execution units via an integrated controller
  - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
- Storage/NAS XOR parity generation accelerator for RAID applications

- Dual DDR SDRAM memory controllers on the MPC8360E and a single DDR SDRAM memory controller on the MPC8358E
  - Programmable timing supporting both DDR1 and DDR2 SDRAM
  - On the MPC8360E, the DDR buses can be configured as two 32-bit buses or one 64-bit bus; on the MPC8358E, the DDR bus can be configured as a 32-bit or a 64-bit bus
  - 32- or 64-bit data interface, up to 333 MHz (for the MPC8360E) and 266 MHz (for the MPC8358E) data rate
  - Four banks of memory, each up to 1 Gbyte
  - DRAM chip configurations from 64 Mbits to 1 Gigabit with x8/x16 data ports
  - Full ECC support (when the MPC8360E is configured as 2x32 bit DDR memory controllers, both support ECC)
  - Page mode support (up to 16 simultaneous open pages for DDR1, up to 32 simultaneous open pages for DDR2)
  - Contiguous or discontiguous memory mapping
  - Read-modify-write support
  - Sleep mode support for self refresh SDRAM
  - Supports auto refreshing
  - Supports source clock mode
  - On-the-fly power management using CKE
  - Registered DIMM support
  - 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2
  - External driver impedance calibration
  - On-die termination (ODT)

- PCI interface
  - PCI Specification Revision 2.3 compatible
  - Data bus widths:
    - Single 32-bit data PCI interface that operates at up to 66 MHz
  - PCI 3.3-V compatible (not 5-V compatible)
  - PCI host bridge capabilities on both interfaces
  - PCI agent mode supported on PCI interface
  - Support for PCI-to-memory and memory-to-PCI streaming
  - Memory prefetching of PCI read accesses and support for delayed read transactions
  - Support for posting of processor-to-PCI and PCI-to-memory writes
  - On-chip arbitration, supporting five masters on PCI
  - Support for accesses to all PCI address spaces
  - Parity support
  - Selectable hardware-enforced coherency
  - Address translation units for address mapping between host and peripheral
  - Dual address cycle supported when the device is the target
  - Internal configuration registers accessible from PCI
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data operating at up to 133 MHz
  - Eight chip selects support eight external slaves
  - Up to eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller
  - Three protocol engines available on a per chip select basis:
    - General-purpose chip select machine (GPCM)
    - Three user programmable machines (UPMs)
    - Dedicated single data rate SDRAM controller
  - Parity support
  - Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Programmable interrupt controller (PIC)
  - Functional and programming compatibility with the MPC8260 interrupt controller
  - Support for 8 external and 35 internal discrete interrupt sources
  - Support for one external (optional) and seven internal machine checkstop interrupt sources
  - Programmable highest priority request
  - Four groups of interrupts with programmable priority
  - External and internal interrupts directed to communication processor
  - Redirects interrupts to external $\overline{\text{INTA}}$ pin when in core disable mode
  - Unique vector number for each interrupt source

- Dual industry-standard I^2C interfaces
  - Two-wire interface
  - Multiple master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
  - System initialization data is optionally loaded from I^2C-1 EPROM by boot sequencer embedded hardware
- DMA controller
  - Four independent virtual channels
  - Concurrent execution across multiple channels with programmable bandwidth control
  - All channels accessible by local core and remote PCI masters
  - Misaligned transfer capability
  - Data chaining and direct mode
  - Interrupt on completed segment and chain
  - DMA external handshake signals: $\overline{\text{DMA\_DREQ}}$[0:3]/$\overline{\text{DMA\_DACK}}$[0:3]/$\overline{\text{DMA\_DONE}}$[0:3]. There is one set for each DMA channel. The pins are multiplexed to the parallel IO pins with other QE functions.
- DUART
  - Two 4-wire interfaces (RxD, TxD, RTS, CTS)
  - Programming model compatible with the original 16450 UART and the PC16550D
- System timers
  - Periodic interrupt timer
  - Real-time clock
  - Software watchdog timer
  - Eight general-purpose timers
- IEEE Std. 1149.1™ compliant, JTAG boundary scan
- Integrated PCI bus and SDRAM clock generation

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8360E/58E. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage For QE frequencies <500 MHz and e300 frequencies <667 MHz For a QE frequency of 500 MHz or an e300 frequency of 667 MHz		V_{DD}	 –0.3 to 1.32 –0.3 to 1.37	V	
PLL supply voltage For QE frequencies <500 MHz and e300 frequencies <667 MHz For a QE frequency of 500 MHz or an e300 frequency of 667 MHz		AV_{DD}	 –0.3 to 1.32 –0.3 to 1.37	V	
DDR and DDR2 DRAM I/O voltage DDR DDR2		GV_{DD}	 –0.3 to 2.75 –0.3 to 1.89	V	
Three-speed Ethernet I/O, MII management voltage		LV_{DD}	–0.3 to 3.63	V	
PCI, local bus, DUART, system control and power management, I^2C, SPI, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	Three-speed Ethernet signals	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	4, 5
	Local bus, DUART, CLKIN, system control and power management, I^2C, SPI, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3, 5
	PCI	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	6
Storage temperature range		T_{STG}	–55 to 150	°C	

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution: M**V_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
4. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
5. (M,L,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 3.
6. OV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 4.

2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the device. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage For QE frequencies <500 MHz and e300 frequencies <667 MHz For a QE frequency of 500 MHz or an e300 frequency of 667 MHz	V_{DD}	 1.2 V ± 60 mV 1.3 V ± 50 mV	V	1
PLL supply voltage For QE frequencies <500 MHz and e300 frequencies <667 MHz For a QE frequency of 500 MHz or an e300 frequency of 667 MHz	AV_{DD}	 1.2 V ± 60 mV 1.3 V ± 50 mV	V	1
DDR and DDR2 DRAM I/O supply voltage DDR DDR2	GV_{DD}	 2.5 V ± 125 mV 1.8V ± 90 mV	V	
Three-speed Ethernet I/O supply voltage	$LV_{DD}0$	3.3 V ± 330 mV 2.5 V ± 125 mV	V	
Three-speed Ethernet I/O supply voltage	$LV_{DD}1$	3.3 V ± 330 mV 2.5 V ± 125 mV	V	
Three-speed Ethernet I/O supply voltage	$LV_{DD}2$	3.3 V ± 330 mV 2.5 V ± 125 mV	V	
PCI, local bus, DUART, system control and power management, I^2C, SPI, and JTAG I/O voltage	OV_{DD}	3.3 V ± 330 mV	V	
Junction temperature	T_J	0 to 105	°C	2

Notes:

1. GV_{DD}, LV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.
2. .The operating conditions for junction temperature, T_J, on the 600/333/400 MHz and 500/333/500 MHz on rev2.0 silicon is 0 °C to 70 °C. Please refer to *General9* in the device errata document.

Figure 3 shows the undershoot and overshoot voltages at the interfaces of the device.

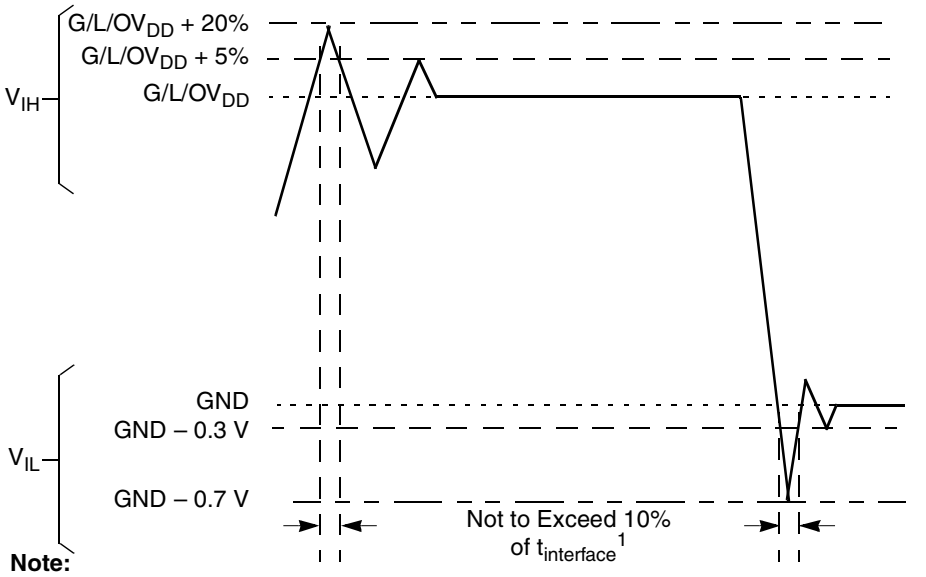


Figure 3. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$

Figure 4 shows the undershoot and overshoot voltage of the PCI interface of the device for the 3.3-V signals, respectively.

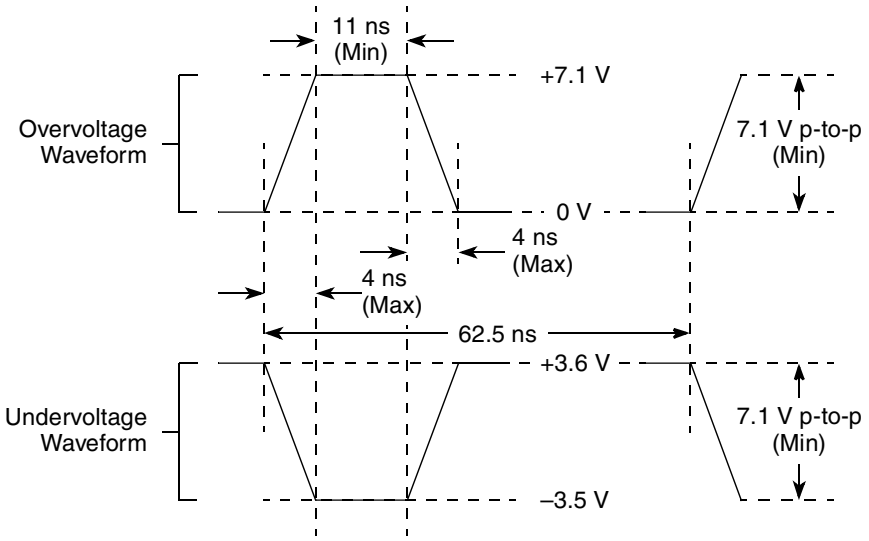


Figure 4. Maximum AC Waveforms on PCI interface for 3.3-V Signaling

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	OV_{DD} = 3.3 V
PCI signals	25	
PCI output clocks (including PCI_SYNC_OUT)	42	
DDR signal	20 36 (half strength mode) [1]	GV_{DD} = 2.5 V
DDR2 signal	18 36 (half strength mode) [1]	GV_{DD} = 1.8 V
10/100/1000 Ethernet signals	42	LV_{DD} = 2.5/3.3 V
DUART, system control, I^2C, SPI, JTAG	42	OV_{DD} = 3.3 V
GPIO signals	42	OV_{DD} = 3.3 V LV_{DD} = 2.5/3.3 V

[1] DDR output impedance values for half strength mode are verified by design and not tested

2.2 Power Sequencing

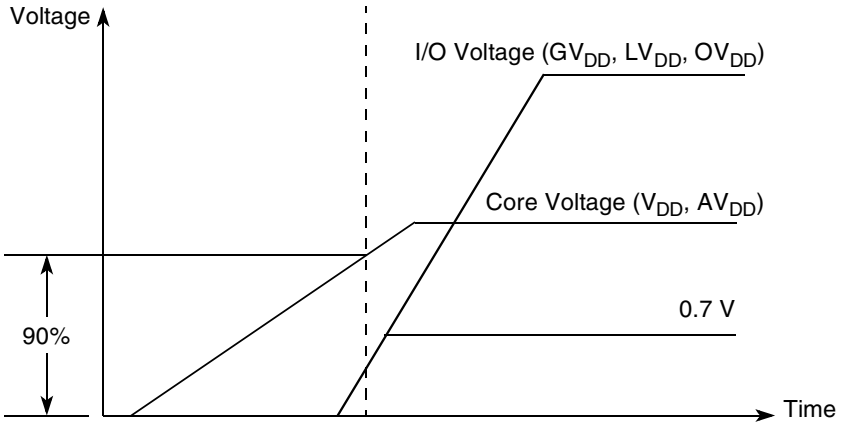
This section details the power sequencing considerations for the MPC8360E/58E.

2.2.1 Power-Up Sequencing

MPC8360E/58E does not require the core supply voltage (V_{DD} and AV_{DD}) and I/O supply voltages (GV_{DD}, LV_{DD}, and OV_{DD}) to be applied in any particular order. During the power ramp up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there may be a period of time that all input and output pins will actively be driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD}, LV_{DD}, and OV_{DD}) and assert $\overline{\text{PORESET}}$ before the power

supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V, see Figure 5.

Figure 5. Power Sequencing Example



I/O voltage supplies (GV_{DD}, LV_{DD}, and OV_{DD}) do not have any ordering requirements with respect to one another.

2.2.2 Power-Down Sequencing

The MPC8360E/58E does not require the core supply voltage and I/O supply voltages to be powered-down in any particular order.

3 Power Characteristics

The estimated typical power dissipation values are shown in Table 4 and Table 5.

Table 4. MPC8360E TBGA Core Power Dissipation[1]

Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
266	266	500	5.0	5.6	W	2, 3, 5
400	266	400	4.5	5.0	W	2, 3, 4
533	266	400	4.8	5.3	W	2, 3, 4
667	333	400	5.8	6.3	W	3, 6, 7, 8
500	333	500	5.9	6.4	W	3, 6, 7, 8

Table 4. MPC8360E TBGA Core Power Dissipation[1] (continued)

Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
667	333	500	6.1	6.8	W	2, 3, 5, 9

Notes:
1. The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}. For I/O power values, see Table 6.
2. Typical power is based on a voltage of V_{DD} = 1.2 V or 1.3 V, a junction temperature of T_J = 105°C, and a Dhrystone benchmark application.
3. Thermal solutions will likely need to design to a value higher than typical power on the end application, T_A target, and I/O power.
4. Maximum power is based on a voltage of V_{DD} = 1.2 V, WC process, a junction T_J = 105°C, and an artificial smoke test.
5. Maximum power is based on a voltage of V_{DD} = 1.3 V for applications that use 667MHz(CPU)/500(QE) with WC process, a junction T_J = 105°C, and an artificial smoke test.
6. Typical power is based on a voltage of V_{DD} = 1.3 V, a junction temperature of T_J = 70°C, and a Dhrystone benchmark application.
7. Maximum power is based on a voltage of V_{DD} = 1.3 V for applications that use 667MHz(CPU) or 500(QE) with WC process, a junction T_J = 70°C, and an artificial smoke test.
8. This frequency combination is only available for rev2.0 silicon.
9. This frequency combination is not available for rev2.0 silicon.

Table 5. MPC8358E TBGA Core Power Dissipation[1]

Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
266	266	300	4.1	4.5	W	2, 3, 4
400	266	400	4.5	5.0	W	2, 3, 4

Notes:
1. The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}. For I/O power values, see Table 6.
2. Typical power is based on a voltage of V_{DD} = 1.2 V, a junction temperature of T_J = 105°C, and a Dhrystone benchmark application.
3. Thermal solutions will likely need to design to a value higher than typical power on the end application, T_A target, and I/O power.
4. Maximum power is based on a voltage of V_{DD} = 1.2 V, WC process, a junction T_J = 105°C, and an artificial smoke test.

Table 6 shows the estimated typical I/O power dissipation for the device.

Table 6. Estimated Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	Unit	Comments
DDR I/O 65% utilization R_s = 20 Ω R_t = 50 Ω 2 pairs of clocks	200 MHz, 1x32 bits	0.3	0.46				W	
	200 MHz, 1x64 bits	0.4	0.58				W	
	200 MHz, 2x32 bits	0.6	0.92				W	
	266 MHz, 1x32 bits	0.35	0.56				W	
	266 MHz, 1x64 bits	0.46	0.7				W	
	266 MHz, 2x32 bits	0.7	1.11				W	
	333 MHz, 1x32 bits	0.4	0.65				W	
	333 MHz, 1x64 bits	0.53	0.82				W	
	333 MHz, 2x32 bits	0.81	1.3				W	
Local Bus I/O Load = 25 pf 3 pairs of clocks	133 MHz, 32 bits			0.22			W	
	83 MHz, 32 bits			0.14			W	
	66 MHz, 32 bits			0.12			W	
	50 MHz, 32 bits			0.09			W	
PCI I/O Load = 30 pf	33 MHz, 32 bits			0.05			W	
	66 MHz, 32 bits			0.07			W	
10/100/1000 Ethernet I/O Load = 20 pf	MII or RMII				0.01		W	Multiply by number of interfaces used.
	GMII or TBI				0.04		W	
	RGMII or RTBI					0.04	W	
Other I/O				0.1			W	

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8360E/58E.

4.1 DC Electrical Characteristics

Table 7 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the device.

Table 7. CLKIN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V
CLKIN input current	$0 V \le V_{IN} \le OV_{DD}$	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	$0 V \le V_{IN} \le 0.5V$ or $OV_{DD} – 0.5V \le V_{IN} \le OV_{DD}$	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	$0.5 V \le V_{IN} \le OV_{DD} – 0.5 V$	I_{IN}	—	±100	μA

4.2 AC Electrical Characteristics

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Table 8 provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the device.

Table 8. CLKIN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
CLKIN/PCI_CLK frequency	f_{CLKIN}	—	—	66.67	MHz	1
CLKIN/PCI_CLK cycle time	t_{CLKIN}	15	—	—	ns	—
CLKIN/PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t_{KHK}/t_{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	±150	ps	4, 5

Notes:

1. **Caution:** The system, core, USB, security, and 10/100/1000 Ethernet must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8360E/58E.

5.1 RESET DC Electrical Characteristics

Table 9 provides the DC electrical characteristics for the RESET pins of the device.

Table 9. RESET Pins DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}		2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}		–0.3	0.8	V
Input current	I_{IN}			±10	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:
1. This table applies for pins $\overline{\text{PORESET}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$ and $\overline{\text{QUIESCE}}$.
2. $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

5.2 RESET AC Electrical Characteristics

This section describes the AC electrical specifications for the reset initialization timing requirements of the device. Table 10 provides the reset initialization AC timing specifications for the DDR SDRAM component(s).

Table 10. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$ or $\overline{\text{SRESET}}$ (input) to activate reset flow	32	—	$t_{PCI\_SYNC\_IN}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to CLKIN when the device is in PCI host mode	32	—	t_{CLKIN}	2
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to PCI_SYNC_IN when the device is in PCI agent mode	32	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$/$\overline{\text{SRESET}}$ assertion (output)	512	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$ negation to $\overline{\text{SRESET}}$ negation (output)	16	—	$t_{PCI\_SYNC\_IN}$	1
Input setup time for POR config signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR config signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI agent mode	4	—	$t_{PCI\_SYNC\_IN}$	1
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	

Table 10. RESET Initialization Timing Specifications (continued)

Time for the device to turn off POR config signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the device to turn on POR config signals with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{PCI\_SYNC\_IN}$	1, 3

Notes:

1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8360E Integrated Communications Processor Reference Manual, Rev. 2* for more details.
2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the device is in PCI host mode. See the *MPC8360E Integrated Communications Processor Reference Manual, Rev. 2* for more details.
3. POR config signals consists of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 11 provides the PLL and DLL lock times.

Table 11. PLL and DLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	µs	
DLL lock times	7680	122,880	csb_clk cycles	1, 2

Notes:

1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The csb_clk is determined by the CLKIN and system PLL ratio. See Section 22, "Clocking," for more information.

5.3 QE Operating Frequency Limitations

This section specify the limits of the AC electrical characteristics for the operation of the QE's communication interfaces.

NOTE

The settings listed below are required for correct hardware interface operation. Each protocol by itself requires a minimal QE operating frequency setting for meeting the performance target. Because the performance is a complex function of all the QE settings, the user should make use of the QE performance utility tool provided by Freescale to validate their system.

Table 12 lists the maximal QE I/O frequencies and the minimal QE core frequency for each interface.

Table 12. QE Operating Frequency Limitations

Interface	Interface Operating Frequency (MHz)	Max interface Bit Rate (Mbps)	Min QE Operating Frequency[1] (MHz)	Notes
Ethernet Management: MDC/MDIO	10 (max)	10	20	
MII	25 (typ)	100	50	

Table 12. QE Operating Frequency Limitations (continued)

Interface	Interface Operating Frequency (MHz)	Max interface Bit Rate (Mbps)	Min QE Operating Frequency[1] (MHz)	Notes
RMII	50 (typ)	100	50	
GMII/RGMII/TBI/RTBI	125 (typ)	1000	250	
SPI (master/slave)	10 (max)	10	20	
UCC through TDM	50 (max)	70	8 × F	2
MCC	25 (max)	16.67	16 × F	2, 4
UTOPIA L2	50 (max)	800	2 × F	2
POS-PHY L2	50 (max)	800	2 × F	2
HDLC Bus	10 (max)	10	20	
HDLC/Transparent	50 (max)	50	8/3 × F	2, 3
UART/Async HDLC	3.68 (max internal ref clock)	115 (Kbps)	20	
BISYNC	2 (max)	2	20	
USB	48 (ref clock)	12	96	

Note:
1. The QE needs to run at a frequency higher than or equal to what is listed in this table.
2. 'F' is the actual interface operating frequency.
3. The bit rate limit is independent of the data bus width (i.e. the same for serial, nibble, or octal interfaces).
4. TDM in high-speed mode for serial data interface.

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR and DDR2 SDRAM interface of the MPC8360E/58E.

6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

Table 13 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the device when GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.125	GV_{DD} + 0.3	V	
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.125	V	

Table 13. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V (continued)

Output leakage current	I_{OZ}	—	±10	μA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	
MV_{REF} input leakage current	I_{VREF}	—	±10	μA	
Input current (0 V ≤V_{IN} ≤ OV_{DD})	I_{IN}	—	±10	μA	

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to equal 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} cannot exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to equal MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 14 provides the DDR2 capacitance when GV_{DD}(typ) = 1.8 V.

Table 14. DDR2 SDRAM Capacitance for GV_{DD}(typ)=1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 15 provides the recommended operating conditions for the DDR SDRAM component(s) of the device when GV_{DD}(typ) = 2.5 V.

Table 15. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.18	GV_{DD} + 0.3	V	
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.18	V	
Output leakage current	I_{OZ}	—	±10	μA	4
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–15.2	—	mA	
Output low current (V_{OUT} = 0.35 V)	I_{OL}	15.2	—	mA	
MV_{REF} input leakage current	I_{VREF}	—	±10	μA	

Table 15. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V (continued)

Input current (0 V ≤V_{IN} ≤ OV_{DD})	I_{IN}	—	±10	μA	

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 16 provides the DDR capacitance when GV_{DD}(typ) = 2.5 V.

Table 16. DDR SDRAM Capacitance for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak to peak) = 0.2 V.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

Table 17 provides the input AC timing specifications for the DDR2 SDRAM interface when GV_{DD}(typ) = 1.8 V.

Table 17. DDR2 SDRAM Input AC Timing Specifications for GV_{DD}(typ) = 1.8 V

At recommended operating conditions with GV_{DD} of 1.8 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V	
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V	

Table 18 provides the input AC timing specifications for the DDR SDRAM interface when GV_{DD}(typ) = 2.5 V.

Table 18. DDR SDRAM Input AC Timing Specifications Mode for GV_{DD}(typ) = 2.5 V

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V	

Table 18. DDR SDRAM Input AC Timing Specifications Mode for GV_{DD}(typ) = 2.5 V (continued)

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V	

Notes:

1. Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if 0 ≤ n ≤ 7) or ECC (MECC[{0...7}] if n = 8).

Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications Mode for GV_{DD}(typ) = 2.5 V

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
MDQS—MDQ/MECC input skew per byte 333 MHz 266 MHz 200 MHz	t_{DISKEW}	 -750 -1125 -1250	 750 1125 1250	ps	1, 2

Notes:

1. AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.
2. Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if 0 ≤ n ≤ 7) or ECC (MECC[{0...7}] if n = 8).

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20 and Table 21 provide the output AC timing specifications and measurement conditions for the DDR and DDR2 SDRAM interface.

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) ± 5%.

Parameter [8]	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time, (MCK[n]/$\overline{\text{MCK}}$[n] crossing)	t_{MCK}	6	10	ns	2
Skew between any MCK to ADDR/CMD 333 MHz 266 MHz 200 MHz	t_{AOSKEW}	 -1.0 -1.1 -1.2	 0.2 0.3 0.4	ns	3
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHAS}	 2.1 2.8 3.5	—	ns	4
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz - DDR1 266 MHz - DDR2 200 MHz	t_{DDKHAX}	 2.0 2.72.8 3.5	—	ns	4
$\overline{\text{MCS}}$(n) output setup with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHCS}	 2.1 2.8 3.5	—	ns	4

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)

Parameter [8]	Symbol [1]	Min	Max	Unit	Notes
$\overline{\text{MCS}}$(n) output hold with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHCX}	 2.0 2.7 3.5	—	ns	4
MCK to MDQS	t_{DDKHMH}	–0.8	0.7	ns	5, 9
MDQ/MECC/MDM output setup with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDS}, t_{DDKLDS}	 0.7 1.0 1.2	—	ns	6
MDQ/MECC/MDM output hold with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDX}, t_{DDKLDX}	 0.7 1.0 1.2	—	ns	6
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	7
MDQS epilogue end	t_{DDKHME}	–0.6	0.9	ns	7

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. In the source synchronous mode, MCK/$\overline{\text{MCK}}$ can be shifted in 1/4 applied cycle increments through the Clock Control Register. For the skew measurements referenced for t_{AOSKEW} it is assumed that the clock adjustment is set to align the address/command valid with the rising edge of MCK.
4. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.
5. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. In source synchronous mode, this will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8360E Integrated Communications Processor Reference Manual, Rev. 2* for a description and understanding of the timing modifications enabled by use of these bits.
6. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the device.
7. All outputs are referenced to the rising edge of MCK(n) at the pins of the device. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
8. AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.
9. In rev2.0 silicon, t_{DDKHMH} maximum meets the specification of 0.6ns. In rev 2.0 silicon, due to errata, t_{DDKHMH} minimum is -0.9 ns. Please refer to *DDR18* in the device errata document.

Figure 6 shows the DDR SDRAM output timing for address skew with respect to any MCK.

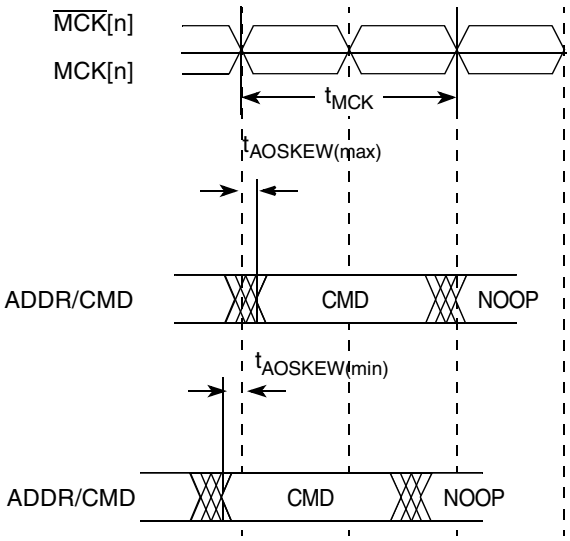


Figure 6. Timing Diagram for t_{AOSKEW} Measurement

Figure 7 provides the AC test load for the DDR bus.

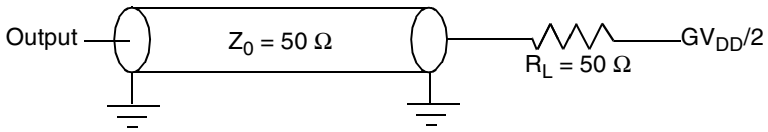


Figure 7. DDR AC Test Load

Table 21. DDR and DDR2 SDRAM Measurement Conditions

Symbol	DDR	DDR2	Unit	Notes
V_{TH}	MV_{REF} ± 0.31 V	MV_{REF} ± 0.25 V	V	1
V_{OUT}	0.5 × GV_{DD}	0.5 × GV_{DD}	V	2

Notes:

1. Data input threshold measurement point.
2. Data output measurement point.

Figure 8 shows the DDR SDRAM output timing diagram for source synchronous mode.

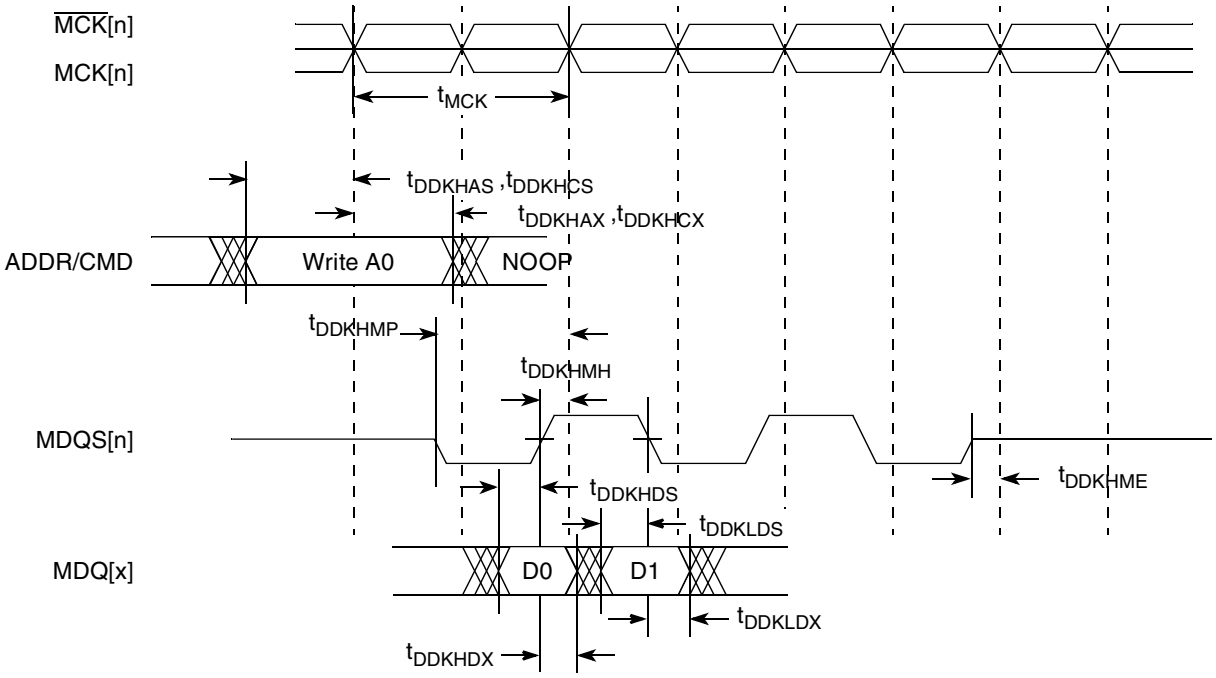


Figure 8. DDR SDRAM Output Timing Diagram for Source Synchronous Mode

Table 22 provides approximate delay information that can be expected for the address and command signals of the DDR controller for various loadings, which can be useful for a system utilizing the DLL. These numbers are the result of simulations for one topology. The delay numbers will strongly depend on the topology used. These delay numbers show the total delay for the address and command to arrive at the DRAM devices. The actual delay could be different than the delays seen in simulation, depending on the system topology. If a heavily loaded system is used, the DLL loop may need to be adjusted to meet setup requirements at the DRAM.

Table 22. Expected Delays for Address/Command

Load	Delay	Unit
4 devices (12 pF)	3.0	ns
9 devices (27 pF)	3.6	ns
36 devices (108 pF) + 40 pF compensation capacitor	5.0	ns
36 devices (108 pF) + 80 pF compensation capacitor	5.2	ns

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8360E/58E.

7.1 DUART DC Electrical Characteristics

Table 23 provides the DC electrical characteristics for the DUART interface of the device.

Table 23. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V	
Low-level input voltage OV_{DD}	V_{IL}	–0.3	0.8	V	
High-level output voltage, I_{OH} = –100 µA	V_{OH}	OV_{DD} – 0.4	—	V	
Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V	
Input current ($0 V \le V_{IN} \le OV_{DD}$)	I_{IN}	—	±10	µA	1

Note:

1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

Table 24 provides the AC timing parameters for the DUART interface of the device.

Table 24. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	—	2

Notes:

1. Actual attainable baud rate will be limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

8 UCC Ethernet Controller: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

8.1 Three-Speed Ethernet Controller (10/100/1000 Mbps)—GMII/MII/RMII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all GMII (gigabit media independent interface), MII (media independent interface), RMII (reduced media independent interface), TBI (ten-bit interface), RGMII (reduced gigabit media independent interface), and RTBI (reduced ten-bit interface) signals except MDIO (management data input/output) and MDC (management data clock). The MII, RMII, GMII and TBI interfaces are only defined for 3.3V, while the RGMII and RTBI interfaces are only defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for the MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

8.1.1 10/100/1000 Ethernet DC Electrical Characteristics

All GMII, MII, RMII, TBI, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 25 and Table 26. The potential applied to the input of a GMII, MII, RMII, TBI, RGMII, or RTBI receiver may exceed the potential of the receiver's power supply (i.e., a RGMII driver powered from a 3.6-V supply driving V_{OH} into a RGMII receiver powered from a 2.5 V supply). Tolerance for dissimilar RGMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 25. RGMII/RTBI, GMII, TBI, MII, and RMII DC Electrical Characteristics (when operating at 3.3 V)

Parameter	Symbol	Conditions		Min	Max	Unit	Notes
Supply voltage 3.3 V	LV_{DD}	—		2.97	3.63	V	1
Output high voltage	V_{OH}	IOH = –4.0 mA	LV_{DD} = Min	2.40	LV_{DD} + 0.3	V	
Output low voltage	V_{OL}	IOL = 4.0 mA	LV_{DD} = Min	GND	0.50	V	
Input high voltage	V_{IH}	—	—	2.0	LV_{DD} + 0.3	V	
Input low voltage	V_{IL}	—	—	–0.3	0.90	V	
Input current	I_{IN}	$0 V \le V_{IN} \le LV_{DD}$		—	±10	μA	

Note:
1. GMII/MII pins that are not needed for RGMII, RMII or RTBI operation are powered by the OV_{DD} supply.

Table 26. RGMII/RTBI DC Electrical Characteristics (when operating at 2.5 V)

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	IOH = –1.0 mA	LV_{DD} = Min	2.00	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD} = Min	GND – 0.3	0.40	V
Input high voltage	V_{IH}	—	LV_{DD} = Min	1.7	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	LV_{DD} = Min	–0.3	0.70	V
Input current	I_{IN}	$0 V \le V_{IN} \le LV_{DD}$		—	±10	μA

8.2 GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

8.2.1 GMII Timing Specifications

This sections describe the GMII transmit and receive AC timing specifications.

8.2.1.1 GMII Transmit AC Timing Specifications

Table 27 provides the GMII transmit AC timing specifications.

Table 27. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} / OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns	
GTX_CLK duty cycle	$t_{GTXH/tGTX}$	40	—	60	%	
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX} t_{GTKHDV}	0.5 —	—	— 5.0	ns	3
GTX_CLK clock rise time, VIL(min) to VIH(max)	t_{GTXR}	—	—	1.0	ns	
GTX_CLK clock fall time, VIH(max) to VIL(min)	t_{GTXF}	—	—	1.0	ns	
GTX_CLK125 clock period	t_{G125}	—	8.0	—	ns	2
GTX_CLK125 reference clock duty cycle measured at $LV_{DD/2}$	t_{G125H}/t_{G125}	45	—	55	%	2

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This symbol is used to represent the external GTX_CLK125 signal and does not follow the original symbol naming convention.
3. In rev 2.0 silicon, due to errata, t_{GTKHDX} minimum and t_{GTKHDV} maximum are not supported when the GTX_CLK is selected. Please refer to *QE_ENET18* in the device errata document.

Figure 9 shows the GMII transmit AC timing diagram.

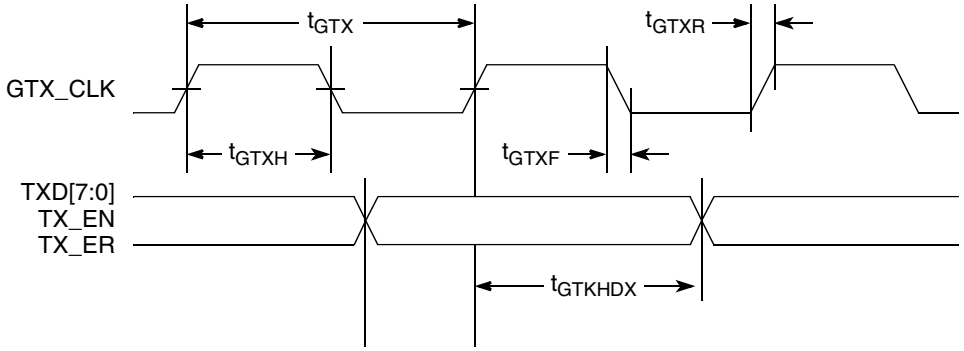


Figure 9. GMII Transmit AC Timing Diagram

8.2.1.2 GMII Receive AC Timing Specifications

Table 28 provides the GMII receive AC timing specifications.

Table 28. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} / OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
RX_CLK clock period	t_{GRX}	—	8.0	—	ns	
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	%	
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns	
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.2	—	—	ns	2
RX_CLK clock rise time, VIL(min) to VIH(max)	t_{GRXR}	—	—	1.0	ns	
RX_CLK clock fall time, VIH(max) to VIL(min)	t_{GRXF}	—	—	1.0	ns	

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In rev 2.0 silicon, due to errata, t_{GRDXKH} minimum is 0.5 which is not compliant with the standard. Please refer to *QE_ENET18* in the device errata document.

Figure 10 shows the GMII receive AC timing diagram.

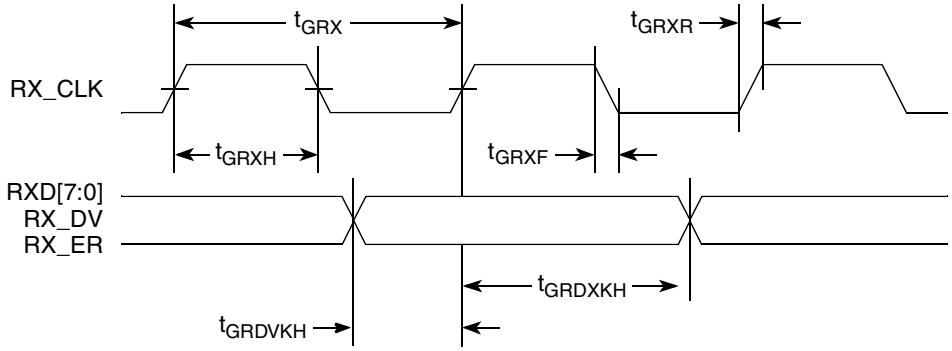


Figure 10. GMII Receive AC Timing Diagram

8.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.2.1 MII Transmit AC Timing Specifications

Table 29 provides the MII transmit AC timing specifications.

Table 29. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} / OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX} t_{MTKHDV}	1 —	5	— 15	ns
TX_CLK data clock rise time, VIL(min) to VIH(max)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall time, VIH(max) to VIL(min)	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 11 shows the MII transmit AC timing diagram.

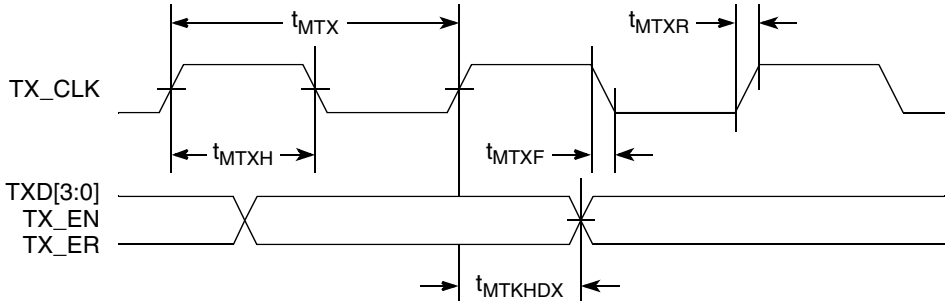


Figure 11. MII Transmit AC Timing Diagram

8.2.2.2 MII Receive AC Timing Specifications

Table 30 provides the MII receive AC timing specifications.

Table 30. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} / OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise time, VIL(min) to VIH(max)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time, VIH(max) to VIL(min)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 12 provides the AC test load.

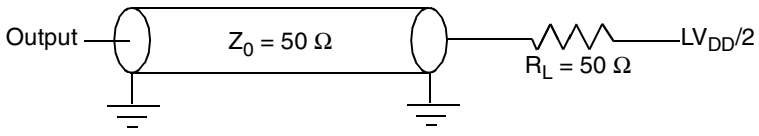


Figure 12. AC Test Load

Figure 13 shows the MII receive AC timing diagram.

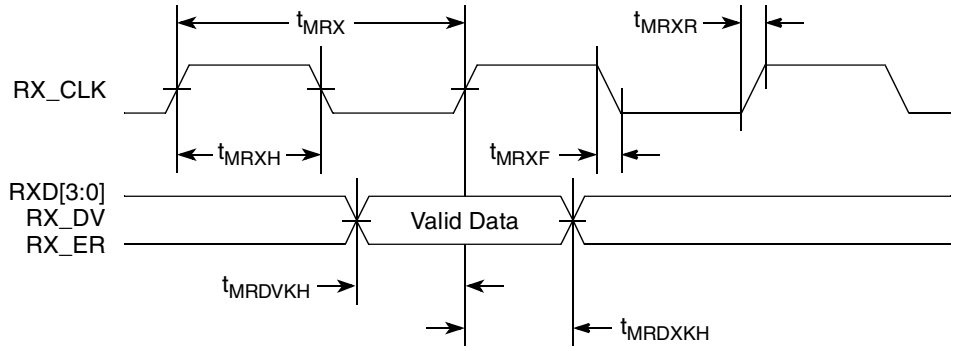


Figure 13. MII Receive AC Timing Diagram

8.2.3 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.3.1 RMII Transmit AC Timing Specifications

Table 31 provides the RMII transmit AC timing specifications.

Table 31. RMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} / OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$ $t_{RMTKHDV}$	2 —	—	— 10	ns
REF_CLK data clock rise time, VIL(min) to VIH(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall time, VIH(max) to VIL(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 14 shows the RMII transmit AC timing diagram.

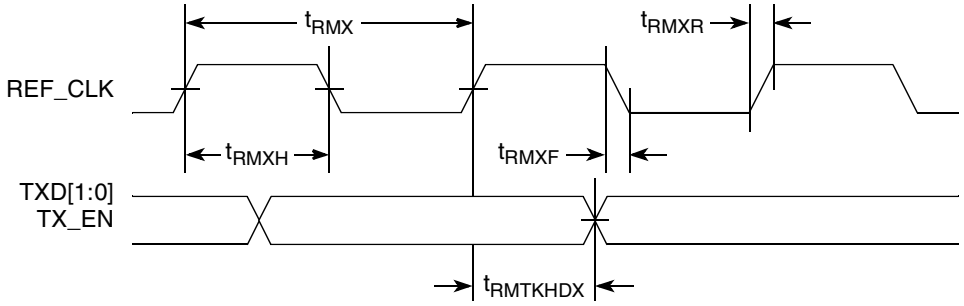


Figure 14. RMII Transmit AC Timing Diagram

8.2.3.2 RMII Receive AC Timing Specifications

Table 32 provides the RMII receive AC timing specifications.

Table 32. RMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} / OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise time, VIL(min) to VIH(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time, VIH(max) to VIL(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 15 provides the AC test load.

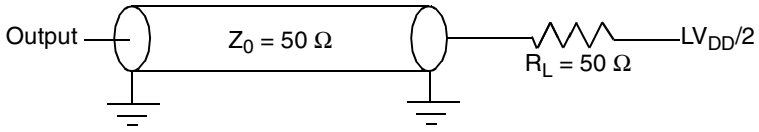


Figure 15. AC Test Load

Figure 16 shows the RMII receive AC timing diagram.

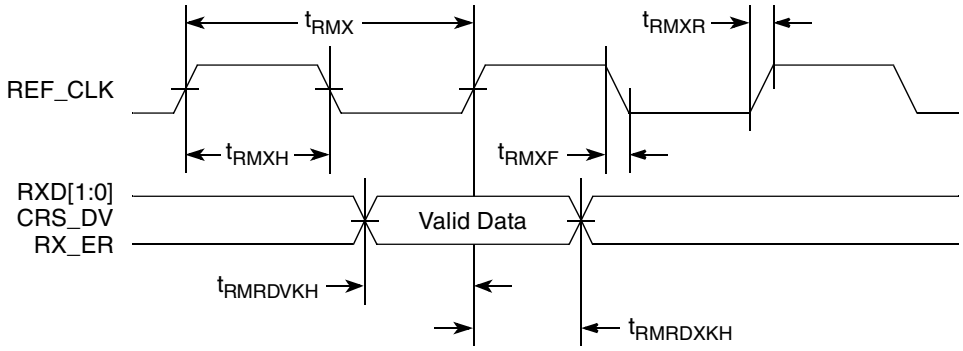


Figure 16. RMII Receive AC Timing Diagram

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.1 TBI Transmit AC Timing Specifications

Table 33 provides the TBI transmit AC timing specifications.

Table 33. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} / OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns	
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	40	—	60	%	
GTX_CLK to TBI data TCG[9:0] delay	t_{TTKHDX} t_{TTKHDV}	1.0 —	—	— 5.0	ns	3
GTX_CLK clock rise time, VIL(min) to VIH(max)	t_{TTXR}	—	—	1.0	ns	
GTX_CLK clock fall time, VIH(max) to VIL(min)	t_{TTXF}	—	—	1.0	ns	
GTX_CLK125 reference clock period	t_{G125}	—	8.0	—	ns	2
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	45	—	55	ns	

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
3. In rev 2.0 silicon, due to errata, t_{TTKHDX} minimum is 0.7 ns for UCC1. Please refer to *QE_ENET19* in the device errata document.

Figure 17 shows the TBI transmit AC timing diagram.

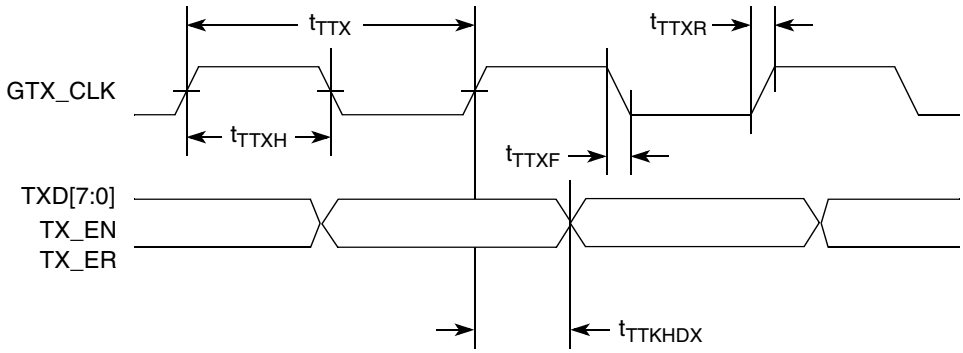


Figure 17. TBI Transmit AC Timing Diagram

8.2.4.2 TBI Receive AC Timing Specifications

Table 34 provides the TBI receive AC timing specifications.

Table 34. TBI Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} / OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
PMA_RX_CLK clock period	t_{TRX}		16.0		ns	
PMA_RX_CLK skew	t_{SKTRX}	7.5	—	8.5	ns	
RX_CLK duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%	
RCG[9:0] setup time to rising PMA_RX_CLK	t_{TRDVKH}	2.5	—	—	ns	2
RCG[9:0] hold time to rising PMA_RX_CLK	t_{TRDXKH}	1.0	—	—	ns	2
RX_CLK clock rise time, VIL(min) to VIH(max)	t_{TRXR}	0.7	—	2.4	ns	
RX_CLK clock fall time, VIH(max) to VIL(min)	t_{TRXF}	0.7	—	2.4	ns	

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
2. Setup and hold time of even numbered RCG are measured from riding edge of PMA_RX_CLK1. Setup and hold time of odd numbered RCG are measured from riding edge of PMA_RX_CLK0.

Figure 18 shows the TBI receive AC timing diagram.

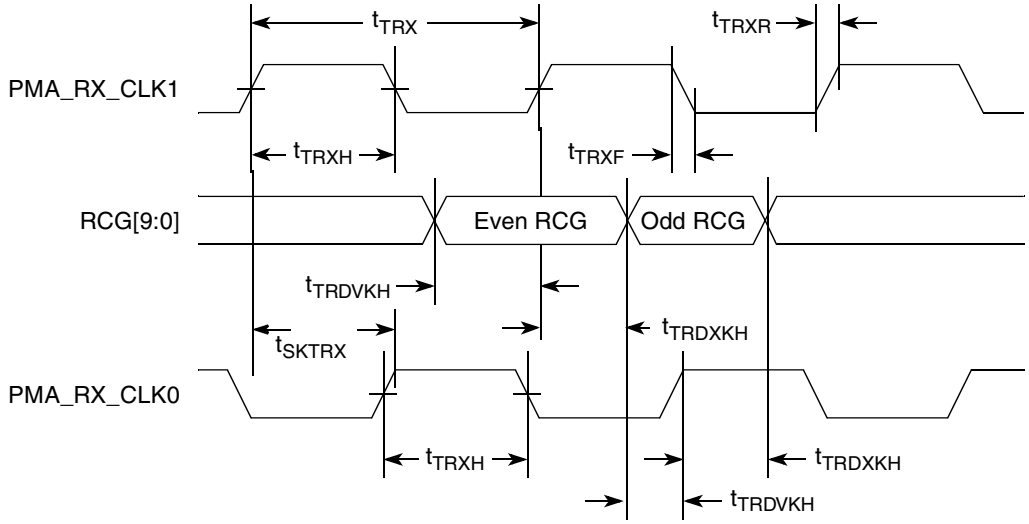


Figure 18. TBI Receive AC Timing Diagram

8.2.5 RGMII and RTBI AC Timing Specifications

Table 35 presents the RGMII and RTBI AC timing specifications.

Table 35. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	$t_{SKRGTKHDX}$ $t_{SKRGTKHDV}$	–0.5 —	—	— 0.5	ns	7
Data to clock input skew (at receiver)	$t_{SKRGDXKH}$ $t_{SKRGDVKH}$	1.0 —	—	— 2.6	ns	2
Clock cycle duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 1000Base-T	t_{RGTH}/t_{RGT}	45	50	55	%	4, 5
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 5
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns	
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns	
GTX_CLK125 reference clock period	t_{G125}	—	8.0	—	ns	6

Table 35. RGMII and RTBI AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	47	—	53	%	

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Duty cycle reference is $LV_{DD}/2$.
6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
7. In rev 2.0 silicon, due to errata, $t_{SKRGTKHDX}$ minimum is -2.3 ns and $t_{SKRGTKHDV}$ maximum is 1 ns for UCC1, 1.2 ns for UCC2 option 1, and 1.8 for UCC2 option 2. In rev2.1 silicon, due to errata, $t_{SKRGTKHDX}$ minimum is -0.65 ns for UCC2 option 1 and -0.9 for UCC2 option 2, and $t_{SKRGTKHDV}$ maximum is 0.75 ns for UCC1 and UCC2 option 1 and 0.85 for UCC2 option 2. Please refer to *QE_ENET10* in the device errata document. UCC1 does meet $t_{SKRGTKHDX}$ minimum for rev2.1 silicon.

Figure 19 shows the RGMII and RTBI AC timing and multiplexing diagrams.

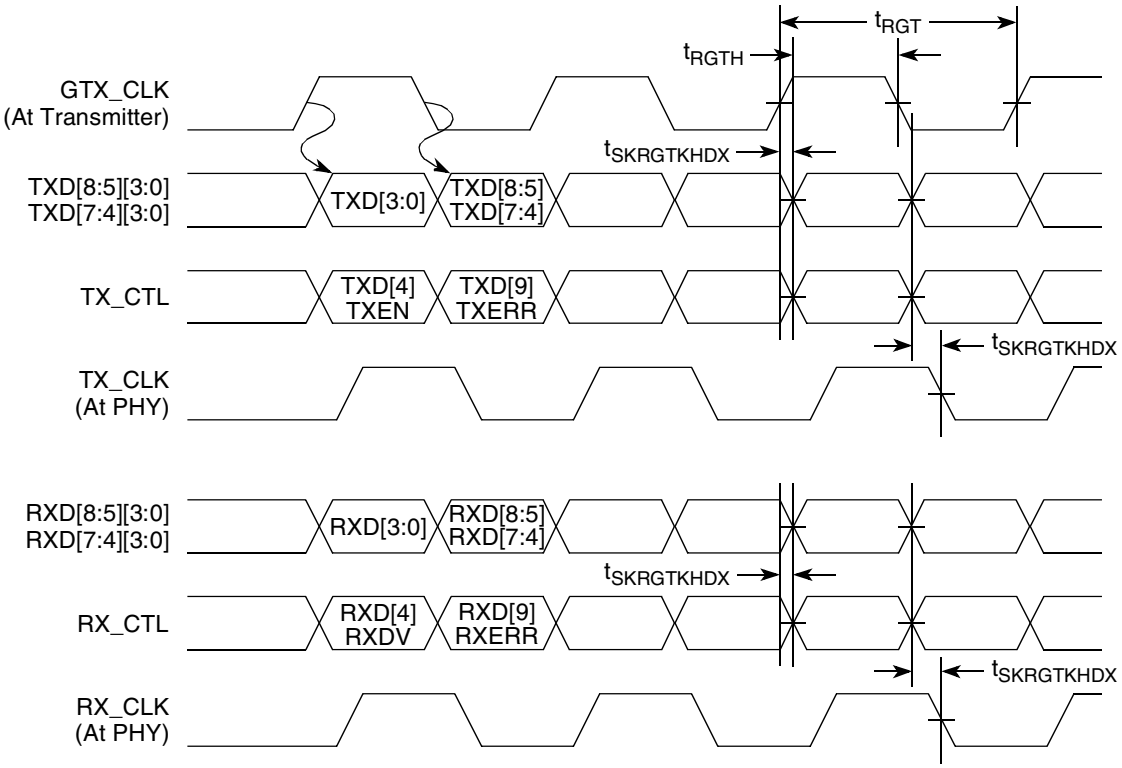


Figure 19. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in Section 8.1, "Three-Speed Ethernet Controller (10/100/1000 Mbps)— GMII/MII/RMII/TBI/RGMII/RTBI Electrical Characteristics."

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 36.

Table 36. MII Management DC Electrical Characteristics when powered at 3.3V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	—		2.97	3.63	V
Output high voltage	V_{OH}	I_{OH} = -1.0 mA	OV_{DD} = Min	2.10	OV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	OV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—		2.00	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±10	μA

8.3.2 MII Management AC Electrical Specifications

Table 37 provides the MII management AC timing specifications.

Table 37. MII Management AC Timing Specifications

At recommended operating conditions with LVDD is 3.3 V ± 10%

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	
MDC to MDIO delay	$t_{MDTKHDX}$ $t_{MDTKHDV}$	10 —	—	— 110	ns	3
MDIO to MDC setup time	$t_{MDRDVKH}$	10	—	—	ns	
MDIO to MDC hold time	$t_{MDRDXKH}$	0	—	—	ns	
MDC rise time	t_{MDCR}	—	—	10	ns	

Table 37. MII Management AC Timing Specifications (continued)

At recommended operating conditions with LVDD is 3.3 V ± 10%

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC fall time	t_{MDHF}	—	—	10	ns	

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, $t_{MDRDVKH}$ symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a csb_clk of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).
3. This parameter is dependent on the ce_clk speed (that is, for a ce_clk of 200 MHz, the delay is 90 ns and for a ce_clk of 300 MHz, the delay is 63 ns).

Figure 20 shows the MII management AC timing diagram.

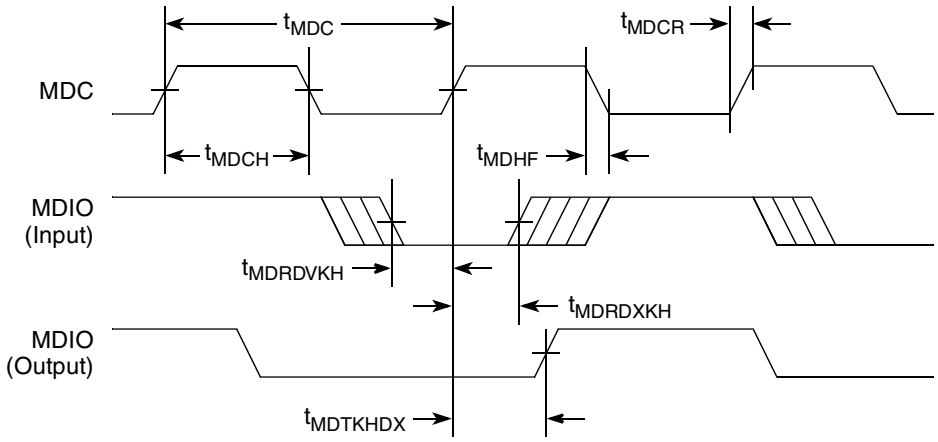


Figure 20. MII Management Interface Timing Diagram

8.3.3 IEEE Std. 1588™ Timer AC Specifications

Table 38 provides the IEEE Std. 1588 timer AC specifications.

Table 38. 1588 Timer AC Specifications

Parameter	Symbol	Min	Max	Unit	Notes
Timer clock cycle time	t_{TMRCK}	0	70	MHz	1
Input Setup to timer clock	t_{TMRCKS}	—	—	—	2,3
Input Hold from timer clock	t_{TMRCKH}	—	—	—	2,3
Output clock to output valid	t_{GCLKNV}	0	6	ns	

Table 38. 1588 Timer AC Specifications (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Timer alarm to output valid	t_{TMRAL}	—	—	—	2

Notes:
1. The timer can operate on rtc_clock or tmr_clock. These clocks get muxed and any one of them can be selected. Min and Max requirement for both rtc_clock and tmr_clock are the same.
2. These are asynchronous signals.
3. Inputs need to be stable at least one TMR clock.

9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8360E/58E.

9.1 Local Bus DC Electrical Characteristics

Table 39 provides the DC electrical characteristics for the local bus interface.

Table 39. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 µA	V_{OH}	OV_{DD} – 0.4	—	V
Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V
Input current	I_{IN}	—	±10	µA

9.2 Local Bus AC Electrical Specifications

Table 40 describes the general timing parameters of the local bus interface of the device.

Table 40. Local Bus General Timing Parameters—DLL Enabled

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	—	ns	2
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	1.7	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.9	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
LUPWAIT Input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3.0	—	ns	6

Table 40. Local Bus General Timing Parameters—DLL Enabled (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to LALE rise	t_{LBKHLR}	—	4.5	ns	
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	4.5	ns	
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	4.5	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	4.5	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	1.0	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	1.0	—	ns	3
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	3.8	ns	

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to rising edge of LSYNC_IN.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and when the load on LALE output pin is at least 10pF less than the load on LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and when the load on LALE output pin is at least 10pF less than the load on LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and when the load on LALE output pin equals to the load on LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

Table 41 describes the general timing parameters of the local bus interface of the device.

Table 41. Local Bus General Timing Parameters—DLL Bypass Mode

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to output valid	t_{LBKHOV}	—	3	ns	3

Table 41. Local Bus General Timing Parameters—DLL Bypass Mode (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	4	ns	

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $OV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and when the load on LALE output pin is at least 10pF less than the load on LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and when the load on LALE output pin is at least 10pF less than the load on LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and when the load on LALE output pin equals to the load on LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
9. DLL bypass mode is not recommended for use at frequencies above 66MHz.

Figure 21 provides the AC test load for the local bus.

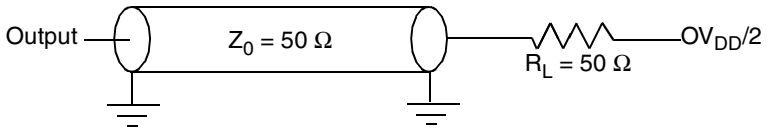


Figure 21. Local Bus C Test Load

Figure 22 through Figure 27 show the local bus signals.

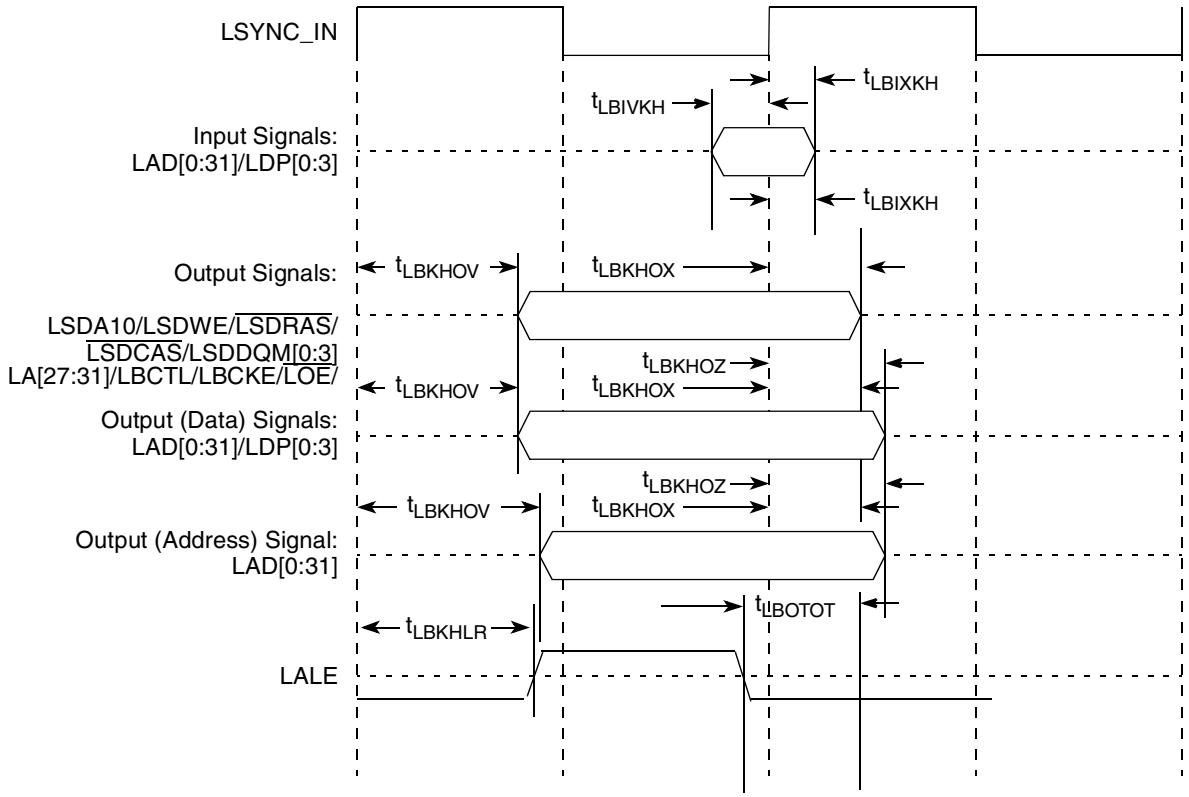


Figure 22. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)

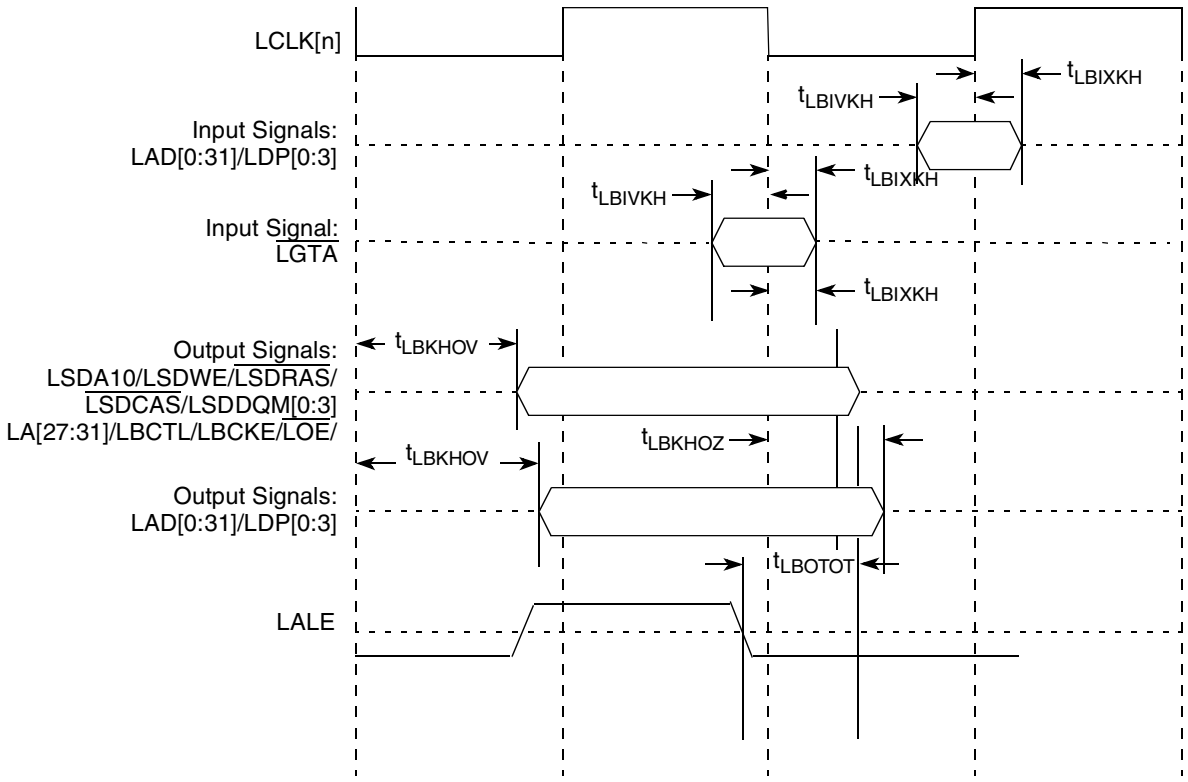


Figure 23. Local Bus Signals, Nonspecial Signals Only (DLL Bypass Mode)

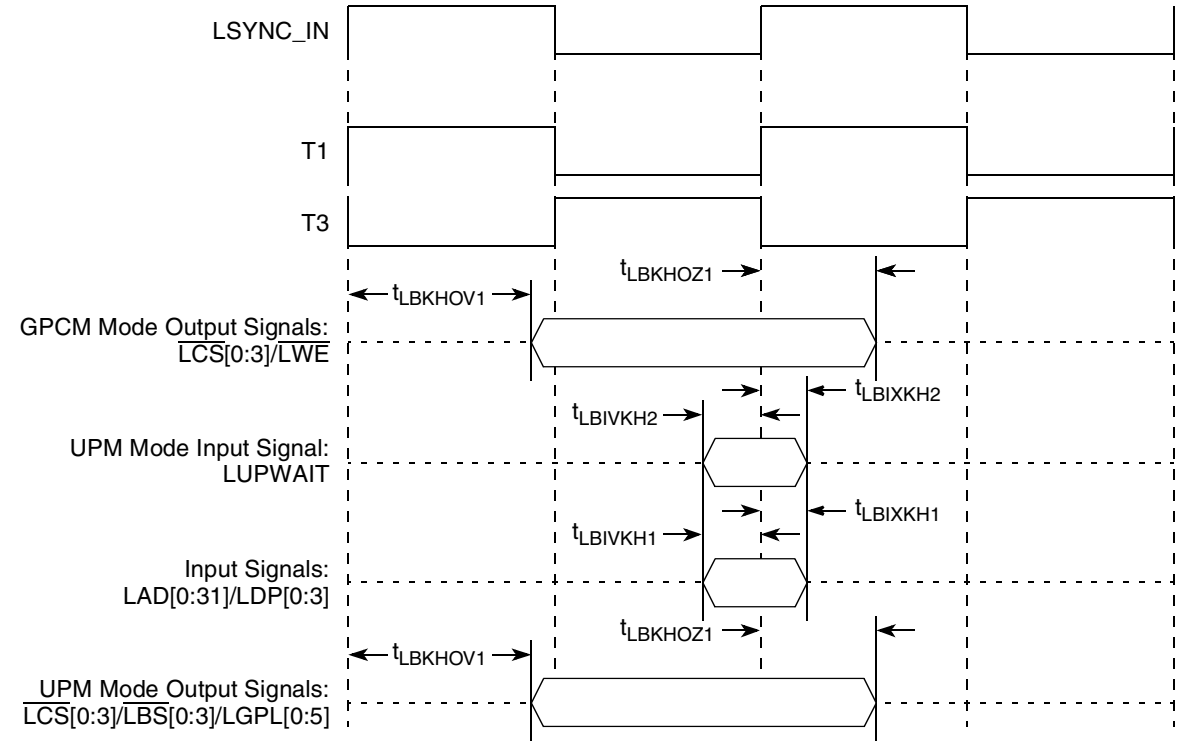


Figure 24. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)

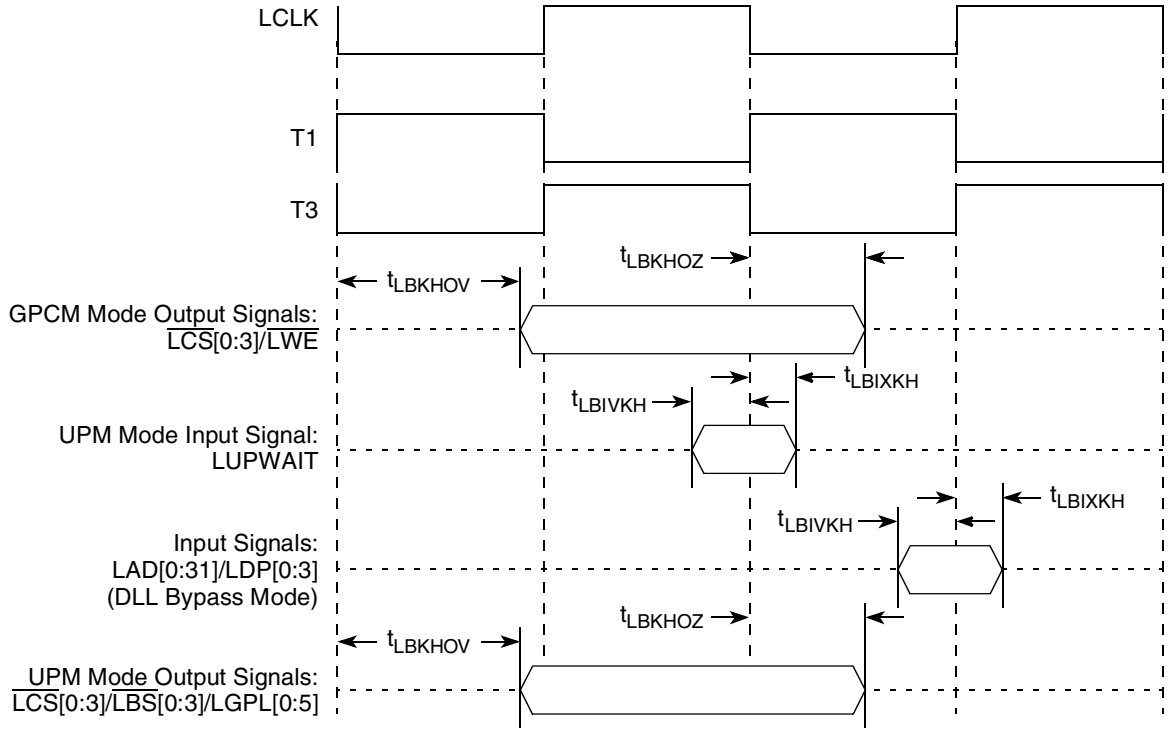


Figure 25. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)

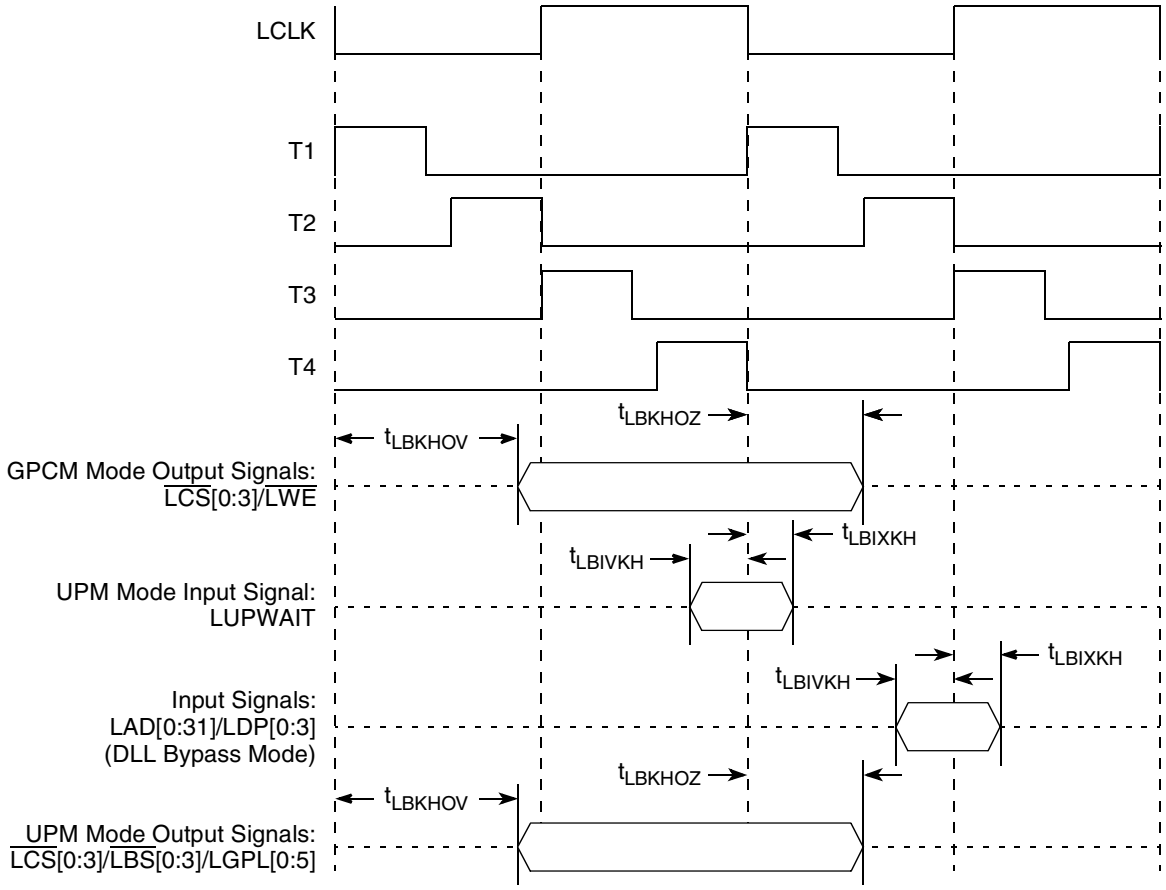


Figure 26. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Bypass Mode)

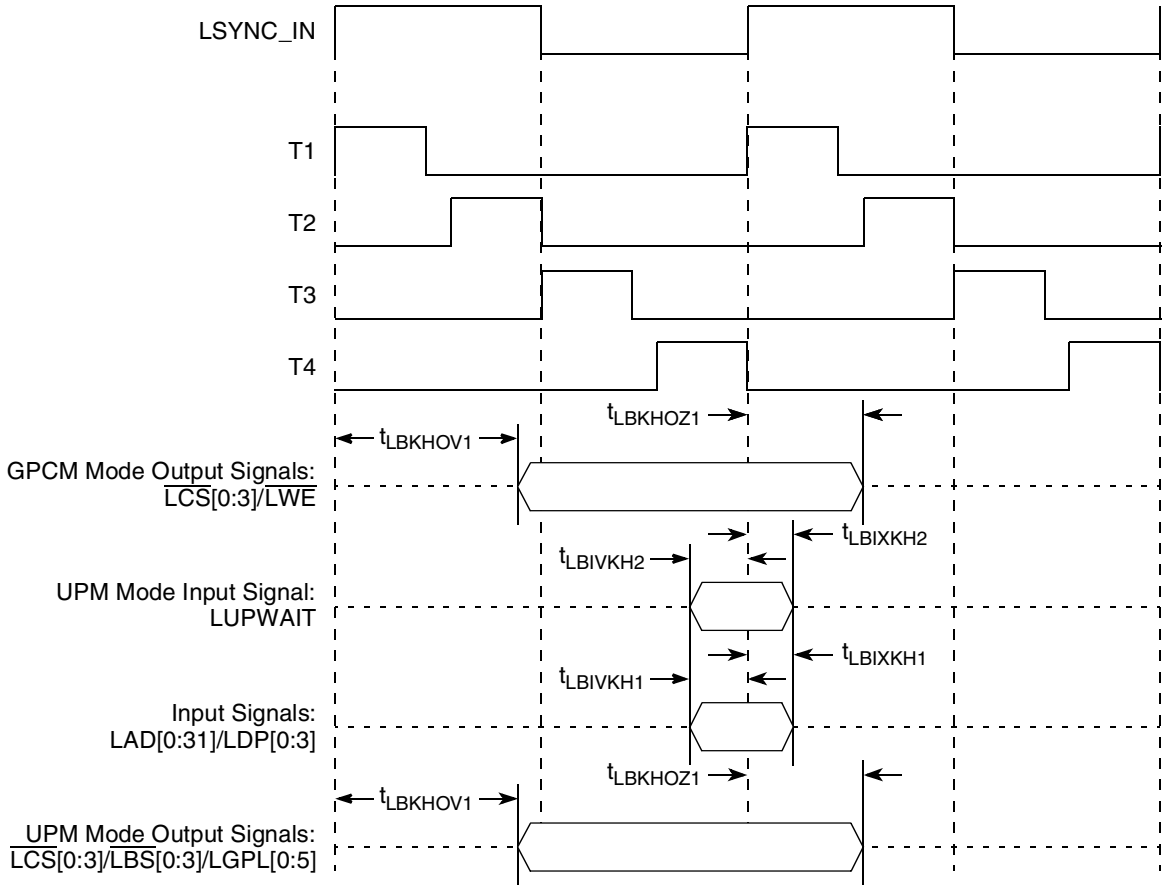


Figure 27. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Enabled)

10 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8360E/58E.

10.1 JTAG DC Electrical Characteristics

Table 42 provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the device.

Table 42. JTAG interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = -6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.5	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±10	μA

This section describes the AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the device.

Table 43 provides the JTAG AC timing specifications as defined in Figure 29 through Figure 32.

Table 43. JTAG AC Timing Specifications (Independent of CLKIN)[1]

At recommended operating conditions (see Table 2).

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	
JTAG external clock cycle time	t_{JTG}	30	—	ns	
JTAG external clock duty cycle	t_{JTKHKL}/t_{JTG}	45	55	%	
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 11 11	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 2 2	 — —	ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 2 2	 19 9	ns	 5, 6 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 21). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

Figure 28 provides the AC test load for TDO and the boundary-scan outputs of the device.

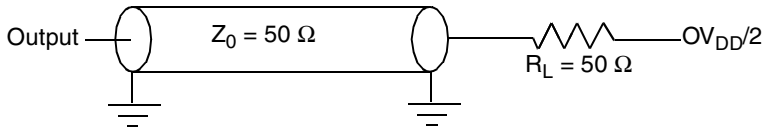


Figure 28. AC Test Load for the JTAG Interface

Figure 29 provides the JTAG clock input timing diagram.

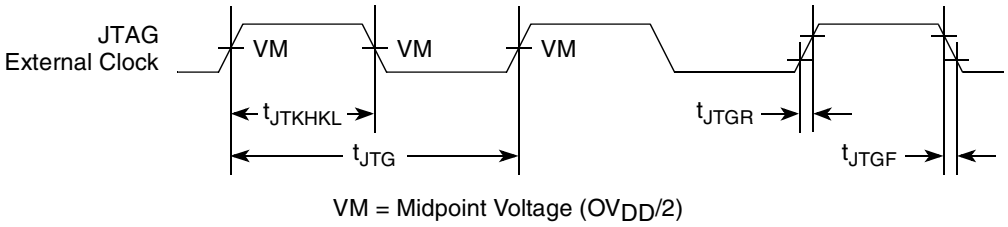


Figure 29. JTAG Clock Input Timing Diagram

Figure 30 provides the $\overline{\text{TRST}}$ timing diagram.

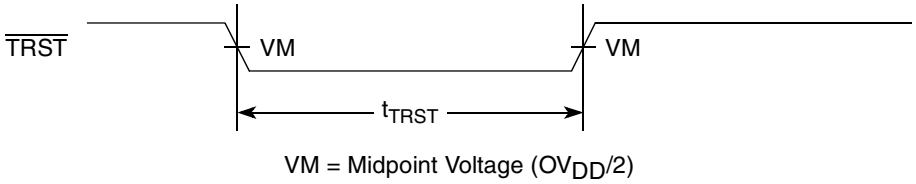


Figure 30. $\overline{\text{TRST}}$ Timing Diagram

Figure 31 provides the boundary-scan timing diagram.

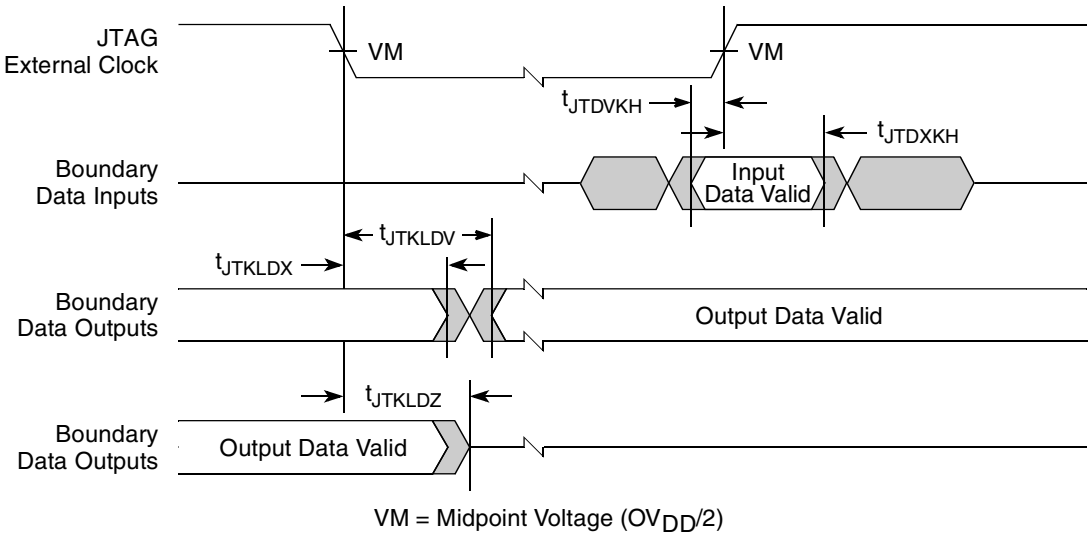


Figure 31. Boundary-Scan Timing Diagram

Figure 32 provides the test access port timing diagram.

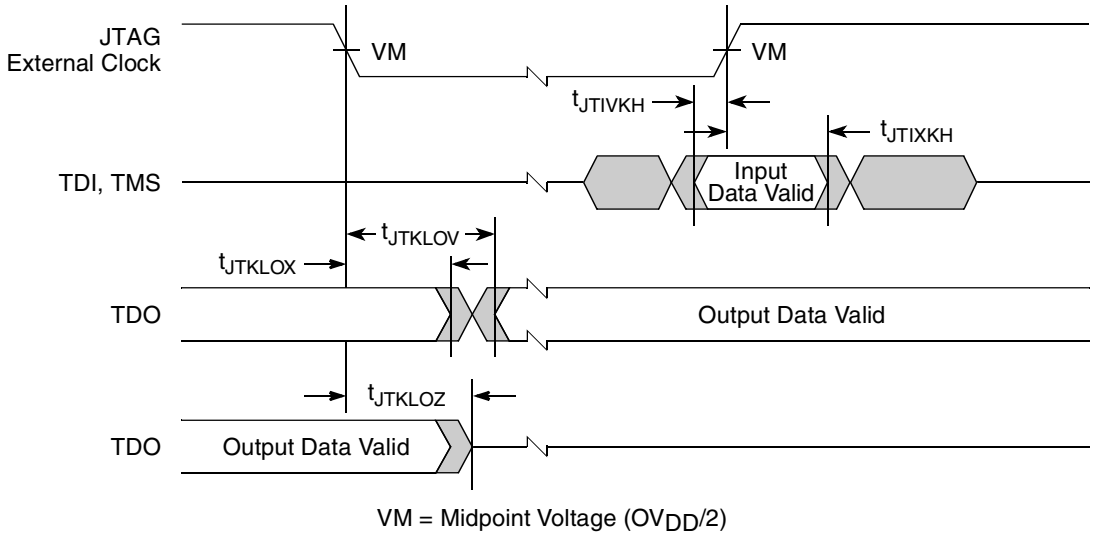


Figure 32. Test Access Port Timing Diagram

11 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8360E/58E.

11.1 I²C DC Electrical Characteristics

Table 44 provides the DC electrical characteristics for the I²C interface of the device.

Table 44. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	
Low level output voltage	V_{OL}	0	0.4	V	1
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	
Input current ($0 V \le V_{IN} \le OV_{DD}$)	I_{IN}	—	±10	μA	4

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8360E Integrated Communications Processor Reference Manual, Rev. 2* for information on the digital filter used.
4. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

11.2 I²C AC Electrical Specifications

Table 45 provides the AC timing parameters for the I²C interface of the device.

Table 45. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 44).

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	νσ
Data hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	— 0 [2]	— 0.9 [3]	μs
Rise time of both SDA and SCL signals	t_{I2CR}	20 + 0.1 C_b [4]	300	ns

Table 45. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 44).

Parameter	Symbol[1]	Min	Max	Unit
Fall time of both SDA and SCL signals	t_{I2CF}	20 + 0.1 C_b [4]	300	ns
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × OV_{DD}	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × OV_{DD}	—	V

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The device provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.

Figure 33 provides the AC test load for the I²C.

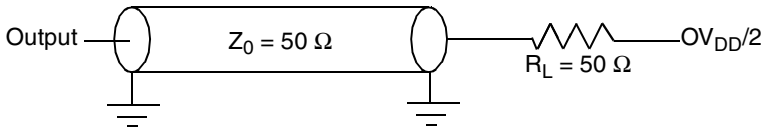


Figure 33. I²C AC Test Load

Figure 34 shows the AC timing diagram for the I²C bus.

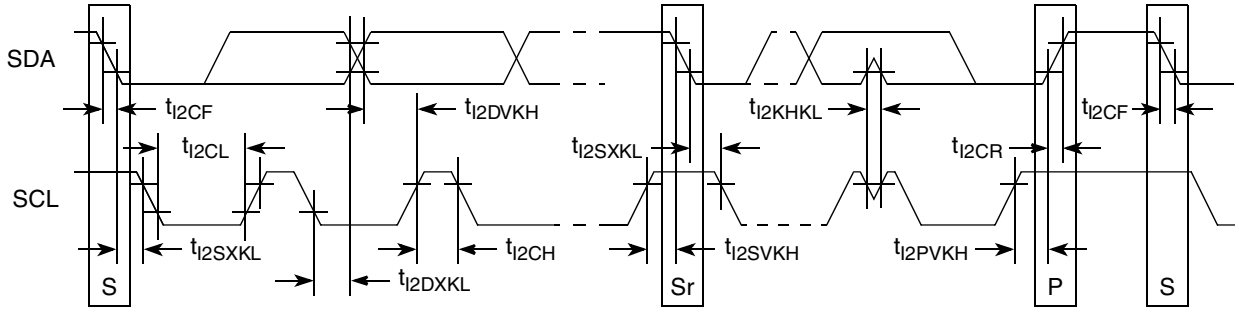


Figure 34. I²C Bus AC Timing Diagram

12 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8360E/58E.

12.1 PCI DC Electrical Characteristics

Table 46 provides the DC electrical characteristics for the PCI interface of the device.

Table 46. PCI DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	$0.5 \times OV_{DD}$	$OV_{DD} + 0.5$	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	-0.5	$0.3 \times OV_{DD}$	V
High-level output voltage	V_{OH}	$I_{OH} = -500$ µA	$0.9 \times OV_{DD}$	—	V
Low-level output voltage	V_{OL}	$I_{OL} = 1500$ µA	—	$0.1 \times OV_{DD}$	V
Input current	I_{IN}	$0 V \leq V_{IN}$[1] $\leq OV_{DD}$	—	±10	µA

Notes:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

12.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the device. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. Table 47 provides the PCI AC timing specifications at 66 MHz.

Table 47. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol [1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2, 5
Output hold from Clock	t_{PCKHOX}	1	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to Clock	t_{PCIVKH}	3.0	—	ns	2, 4

Table 47. PCI AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
Input hold from Clock	t_{PCIXKH}	0.3	—	ns	2, 4, 6

Notes:

1. Note that the symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. In rev 2.0 silicon, due to errata, t_{PCIHOV} maximum is 6.6ns. Please refer to *PCI21* in the device errata document.
6. In rev 2.0 silicon, due to errata, t_{PCIXKH} minimum is 1 ns. Please refer to *PCI17* in the device errata document.

Table 48. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol [1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from Clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to Clock	t_{PCIVKH}	7.0	—	ns	2, 4
Input hold from Clock	t_{PCIXKH}	0.3	—	ns	2, 4, 5

Notes:

1. Note that the symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. In rev 2.0 silicon, due to errata, t_{PCIXKH} minimum is 1 ns. Please refer to *PCI17* in the device errata document.

Figure 35 provides the AC test load for PCI.

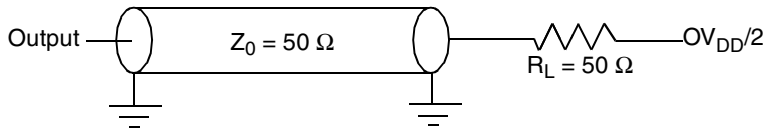


Figure 35. PCI AC Test Load

Figure 36 shows the PCI input AC timing conditions.

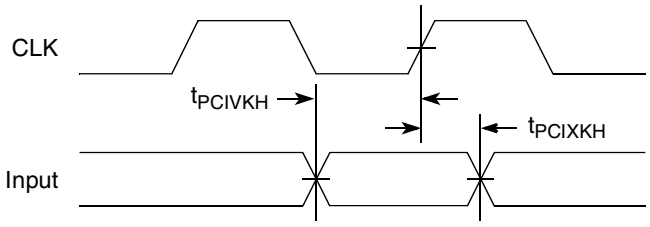


Figure 36. PCI Input AC Timing Measurement Conditions

Figure 37 shows the PCI output AC timing conditions.

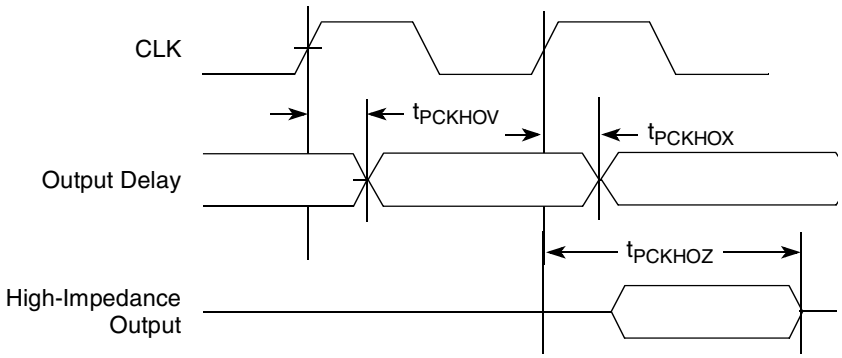


Figure 37. PCI Output AC Timing Measurement Condition

13 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8360E/58E.

13.1 Timers DC Electrical Characteristics

Table 49 provides the DC electrical characteristics for the device timer pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$ and RTC_CLK.

Table 49. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±10	μA

13.2 Timers AC Timing Specifications

Table 50 provides the timer input and output AC timing specifications.

Table 50. Timers Input AC Timing Specifications[1]

Characteristic	Symbol [2]	Typ	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

Figure 38 provides the AC test load for the timers.

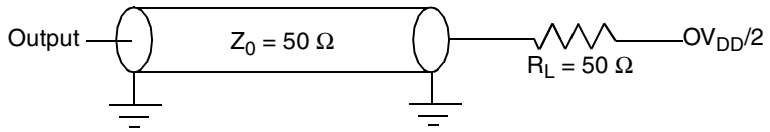


Figure 38. Timers AC Test Load

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8360E/58E.

14.1 GPIO DC Electrical Characteristics

Table 51 provides the DC electrical characteristics for the device GPIO.

Table 51. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±10	μA	

Note: This specification applies when operating from 3.3V supply.

14.2 GPIO AC Timing Specifications

Table 52 provides the GPIO input and output AC timing specifications.

Table 52. GPIO Input AC Timing Specifications[1]

Characteristic	Symbol [2]	Typ	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

Figure 39 provides the AC test load for the GPIO.

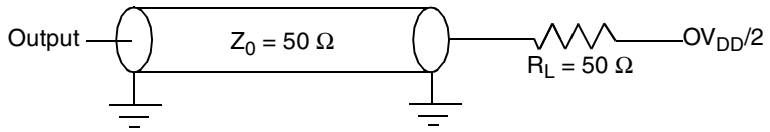


Figure 39. GPIO AC Test Load

15 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8360E/58E.

15.1 IPIC DC Electrical Characteristics

Table 53 provides the DC electrical characteristics for the external interrupt pins of the IPIC.

Table 53. IPIC DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}		2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}		–0.3	0.8	V
Input current	I_{IN}			±10	μA
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:
1. This table applies for pins $\overline{\text{IRQ}}$[0:7], $\overline{\text{IRQ\_OUT}}$, $\overline{\text{MCP\_OUT}}$, and CE ports Interrupts.
2. $\overline{\text{IRQ\_OUT}}$ and $\overline{\text{MCP\_OUT}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

15.2 IPIC AC Timing Specifications

Table 54 provides the IPIC input and output AC timing specifications.

Table 54. IPIC Input AC Timing Specifications[1]

Characteristic	Symbol [2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

16 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8360E/58E.

16.1 SPI DC Electrical Characteristics

Table 55 provides the DC electrical characteristics for the device SPI.

Table 55. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±10	μA

16.2 SPI AC Timing Specifications

Table 56 and provide the SPI input and output AC timing specifications.

Table 56. SPI AC Timing Specifications[1]

Characteristic	Symbol [2]	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	t_{NIKHOX} t_{NIKHOV}	0.3 —	— 8	ns
SPI outputs—Slave mode (external clock) delay	t_{NEKHOX} t_{NEKHOV}	2 —	— 8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	8	—	ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns

Table 56. SPI AC Timing Specifications[1]

Characteristic	Symbol [2]	Min	Max	Unit
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

Figure 40 provides the AC test load for the SPI.

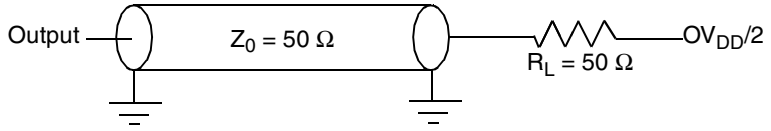
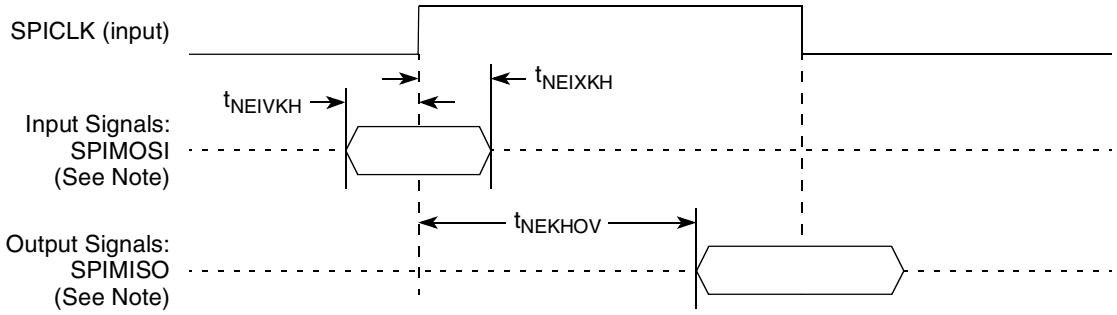


Figure 40. SPI AC Test Load

Figure 41 through Figure 42 represent the AC timing from Table 56. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

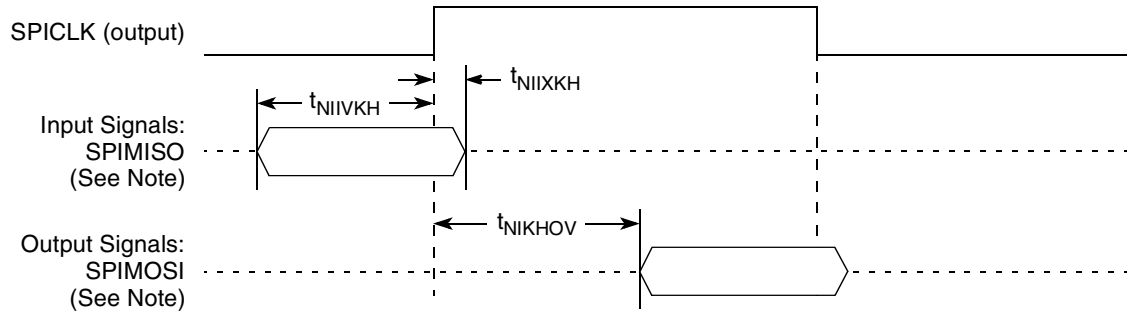
Figure 41 shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 41. SPI AC Timing in Slave mode (External Clock) Diagram

Figure 42 shows the SPI timing in Master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 42. SPI AC Timing in Master mode (Internal Clock) Diagram

17 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8360E/58E.

17.1 TDM/SI DC Electrical Characteristics

Table 57 provides the DC electrical characteristics for the device TDM/SI.

Table 57. TDM/SI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±10	μA

17.2 TDM/SI AC Timing Specifications

Table 58 provides the TDM/SI input and output AC timing specifications.

Table 58. TDM/SI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max[3]	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	10	ns
TDM/SI outputs—External clock high impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns

Table 58. TDM/SI AC Timing Specifications[1] (continued)

Characteristic	Symbol[2]	Min	Max[3]	Unit
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
3. Timings are measured from the positive or negative edge of the clock, according to SIxMR [CE] and SITXCEI[TXCEIx]. See the *MPC8360E Integrated Communications Processor Reference Manual, Rev. 2* for more details.

Figure 43 provides the AC test load for the TDM/SI.

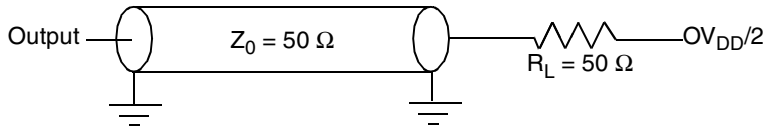
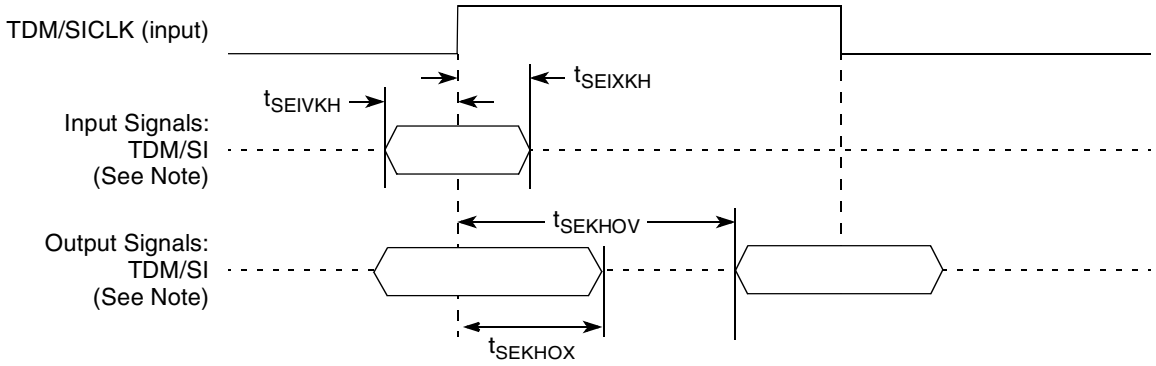


Figure 43. TDM/SI AC Test Load

Figure 44 represents the AC timing from Table 56. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 44 shows the TDM/SI timing with external clock.



Note: The clock edge is selectable on TDM/SI

Figure 44. TDM/SI AC Timing (External Clock) Diagram

18 UTOPIA/POS

This section describes the DC and AC electrical specifications for the UTOPIA/POS of the MPC8360E/58E.

18.1 UTOPIA/POS DC Electrical Characteristics

Table 59 provides the DC electrical characteristics for the device UTOPIA.

Table 59. UTOPIA DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±10	μA

18.2 Utopia/POS AC Timing Specifications

Table 60 provides the UTOPIA input and output AC timing specifications.

Table 60. UTOPIA AC Timing Specifications[1]

Characteristic	Symbol [2]	Min	Max	Unit	Notes
UTOPIA outputs—Internal clock delay	t_{UIKHOV}	0	11.5	ns	
UTOPIA outputs—External clock delay	t_{UEKHOV}	1	11.6	ns	
UTOPIA outputs—Internal clock High Impedance	t_{UIKHOX}	0	8.0	ns	
UTOPIA outputs—External clock High Impedance	t_{UEKHOX}	1	10.0	ns	
UTOPIA inputs—Internal clock input setup time	t_{UIIVKH}	6	—	ns	
UTOPIA inputs—External clock input setup time	t_{UEIVKH}	4	—	ns	3
UTOPIA inputs—Internal clock input Hold time	t_{UIIXKH}	2.4	—	ns	
UTOPIA inputs—External clock input hold time	t_{UEIXKH}	1	—	ns	3

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{UIKHOX} symbolizes the UTOPIA outputs internal timing (UI) for the time t_{UTOPIA} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
3. In rev 2.0 silicon, due to errata, t_{UEIVKH} minimum is 4.3 ns and t_{UEIXKH} minimum is 1.4 ns under specific conditions. Please refer to *QE_UPC3* in the device errata document.

Figure 45 provides the AC test load for the UTOPIA.

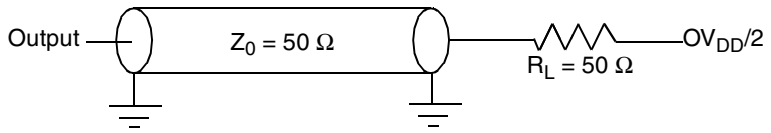


Figure 45. UTOPIA AC Test Load

Figure 46 and Figure 47 represent the AC timing from Table 56. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 46 shows the UTOPIA timing with external clock.

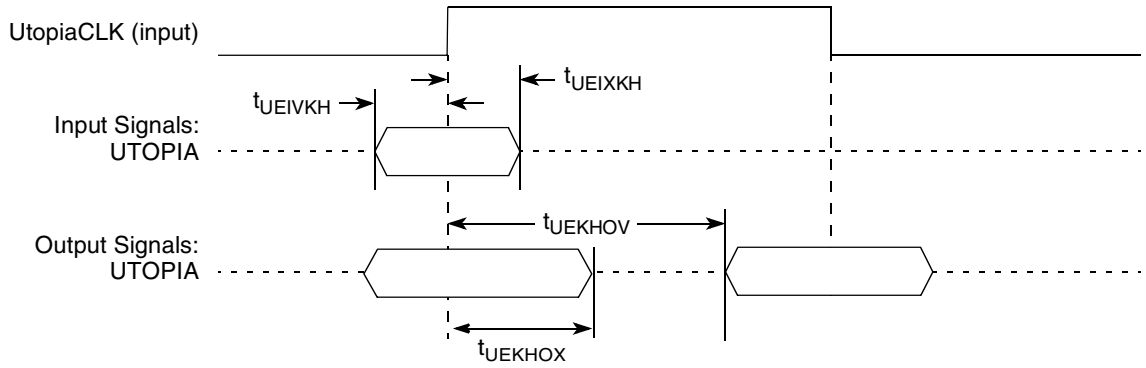


Figure 46. UTOPIA AC Timing (External Clock) Diagram

Figure 47 shows the UTOPIA timing with internal clock.

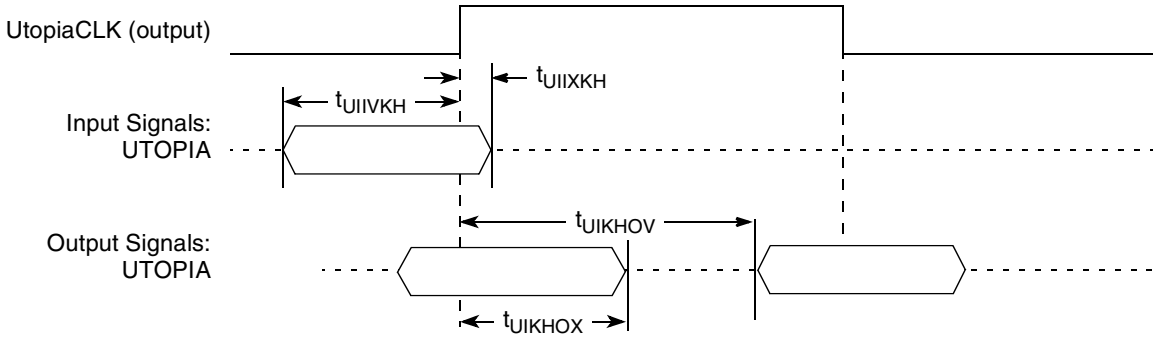


Figure 47. UTOPIA AC Timing (Internal Clock) Diagram

19 HDLC, BISYNC, Transparent, and Synchronous UART

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), BiSync, transparent, and synchronous UART protocols of the MPC8360E/58E.

19.1 HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

Table 61 provides the DC electrical characteristics for the device HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 61. HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±10	μA

19.2 HDLC, BISYNC, Transparent, and Synchronous UART AC Timing Specifications

Table 62 and Table 63 provide the input and output AC timing specifications for HDLC, BiSync, transparent, and synchronous UART protocols.

Table 62. HDLC, BISYNC, and Transparent AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—Internal clock delay	t_{HIKHOV}	0	11.2	ns
Outputs—External clock delay	t_{HEKHOV}	1	10.8	ns
Outputs—Internal clock High Impedance	t_{HIKHOX}	-0.5	5.5	ns
Outputs—External clock High Impedance	t_{HEKHOX}	1	8	ns
Inputs—Internal clock input setup time	t_{HIIVKH}	8.5	—	ns
Inputs—External clock input setup time	t_{HEIVKH}	4	—	ns
Inputs—Internal clock input Hold time	t_{HIIXKH}	1.4	—	ns
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Table 63. Synchronous UART AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—Internal clock delay	$t_{UAIKHOV}$	0	11.3	ns
Outputs—External clock delay	$t_{UAEKHOV}$	1	14	ns
Outputs—Internal clock High Impedance	$t_{UAIKHOX}$	0	11	ns
Outputs—External clock High Impedance	$t_{UAEKHOX}$	1	14	ns
Inputs—Internal clock input setup time	$t_{UAIIVKH}$	6	—	ns
Inputs—External clock input setup time	$t_{UAEIVKH}$	8	—	ns
Inputs—Internal clock input Hold time	$t_{UAIIXKH}$	1	—	ns
Inputs—External clock input hold time	$t_{UAEIXKH}$	1	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 48 provides the AC test load.

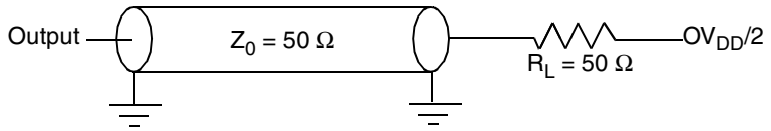
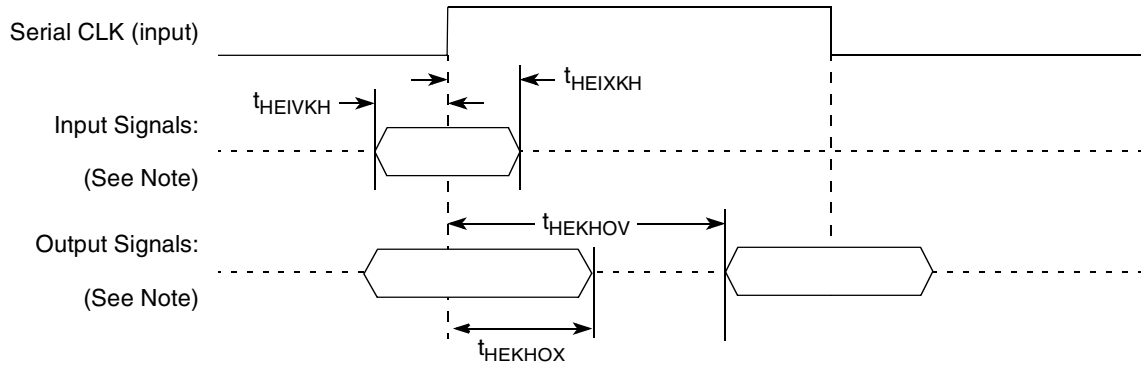


Figure 48. AC Test Load

19.3 AC Test Load

Figure 49 and Figure 50 represent the AC timing from Table 62 and Table 63. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

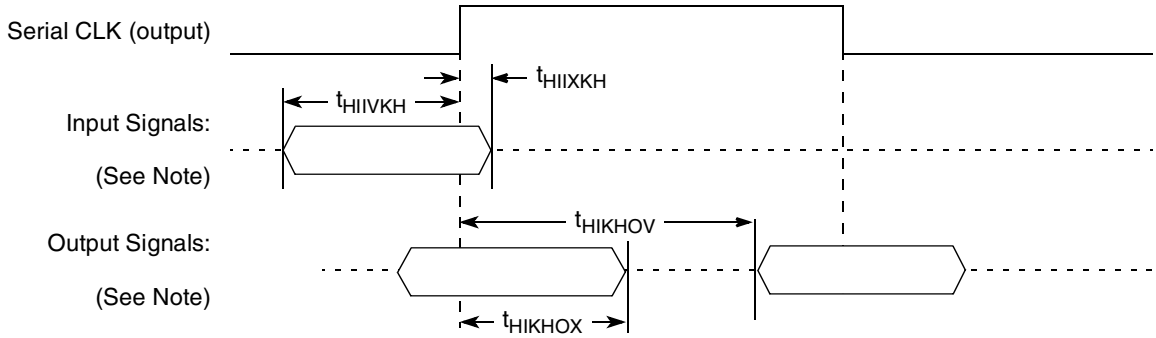
Figure 49 shows the timing with external clock.



Note: The clock edge is selectable.

Figure 49. AC Timing (External Clock) Diagram

Figure 50 shows the timing with internal clock.



Note: The clock edge is selectable.

Figure 50. AC Timing (Internal Clock) Diagram

20 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8360E/58E.

20.1 USB DC Electrical Characteristics

Table 64 provides the DC electrical characteristics for the USB interface.

Table 64. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 µA	V_{OH}	OV_{DD} – 0.4	—	V
Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V
Input current	I_{IN}	—	±10	µA

Note:

1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

20.2 USB AC Electrical Specifications

Table 65 describes the general timing parameters of the USB interface of the device.

Table 65. USB General Timing Parameters

Parameter	Symbol [1]	Min	Max	Unit	Notes
usb clock cycle time	t_{USCK}	20.83	—	ns	full speed 48MHz
usb clock cycle time	t_{USCK}	166.67	—	ns	low speed 6MHz
skew between TXP and TXN	t_{USTSPN}	—	5	ns	
skew among RXP, RXN and RXD	$t_{USRSPND}$	—	10	ns	full speed transitions
skew among RXP, RXN and RXD	t_{USRPND}	—	100	ns	low speed transitions

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(state)(signal)}}$ for receive signals and $t_{\text{(First two letters of functional block)(state)(signal)}}$ for transmit signals. For example, $t_{USRSPND}$ symbolizes usb timing (US) for the usb receive signals skew (RS) among RXP, RXN, and RXD (PND). Also, t_{USTSPN} symbolizes usb timing (US) for the usb transmit signals skew (TS) between TXP and TXN (PN).

2.Skew measurements are done at $OV_{DD}/2$ of the rising or falling edge of the signals.

Figure 51 provide the AC test load for the USB.

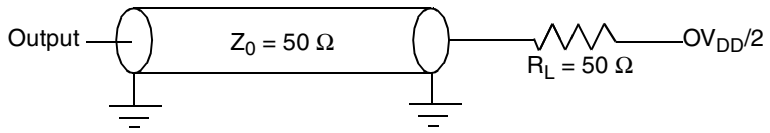


Figure 51. USB AC Test Load

21 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8360E/58E is available in a tape ball grid array (TBGA), see Section 21.1, "Package Parameters for the TBGA Package and Section 21.2, "Mechanical Dimensions of the TBGA Package," for information on the package.

21.1 Package Parameters for the TBGA Package

The package parameters for rev 2.0 silicon are as provided in the following list. The package type is **37.5** mm × **37.5** mm, **740** tape ball grid array (TBGA).

Package outline	**37.5 mm × 37.5 mm**
Interconnects	**740**
Pitch	**1.00 mm**
Module height (typical)	1.46 mm
Solder Balls	62 Sn/36 Pb/2 Ag (ZU package)
	95.5 Sn/0.5 Cu/4Ag (VV package)
Ball diameter (typical)	0.64 mm

21.2 Mechanical Dimensions of the TBGA Package

Figure 52 depicts the mechanical dimensions and bottom surface nomenclature of the device, 740-TBGA package.

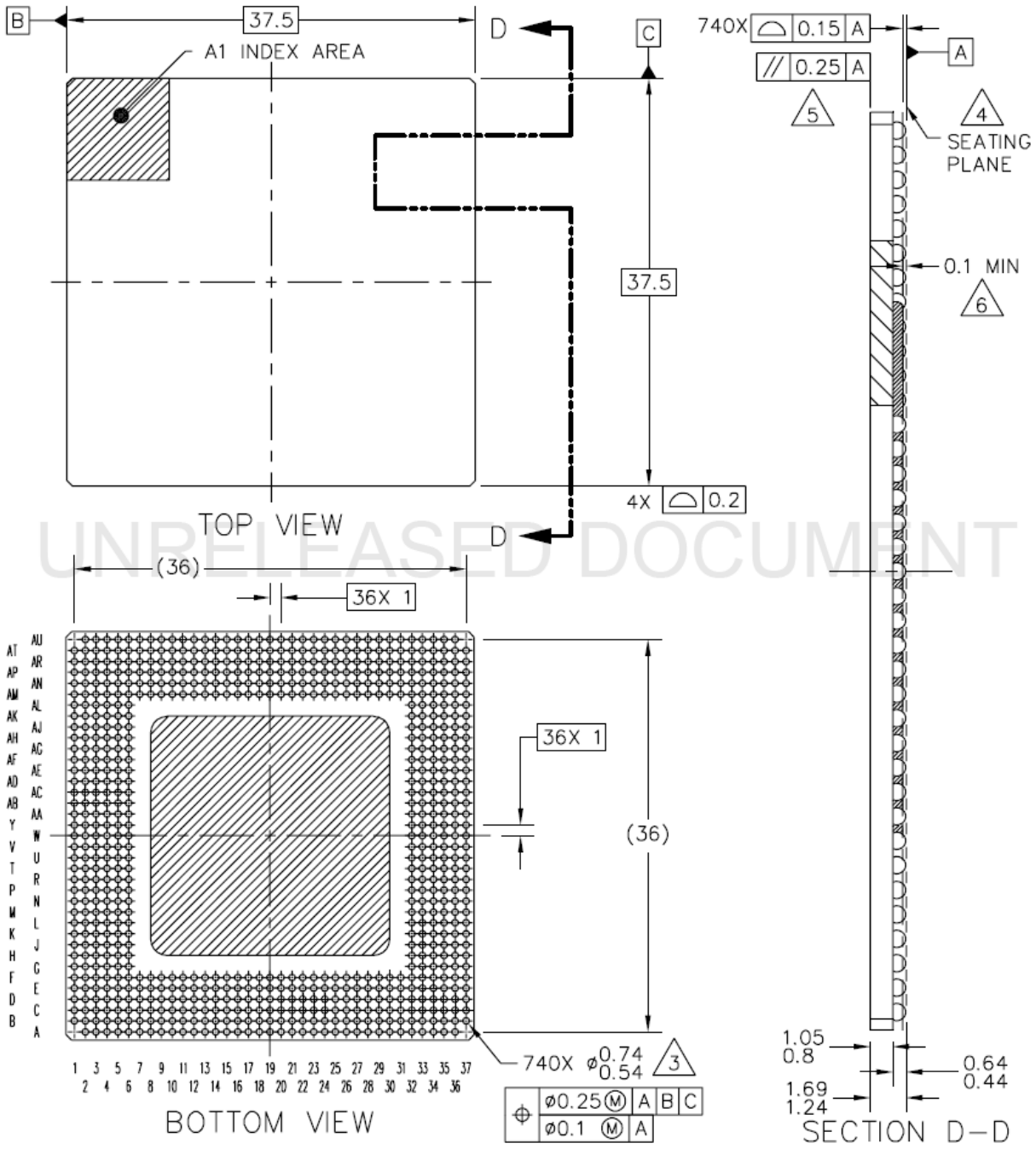


Figure 52. Mechanical Dimensions and Bottom Surface Nomenclature of the TBGA Package

21.3 Pinout Listings

Table 66 shows the pin list of the MPC8360E TBGA package.

Table 66. MPC8360E TBGA Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Primary DDR SDRAM Memory Controller Interface				
MEMC1_MDQ[0:31]	AJ34, AK33, AL33, AL35, AJ33, AK34, AK32, AM36, AN37, AN35, AR34, AT34, AP37, AP36, AR36, AT35, AP34, AR32, AP32, AM31, AN33, AM34, AM33, AM30, AP31, AM27, AR30, AT32, AN29, AP29, AN27, AR29	I/O	GV_{DD}	
MEMC1_MDQ[32:63]/ MEMC2_MDQ[0:31]	AN8, AN7, AM8, AM6, AP9, AN9, AT7, AP7, AU6, AP6, AR4, AR3, AT6, AT5, AR5, AT3, AP4, AM5, AP3, AN3, AN5, AL5, AN4, AM2, AL2, AH5, AK3, AJ2, AJ3, AH4, AK4, AH3	I/O	GV_{DD}	
MEMC1_MECC[0:4]/ MSRCID[0:4]	AP24, AN22, AM19, AN19, AM24	I/O	GV_{DD}	
MEMC1_MECC[5]/ MDVAL	AM23	I/O	GV_{DD}	
MEMC1_MECC[6:7]	AM22, AN18	I/O	GV_{DD}	
MEMC1_MDM[0:3]	AL36, AN34, AP33, AN28	O	GV_{DD}	
MEMC1_MDM[4:7]/ MEMC2_MDM[0:3]	AT9, AU4, AM3, AJ6	O	GV_{DD}	
MEMC1_MDM[8]	AP27	O	GV_{DD}	
MEMC1_MDQS[0:3]	AK35, AP35, AN31, AM26	I/O	GV_{DD}	
MEMC1_MDQS[4:7]/ MEMC2_MDQS[0:3]	AT8, AU3, AL4, AJ5	I/O	GV_{DD}	
MEMC1_MDQS[8]	AP26	I/O	GV_{DD}	
MEMC1_MBA[0:1]	AU29, AU30	O	GV_{DD}	
MEMC1_MBA[2]	AT30	O	GV_{DD}	
MEMC1_MA[0:14]	AU21, AP22, AP21, AT21, AU25, AU26, AT23, AR26, AU24, AR23, AR28, AU23, AR22, AU20, AR18	O	GV_{DD}	
MEMC1_MODT[0:1]	AG33, AJ36	O	GV_{DD}	6
MEMC1_MODT[2:3]/ MEMC2_MODT[0:1]	AT1, AK2	O	GV_{DD}	6
$\overline{\text{MEMC1\_MWE}}$	AT26	O	GV_{DD}	
$\overline{\text{MEMC1\_MRAS}}$	AT29	O	GV_{DD}	
$\overline{\text{MEMC1\_MCAS}}$	AT24	O	GV_{DD}	
$\overline{\text{MEMC1\_MCS}}$[0:1]	AU27, AT27	O	GV_{DD}	
$\overline{\text{MEMC1\_MCS}}$[2:3]/ $\overline{\text{MEMC2\_MCS}}$[0:1]	AU8, AU7	O	GV_{DD}	
MEMC1_MCKE[0:1]	AL32, AU33	O	GV_{DD}	3
MEMC1_MCK[0:1]	AK37, AT37	O	GV_{DD}	
MEMC1_MCK[2:3]/ MEMC2_MCK[0:1]	AN1, AR2	O	GV_{DD}	

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC1_MCK[4:5]/ MEMC2_MCKE[0:1]	AN25, AK1	O	GV_{DD}	
$\overline{\text{MEMC1\_MCK}}$[0:1]	AL37, AT36	O	GV_{DD}	
$\overline{\text{MEMC1\_MCK}}$[2:3]/ $\overline{\text{MEMC2\_MCK}}$[0:1]	AP2, AT2	O	GV_{DD}	
$\overline{\text{MEMC1\_MCK}}$[4]/ MEMC2_MDM[8]	AN24	O	GV_{DD}	
$\overline{\text{MEMC1\_MCK}}$[5]/ MEMC2_MDQS[8]	AL1	O	GV_{DD}	
MDIC[0:1]	AH6, AP30	I/O	GV_{DD}	10
Secondary DDR SDRAM Memory Controller Interface				
MEMC2_MECC[0:7]	AN16, AP18, AM16, AM17, AN17, AP13, AP15, AN13	I/O	GV_{DD}	
MEMC2_MBA[0:2]	AU12, AU15, AU13	O	GV_{DD}	
MEMC2_MA[0:14]	AT12, AP11, AT13, AT14, AR13, AR15, AR16, AT16, AT18, AT17, AP10, AR20, AR17, AR14, AR11	O	GV_{DD}	
$\overline{\text{MEMC2\_MWE}}$	AU10	O	GV_{DD}	
$\overline{\text{MEMC2\_MRAS}}$	AT11	O	GV_{DD}	
$\overline{\text{MEMC2\_MCAS}}$	AU11	O	GV_{DD}	
PCI				
$\overline{\text{PCI\_INTA}}$/ $\overline{\text{IRQ\_OUT}}$/ CE_PF[5]	A20	I/O	LV_{DD}2	2
$\overline{\text{PCI\_RESET\_OUT}}$/ CE_PF[6]	E19	I/O	LV_{DD}2	
PCI_AD[31:30]/ CE_PG[31:30]	D20, D21	I/O	LV_{DD}2	
PCI_AD[29:25]/ CE_PG[29:25]	A24, B23, C23, E23, A26	I/O	OV_{DD}	
PCI_AD[24]/ CE_PG[24]	B21	I/O	LV_{DD}2	
PCI_AD[23:0]/ CE_PG[23:0]	C24, C25, D25, B25, E24, F24, A27, A28, F27, A30, C30, D30, E29, B31, C31, D31, D32, A32, C33, B33, F30, E31, A34, D33	I/O	OV_{DD}	
PCI_C/ $\overline{\text{BE}}$[3:0]/ CE_PF[10:7]	E22, B26, E28, F28	I/O	OV_{DD}	
PCI_PAR/ CE_PF[11]	D28	I/O	OV_{DD}	
$\overline{\text{PCI\_FRAME}}$/ CE_PF[12]	D26	I/O	OV_{DD}	5
$\overline{\text{PCI\_TRDY}}$/ CE_PF[13]	C27	I/O	OV_{DD}	5

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_IRDY/ CE_PF[14]	C28	I/O	OV_{DD}	5
PCI_STOP/ CE_PF[15]	B28	I/O	OV_{DD}	5
PCI_DEVSEL/ CE_PF[16]	E26	I/O	OV_{DD}	5
PCI_IDSEL/ CE_PF[17]	F22	I/O	OV_{DD}	
PCI_SERR/ CE_PF[18]	B29	I/O	OV_{DD}	5
PCI_PERR/ CE_PF[19]	A29	I/O	OV_{DD}	5
PCI_REQ[0]/ CE_PF[20]	F19	I/O	LV_{DD}2	
PCI_REQ[1]/ CPCI_HS_ES/ CE_PF[21]	A21	I/O	LV_{DD}2	
PCI_REQ[2]/ CE_PF[22]	C21	I/O	LV_{DD}2	
PCI_GNT[0]/ CE_PF[23]	E20	I/O	LV_{DD}2	
PCI_GNT[1]/ CPCI1_HS_LED/ CE_PF[24]	B20	I/O	LV_{DD}2	
PCI_GNT[2]/ CPCI1_HS_ENUM/ CE_PF[25]	C20	I/O	LV_{DD}2	
PCI_MODE	D36	I	OV_{DD}	
M66EN/ CE_PF[4]	B37	I/O	OV_{DD}	
Local Bus Controller Interface				
LAD[0:31]	N32, N33, N35, N36, P37, P32, P34, R36, R35, R34, R33, T37, T35, T34, T33, U37, T32, U36, U34, V36, V35, W37, W35, V33, V32, W34, Y36, W32, AA37, Y33, AA35, AA34	I/O	OV_{DD}	
LDP[0]/ CKSTOP_OUT	AB37	I/O	OV_{DD}	
LDP[1]/ CKSTOP_IN	AB36	I/O	OV_{DD}	
LDP[2]/ LCS[6]	AB35	I/O	OV_{DD}	
LDP[3]/ LCS[7]	AA33	I/O	OV_{DD}	
LA[27:31]	AC37, AA32, AC36, AC34, AD36	O	OV_{DD}	
LCS[0:5]	AD33, AG37, AF34, AE33, AD32, AH37	O	OV_{DD}	

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{LWE}}$[0:3]/ LSDDQM[0:3]/ $\overline{\text{LBS}}$[0:3]	AG35, AG34, AH36, AE32	O	OV_{DD}	
LBCTL	AD35	O	OV_{DD}	
LALE	M37	O	OV_{DD}	
LGPL0/ LSDA10/ cfg_reset_source0	AB32	I/O	OV_{DD}	
LGPL1/ $\overline{\text{LSDWE}}$/ cfg_reset_source1	AE37	I/O	OV_{DD}	
LGPL2/ $\overline{\text{LSDRAS}}$/ $\overline{\text{LOE}}$	AC33	O	OV_{DD}	
LGPL3/ $\overline{\text{LSDCAS}}$/ cfg_reset_source2	AD34	I/O	OV_{DD}	
LGPL4/ $\overline{\text{LGTA}}$/ LUPWAIT/ LPBSE	AE35	I/O	OV_{DD}	
LGPL5/ cfg_clkin_div	AF36	I/O	OV_{DD}	
LCKE	G36	O	OV_{DD}	
LCLK[0]	J33	O	OV_{DD}	
LCLK[1]/ LCS[6]	J34	O	OV_{DD}	
LCLK[2]/ LCS[7]	G37	O	OV_{DD}	
LSYNC_OUT	F34	O	OV_{DD}	
LSYNC_IN	G35	I	OV_{DD}	
Programmable Interrupt Controller				
$\overline{\text{MCP\_OUT}}$	E34	O	OV_{DD}	2
$\overline{\text{IRQ}}$0/ $\overline{\text{MCP_IN}}$	C37	I	OV_{DD}	
$\overline{\text{IRQ}}$[1]/ M1SRCID[4]/ M2SRCID[4]/ LSRCID[4]	F35	I/O	OV_{DD}	
$\overline{\text{IRQ}}$[2]/ M1DVAL/ M2DVAL/ LDVAL	F36	I/O	OV_{DD}	
$\overline{\text{IRQ}}$[3]/ CORE_SRESET	H34	I/O	OV_{DD}	

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{IRQ}}$[4:5]	G33, G32	I/O	OV_{DD}	
$\overline{\text{IRQ}}$[6]/ $\overline{\text{LCS}}$[6]/ $\overline{\text{CKSTOP\_OUT}}$	E35	I/O	OV_{DD}	
$\overline{\text{IRQ}}$[7]/ $\overline{\text{LCS}}$[7]/ $\overline{\text{CKSTOP\_IN}}$	H36	I/O	OV_{DD}	
DUART				
UART1_SOUT/ M1SRCID[0]/ M2SRCID[0]/ LSRCID[0]	E32	O	OV_{DD}	
UART1_SIN/ M1SRCID[1]/ M2SRCID[1]/ LSRCID[1]	B34	I/O	OV_{DD}	
$\overline{\text{UART1\_CTS}}$/ M1SRCID[2]/ M2SRCID[2]/ LSRCID[2]	C34	I/O	OV_{DD}	
$\overline{\text{UART1\_RTS}}$ M1SRCID[3]/ M2SRCID[3]/ LSRCID[3]	A35	O	OV_{DD}	
I^2C Interface				
IIC1_SDA	D34	I/O	OV_{DD}	2
IIC1_SCL	B35	I/O	OV_{DD}	2
IIC2_SDA	E33	I/O	OV_{DD}	2
IIC2_SCL	C35	I/O	OV_{DD}	2
QUICC™ Engine				
CE_PA[0]	F8	I/O	LV_{DD0}	
CE_PA[1:2]	AH1, AG5	I/O	OV_{DD}	
CE_PA[3:7]	F6, D4, C3, E5, A3	I/O	$LV_{DD}0$	
CE_PA[8]	AG3	I/O	OV_{DD}	
CE_PA[9:12]	F7, B3, E6, B4	I/O	$LV_{DD}0$	
CE_PA[13:14]	AG1, AF6	I/O	OV_{DD}	
CE_PA[15]	B2	I/O	$LV_{DD}0$	
CE_PA[16]	AF4	I/O	OV_{DD}	
CE_PA[17:21]	B16, A16, E17, A17, B17	I/O	$LV_{DD}1$	
CE_PA[22]	AF3	I/O	OV_{DD}	
CE_PA[23:26]	C18, D18, E18, A18	I/O	$LV_{DD}1$	
CE_PA[27:28]	AF2, AE6	I/O	OV_{DD}	

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
CE_PA[29]	B19	I/O	$LV_{DD}1$	
CE_PA[30]	AE5	I/O	OV_{DD}	
CE_PA[31]	F16	I/O	$LV_{DD}1$	
CE_PB[0:27]	AE2, AE1, AD5, AD3, AD2, AC6, AC5, AC4, AC2, AC1, AB5, AB4, AB3, AB1, AA6, AA4, AA2, Y6, Y4, Y3, Y2, Y1, W6, W5, W2, V5, V3, V2	I/O	OV_{DD}	
CE_PC[0:1]	V1, U6	I/O	OV_{DD}	
CE_PC[2:3]	C16, A15	I/O	$LV_{DD}1$	
CE_PC[4:6]	U4, U3, T6	I/O	OV_{DD}	
CE_PC[7]	C19	I/O	$LV_{DD}2$	
CE_PC[8:9]	A4, C5	I/O	$LV_{DD}0$	
CE_PC[10:30]	T5, T4, T2, T1, R5, R3, R1, C11, D12, F13, B10, C10, E12, A9, B8, D10, A14, E15, B14, D15, AH2	I/O	OV_{DD}	
CE_PD[0:27]	E11, D9, C8, F11, A7, E9, C7, A6, F10, B6, D7, E8, B5, A5, C2, E4, F5, B1, D2, G5, D1, E2, H6, F3, E1, F2, G3, H4	I/O	OV_{DD}	
CE_PE[0:31]	K3, J2, F1, G2, J5, H3, G1, H2, K6, J3, K5, K4, L6, P6, P4, P3, P1, N4, N5, N2, N1, M2, M3, M5, M6, L1, L2, L4, E14, C13, C14, B13	I/O	OV_{DD}	
CE_PF[0:3]	F14, D13, A12, A11	I/O	OV_{DD}	
Clocks				
PCI_CLK_OUT[0]/ CE_PF[26]	B22	I/O	$LV_{DD}2$	
PCI_CLK_OUT[1:2]/ CE_PF[27:28]	D22, A23	I/O	OV_{DD}	
CLKIN	E37	I	OV_{DD}	
PCI_CLOCK/ PCI_SYNC_IN	M36	I	OV_{DD}	
PCI_SYNC_OUT/ CE_PF[29]	D37	I/O	OV_{DD}	3
JTAG				
TCK	K33	I	OV_{DD}	
TDI	K34	I	OV_{DD}	4
TDO	H37	O	OV_{DD}	3
TMS	J36	I	OV_{DD}	4
$\overline{\text{TRST}}$	L32	I	OV_{DD}	4
Test				
TEST	L35	I	OV_{DD}	7
TEST_SEL	AU34	I	GV_{DD}	7
PMC				
$\overline{\text{QUIESCE}}$	B36	O	OV_{DD}	

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
System Control				
$\overline{\text{PORESET}}$	L37	I	OV_{DD}	
$\overline{\text{HRESET}}$	L36	I/O	OV_{DD}	1
$\overline{\text{SRESET}}$	M33	I/O	OV_{DD}	2
Thermal Management				
THERM0	AP19	I	GV_{DD}	
THERM1	AT31	I	GV_{DD}	
Power and Ground Signals				
$AV_{DD}1$	K35	Power for LBIU DLL (1.2 V)	$AV_{DD}1$	
$AV_{DD}2$	K36	Power for CE PLL (1.2 V)	$AV_{DD}2$	
$AV_{DD}5$	AM29	Power for e300 PLL (1.2 V)	$AV_{DD}5$	
$AV_{DD}6$	K37	Power for system PLL (1.2 V)	$AV_{DD}6$	
GND	A2, A8, A13, A19, A22, A25, A31, A33, A36, B7, B12, B24, B27, B30, C4, C6, C9, C15, C26, C32, D3, D8, D11, D14, D17, D19, D23, D27, E7, E13, E25, E30, E36, F4, F37, G34, H1, H5, H32, H33, J4, J32, J37, K1, L3, L5, L33, L34, M1, M34, M35, N37, P2, P5, P35, P36, R4, T3, U1, U5, U35, V37, W1, W4, W33, W36, Y34, AA3, AA5, AC3, AC32, AC35, AD1, AD37, AE4, AE34, AE36, AF33, AG4, AG6, AG32, AH35, AJ1, AJ4, AJ32, AJ35, AJ37, AK36, AL3, AL34, AM4, AN6, AN23, AN30, AP8, AP12, AP14, AP16, AP17, AP20, AP25, AR6, AR8, AR9, AR19, AR24, AR31, AR35, AR37, AT4, AT10, AT19, AT20, AT25, AU14, AU22, AU28, AU35	—	—	
GV_{DD}	AD4, AE3, AF1, AF5, AF35, AF37, AG2, AG36, AH33, AH34, AK5, AM1, AM35, AM37, AN2, AN10, AN11, AN12, AN14, AN32, AN36, AP5, AP23, AP28, AR1, AR7, AR10, AR12, AR21, AR25, AR27, AR33, AT15, AT22, AT28, AT33, AU2, AU5, AU16, AU31, AU36	Power for DDR DRAM I/O Voltage (2.5 V or 1.8 V)	GV_{DD}	
$LV_{DD}0$	D5, D6	Power for UCC1 Ethernet Interface (2.5V, 3.3V)	$LV_{DD}0$	

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$LV_{DD}1$	C17, D16	Power for UCC2 Ethernet Interface option 1 (2.5V, 3.3V)	LV_{DD1}	9
$LV_{DD}2$	B18, E21	Power for UCC2 Ethernet Interface Option 2 (2.5V, 3.3V)	$LV_{DD}2$	9
V_{DD}	C36, D29, D35, E16, F9, F12, F15, F17, F18, F20, F21, F23, F25, F26, F29, F31, F32, F33, G6, J6, K32, M32, N6, P33, R6, R32, U32, V6, Y5, Y32, AB6, AB33, AD6, AF32, AK6, AL6, AM7, AM9, AM10, AM11, AM12, AM13, AM14, AM15, AM18, AM21, AM25, AM28, AM32, AN15, AN21, AN26, AU9, AU17	Power for Core (1.2 V)	V_{DD}	
OV_{DD}	A10, B9, B15, B32, C1, C12, C22, C29, D24, E3, E10, E27, G4, H35, J1, J35, K2, M4, N3, N34, R2, R37, T36, U2, U33, V4, V34, W3, Y35, Y37, AA1, AA36, AB2, AB34	PCI, 10/100 Ethernet, and other Standard (3.3 V)	OV_{DD}	
MVREF1	AN20	I	DDR Reference Voltage	
MVREF2	AU32	I	DDR Reference Voltage	
SPARE1	B11	I/O	OV_{DD}	
SPARE3	AH32	—	GV_{DD}	8
SPARE4	AU18	—	GV_{DD}	7
SPARE5	AP1	—	GV_{DD}	8
No Connect				

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
NC	AM20, AU19	—	—	—

Notes:

1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV_{DD}
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
6. These are On Die Termination pins, used to control DDR2 memories internal termination resistance
7. This pin must always be tied to GND.
8. This pin must always be left not connected.
9. Refers to *MPC8360E PowerQUICC II™ Pro Integrated Communications Processor Reference Manual* section on "RGMII Pins" for information about the two UCC2 Ethernet interface options.
10. It is recommended that MDIC0 be tied to GND using an 18.2 Ω resistor and MDIC1 be tied to DDR power using an 18.2 Ω resistor for DDR2.

Table 67 shows the pin list of the MPC8358E TBGA package.

Table 67. MPC8358E TBGA Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Controller Interface				
MEMC1_MDQ[0:63]	AJ34, AK33, AL33, AL35, AJ33, AK34, AK32, AM36, AN37, AN35, AR34, AT34, AP37, AP36, AR36, AT35, AP34, AR32, AP32, AM31, AN33, AM34, AM33, AM30, AP31, AM27, AR30, AT32, AN29, AP29, AN27, AR29, AN8, AN7, AM8, AM6, AP9, AN9, AT7, AP7, AU6, AP6, AR4, AR3, AT6, AT5, AR5, AT3, AP4, AM5, AP3, AN3, AN5, AL5, AN4, AM2, AL2, AH5, AK3, AJ2, AJ3, AH4, AK4, AH3	I/O	GV_{DD}	
MEMC_MECC[0:4]/ MSRCID[0:4]	AP24, AN22, AM19, AN19, AM24	I/O	GV_{DD}	
MEMC_MECC[5]/ MDVAL	AM23	I/O	GV_{DD}	
MEMC_MECC[6:7]	AM22, AN18	I/O	GV_{DD}	
MEMC_MDM[0:8]	AL36, AN34, AP33, AN28,AT9, AU4, AM3, AJ6,AP27	O	GV_{DD}	
MEMC_MDQS[0:8]	AK35, AP35, AN31, AM26,AT8, AU3, AL4, AJ5, AP26	I/O	GV_{DD}	
MEMC_MBA[0:1]	AU29, AU30	O	GV_{DD}	
MEMC_MBA[2]	AT30	O	GV_{DD}	
MEMC_MA[0:14]	AU21, AP22, AP21, AT21, AU25, AU26, AT23, AR26, AU24, AR23, AR28, AU23, AR22, AU20, AR18	O	GV_{DD}	
MEMC_MODT[0:3]	AG33, AJ36, AT1, AK2	O	GV_{DD}	6
$\overline{\text{MEMC\_MWE}}$	AT26	O	GV_{DD}	
$\overline{\text{MEMC\_MRAS}}$	AT29	O	GV_{DD}	
$\overline{\text{MEMC\_MCAS}}$	AT24	O	GV_{DD}	

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MCS[0:3]	AU27, AT27, AU8, AU7	O	GV_{DD}	
MEMC_MCKE[0:1]	AL32, AU33	O	GV_{DD}	3
MEMC_MCK[0:5]	AK37, AT37, AN1, AR2, AN25, AK1	O	GV_{DD}	
MEMC_MCK[0:5]	AL37, AT36, AP2, AT2, AN24, AL1	O	GV_{DD}	
MDIC[0:1]	AH6, AP30	I/O	GV_{DD}	11
PCI				
PCI_INTA/ IRQ_OUT/ CE_PF[5]	A20	I/O	$LV_{DD}2$	2
PCI_RESET_OUT/ CE_PF[6]	E19	I/O	$LV_{DD}2$	
PCI_AD[31:30]/ CE_PG[31:30]	D20, D21	I/O	$LV_{DD}2$	
PCI_AD[29:25]/ CE_PG[29:25]	A24, B23, C23, E23, A26	I/O	OV_{DD}	
PCI_AD[24]/ CE_PG[24]	B21	I/O	$LV_{DD}2$	
PCI_AD[23:0]/ CE_PG[23:0]	C24, C25, D25, B25, E24, F24, A27, A28, F27, A30, C30, D30, E29, B31, C31, D31, D32, A32, C33, B33, F30, E31, A34, D33	I/O	OV_{DD}	
PCI_C/ BE[3:0]/ CE_PF[10:7]	E22, B26, E28, F28	I/O	OV_{DD}	
PCI_PAR/ CE_PF[11]	D28	I/O	OV_{DD}	
PCI_FRAME/ CE_PF[12]	D26	I/O	OV_{DD}	5
PCI_TRDY/ CE_PF[13]	C27	I/O	OV_{DD}	5
PCI_IRDY/ CE_PF[14]	C28	I/O	OV_{DD}	5
PCI_STOP/ CE_PF[15]	B28	I/O	OV_{DD}	5
PCI_DEVSEL/ CE_PF[16]	E26	I/O	OV_{DD}	5
PCI_IDSEL/ CE_PF[17]	F22	I/O	OV_{DD}	
PCI_SERR/ CE_PF[18]	B29	I/O	OV_{DD}	5
PCI_PERR/ CE_PF[19]	A29	I/O	OV_{DD}	5
PCI_REQ[0]/ CE_PF[20]	F19	I/O	$LV_{DD}2$	

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_REQ[1]/ CPCI_HS_ES/ CE_PF[21]	A21	I/O	$LV_{DD}2$	
PCI_REQ[2]/ CE_PF[22]	C21	I/O	$LV_{DD}2$	
PCI_GNT[0]/ CE_PF[23]	E20	I/O	$LV_{DD}2$	
PCI_GNT[1]/ CPCI1_HS_LED/ CE_PF[24]	B20	I/O	$LV_{DD}2$	
PCI_GNT[2]/ CPCI1_HS_ENUM/ CE_PF[25]	C20	I/O	$LV_{DD}2$	
PCI_MODE	D36	I	OV_{DD}	
M66EN/CE_PF[4]	B37	I/O	OV_{DD}	
Local Bus Controller Interface				
LAD[0:31]	N32, N33, N35, N36, P37, P32, P34, R36, R35, R34, R33, T37, T35, T34, T33, U37, T32, U36, U34, V36, V35, W37, W35, V33, V32, W34, Y36, W32, AA37, Y33, AA35, AA34	I/O	OV_{DD}	
LDP[0]/ CKSTOP_OUT	AB37	I/O	OV_{DD}	
LDP[1]/ CKSTOP_IN	AB36	I/O	OV_{DD}	
LDP[2]/ LCS[6]	AB35	I/O	OV_{DD}	
LDP[3]/ LCS[7]	AA33	I/O	OV_{DD}	
LA[27:31]	AC37, AA32, AC36, AC34, AD36	O	OV_{DD}	
LCS[0:5]	AD33, AG37, AF34, AE33, AD32, AH37	O	OV_{DD}	
LWE[0:3]/ LSDDQM[0:3]/ LBS[0:3]	AG35, AG34, AH36, AE32	O	OV_{DD}	
LBCTL	AD35	O	OV_{DD}	
LALE	M37	O	OV_{DD}	
LGPL0/ LSDA10/ cfg_reset_source0	AB32	I/O	OV_{DD}	
LGPL1/ LSDWE/ cfg_reset_source1	AE37	I/O	OV_{DD}	
LGPL2/ LSDRAS/ LOE	AC33	O	OV_{DD}	

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LGPL3/ LSDCAS/ cfg_reset_source2	AD34	I/O	OV_{DD}	
LGPL4/ LGTA/ LUPWAIT/ LPBSE	AE35	I/O	OV_{DD}	
LGPL5/ cfg_clkin_div	AF36	I/O	OV_{DD}	
LCKE	G36	O	OV_{DD}	
LCLK[0]	J33	O	OV_{DD}	
LCLK[1]/ LCS[6]	J34	O	OV_{DD}	
LCLK[2]/ LCS[7]	G37	O	OV_{DD}	
LSYNC_OUT	F34	O	OV_{DD}	
LSYNC_IN	G35	I	OV_{DD}	
Programmable Interrupt Controller				
MCP_OUT	E34	O	OV_{DD}	2
IRQ0/ MCP_IN	C37	I	OV_{DD}	
IRQ[1]/ M1SRCID[4]/ M2SRCID[4]/ LSRCID[4]	F35	I/O	OV_{DD}	
IRQ[2]/ M1DVAL/ M2DVAL/ LDVAL	F36	I/O	OV_{DD}	
IRQ[3]/ CORE_SRESET	H34	I/O	OV_{DD}	
IRQ[4:5]	G33, G32	I/O	OV_{DD}	
IRQ[6]/ LCS[6]/ CKSTOP_OUT	E35	I/O	OV_{DD}	
IRQ[7]/ LCS[7]/ CKSTOP_IN	H36	I/O	OV_{DD}	
DUART				
UART1_SOUT/ M1SRCID[0]/ M2SRCID[0]/ LSRCID[0]	E32	O	OV_{DD}	

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
UART1_SIN/ M1SRCID[1]/ M2SRCID[1]/ LSRCID[1]	B34	I/O	OV_{DD}	
$\overline{\text{UART1\_CTS}}$/ M1SRCID[2]/ M2SRCID[2]/ LSRCID[2]	C34	I/O	OV_{DD}	
$\overline{\text{UART1\_RTS}}$/ M1SRCID[3]/ M2SRCID[3]/ LSRCID[3]	A35	O	OV_{DD}	
I^2C Interface				
IIC1_SDA	D34	I/O	OV_{DD}	2
IIC1_SCL	B35	I/O	OV_{DD}	2
IIC2_SDA	E33	I/O	OV_{DD}	2
IIC2_SCL	C35	I/O	OV_{DD}	2
QUICC™ Engine				
CE_PA[0]	F8	I/O	LV_{DD0}	
CE_PA[1:2]	AH1, AG5	I/O	OV_{DD}	
CE_PA[3:7]	F6, D4, C3, E5, A3	I/O	$LV_{DD}0$	
CE_PA[8]	AG3	I/O	OV_{DD}	
CE_PA[9:12]	F7, B3, E6, B4	I/O	$LV_{DD}0$	
CE_PA[13:14]	AG1, AF6	I/O	OV_{DD}	
CE_PA[15]	B2	I/O	$LV_{DD}0$	
CE_PA[16]	AF4	I/O	OV_{DD}	
CE_PA[17:21]	B16, A16, E17, A17, B17	I/O	$LV_{DD}1$	
CE_PA[22]	AF3	I/O	OV_{DD}	
CE_PA[23:26]	C18, D18, E18, A18	I/O	$LV_{DD}1$	
CE_PA[27:28]	AF2, AE6	I/O	OV_{DD}	
CE_PA[29]	B19	I/O	$LV_{DD}1$	
CE_PA[30]	AE5	I/O	OV_{DD}	
CE_PA[31]	F16	I/O	$LV_{DD}1$	
CE_PB[0:27]	AE2, AE1, AD5, AD3, AD2, AC6, AC5, AC4, AC2, AC1, AB5, AB4, AB3, AB1, AA6, AA4, AA2, Y6, Y4, Y3, Y2, Y1, W6, W5, W2, V5, V3, V2	I/O	OV_{DD}	
CE_PC[0:1]	V1, U6	I/O	OV_{DD}	
CE_PC[2:3]	C16, A15	I/O	$LV_{DD}1$	
CE_PC[4:6]	U4, U3, T6	I/O	OV_{DD}	
CE_PC[7]	C19	I/O	$LV_{DD}2$	
CE_PC[8:9]	A4, C5	I/O	$LV_{DD}0$	

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
CE_PC[10:30]	T5, T4, T2, T1, R5, R3, R1, C11, D12, F13, B10, C10, E12, A9, B8, D10, A14, E15, B14, D15, AH2	I/O	OV_{DD}	
CE_PD[0:27]	E11, D9, C8, F11, A7, E9, C7, A6, F10, B6, D7, E8, B5, A5, C2, E4, F5, B1, D2, G5, D1, E2, H6, F3, E1, F2, G3, H4	I/O	OV_{DD}	
CE_PE[0:31]	K3, J2, F1, G2, J5, H3, G1, H2, K6, J3, K5, K4, L6, P6, P4, P3, P1, N4, N5, N2, N1, M2, M3, M5, M6, L1, L2, L4, E14, C13, C14, B13	I/O	OV_{DD}	
CE_PF[0:3]	F14, D13, A12, A11	I/O	OV_{DD}	
Clocks				
PCI_CLK_OUT[0]/ CE_PF[26]	B22	I/O	$LV_{DD}2$	
PCI_CLK_OUT[1:2]/ CE_PF[27:28]	D22, A23	I/O	OV_{DD}	
CLKIN	E37	I	OV_{DD}	
PCI_CLOCK/ PCI_SYNC_IN	M36	I	OV_{DD}	
PCI_SYNC_OUT/ CE_PF[29]	D37	I/O	OV_{DD}	3
JTAG				
TCK	K33	I	OV_{DD}	
TDI	K34	I	OV_{DD}	4
TDO	H37	O	OV_{DD}	3
TMS	J36	I	OV_{DD}	4
$\overline{\text{TRST}}$	L32	I	OV_{DD}	4
Test				
TEST	L35	I	OV_{DD}	7
$\overline{\text{TEST\_SEL}}$	AU34	I	GV_{DD}	10
PMC				
$\overline{\text{QUIESCE}}$	B36	O	OV_{DD}	
System Control				
$\overline{\text{PORESET}}$	L37	I	OV_{DD}	
$\overline{\text{HRESET}}$	L36	I/O	OV_{DD}	1
$\overline{\text{SRESET}}$	M33	I/O	OV_{DD}	2
Thermal Management				
THERM0	AP19	I	GV_{DD}	
THERM1	AT31	I	GV_{DD}	

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Power and Ground Signals				
$AV_{DD}1$	K35	Power for LBIU DLL (1.2 V)	$AV_{DD}1$	
$AV_{DD}2$	K36	Power for CE PLL (1.2 V)	$AV_{DD}2$	
$AV_{DD}5$	AM29	Power for e300 PLL (1.2 V)	$AV_{DD}5$	
$AV_{DD}6$	K37	Power for system PLL (1.2 V)	$AV_{DD}6$	
GND	A2, A8, A13, A19, A22, A25, A31, A33, A36, B7, B12, B24, B27, B30, C4, C6, C9, C15, C26, C32, D3, D8, D11, D14, D17, D19, D23, D27, E7, E13, E25, E30, E36, F4, F37, G34, H1, H5, H32, H33, J4, J32, J37, K1, L3, L5, L33, L34, M1, M34, M35, N37, P2, P5, P35, P36, R4, T3, U1, U5, U35, V37, W1, W4, W33, W36, Y34, AA3, AA5, AC3, AC32, AC35, AD1, AD37, AE4, AE34, AE36, AF33, AG4, AG6, AG32, AH35, AJ1, AJ4, AJ32, AJ35, AJ37, AK36, AL3, AL34, AM4, AN6, AN23, AN30, AP8, AP12, AP14, AP16, AP17, AP20, AP25, AR6, AR8, AR9, AR19, AR24, AR31, AR35, AR37, AT4, AT10, AT19, AT20, AT25, AU14, AU22, AU28, AU35	—	—	
GV_{DD}	AD4, AE3, AF1, AF5, AF35, AF37, AG2, AG36, AH33, AH34, AK5, AM1, AM35, AM37, AN2, AN10, AN11, AN12, AN14, AN32, AN36, AP5, AP23, AP28, AR1, AR7, AR10, AR12, AR21, AR25, AR27, AR33, AT15, AT22, AT28, AT33, AU2, AU5, AU16, AU31, AU36	Power for DDR DRAM I/O Voltage (2.5 V or 1.8 V)	GV_{DD}	
$LV_{DD}0$	D5, D6	Power for UCC1 Ethernet Interface (2.5V, 3.3V)	$LV_{DD}0$	
$LV_{DD}1$	C17, D16	Power for UCC2 Ethernet Interface option 1 (2.5V, 3.3V)	$LV_{DD}1$	9

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$LV_{DD}2$	B18, E21	Power for UCC2 Ethernet Interface Option 2 (2.5V, 3.3V)	$LV_{DD}2$	9
V_{DD}	C36, D29, D35, E16, F9, F12, F15, F17, F18, F20, F21, F23, F25, F26, F29, F31, F32, F33, G6, J6, K32, M32, N6, P33, R6, R32, U32, V6, Y5, Y32, AB6, AB33, AD6, AF32, AK6, AL6, AM7, AM9, AM10, AM11, AM12, AM13, AM14, AM15, AM18, AM21, AM25, AM28, AM32, AN15, AN21, AN26, AU9, AU17	Power for Core (1.2 V)	V_{DD}	
OV_{DD}	A10, B9, B15, B32, C1, C12, C22, C29, D24, E3, E10, E27, G4, H35, J1, J35, K2, M4, N3, N34, R2, R37, T36, U2, U33, V4, V34, W3, Y35, Y37, AA1, AA36, AB2, AB34	PCI, 10/100 Ethernet, and other Standard (3.3 V)	OV_{DD}	
MVREF1	AN20	I	DDR Reference Voltage	
MVREF2	AU32	I	DDR Reference Voltage	
SPARE1	B11	I/O	OV_{DD}	
SPARE3	AH32	—	GV_{DD}	8
SPARE4	AU18	—	GV_{DD}	7
SPARE5	AP1	—	GV_{DD}	8
No Connect				

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
NC	AM16, AM17, AM20, AN13, AN16, AN17, AP10, AP11, AP13, AP15, AP18, AR11, AR13, AR14, AR15, AR16, AR17, AR20, AT11, AT12, AT13, AT14, AT16, AT17, AT18, AU10, AU11, AU12, AU13, AU15, AU19	—	—	—

Notes:

1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV_{DD}.
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
6. These are On Die Termination pins, used to control DDR2 memories internal termination resistance.
7. This pin must always be tied to GND.
8. This pin must always be left not connected.
9. Refers to *MPC8360E PowerQUICC II™ Pro Integrated Communications Processor Reference Manual* section on "RGMII Pins" for information about the two UCC2 Ethernet interface options.
10. This pin must always be tied to GV_{DD}.
11. It is recommended that MDIC0 be tied to GND using an 18.2 Ω resistor and MDIC1 be tied to DDR power using an 18.2 Ω resistor for DDR2.

22 Clocking

Figure 53 shows the internal distribution of clocks within the MPC8360E.

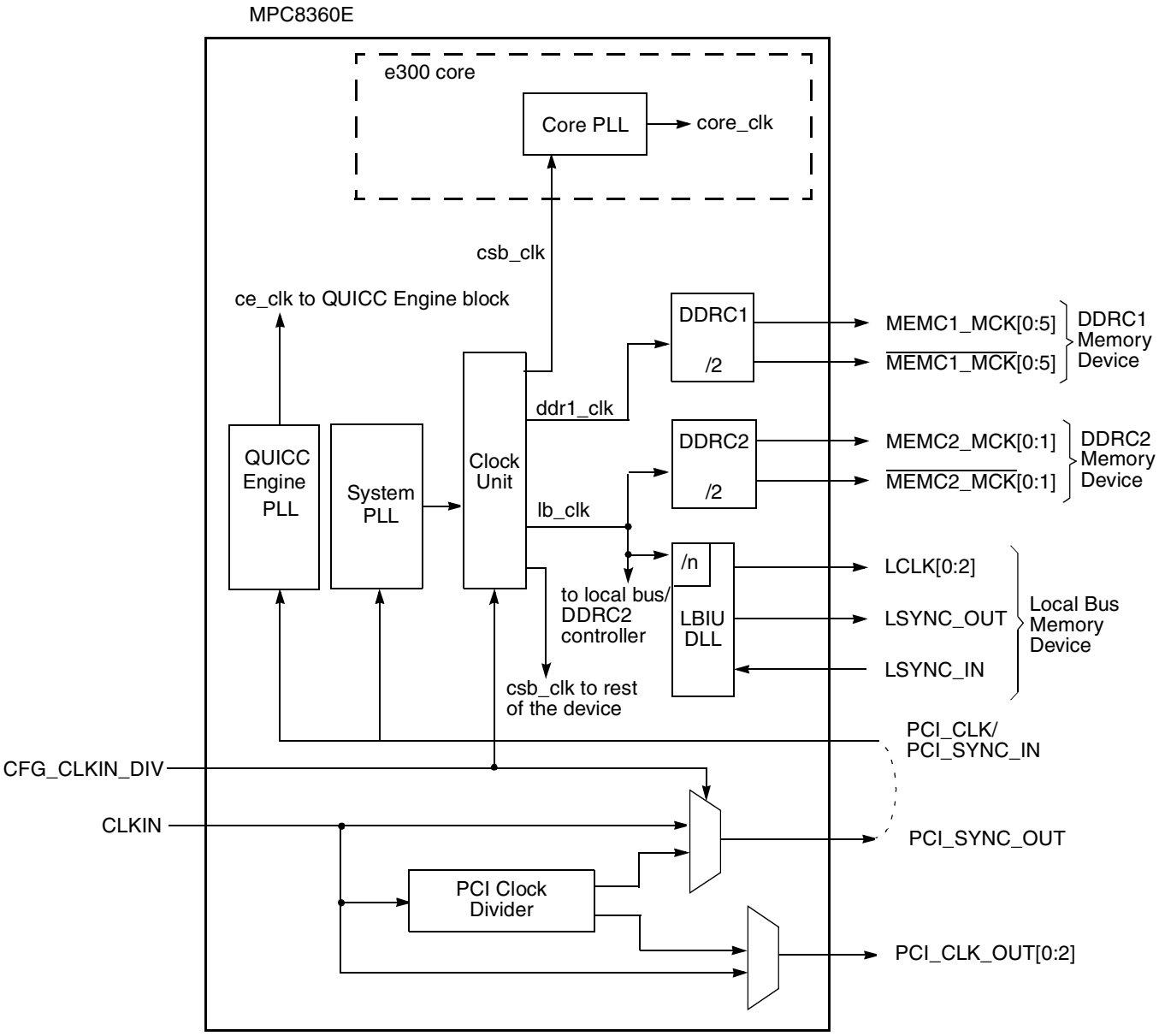


Figure 53. MPC8360E Clock Subsystem

Figure 54 shows the internal distribution of clocks within the MPC8358E.

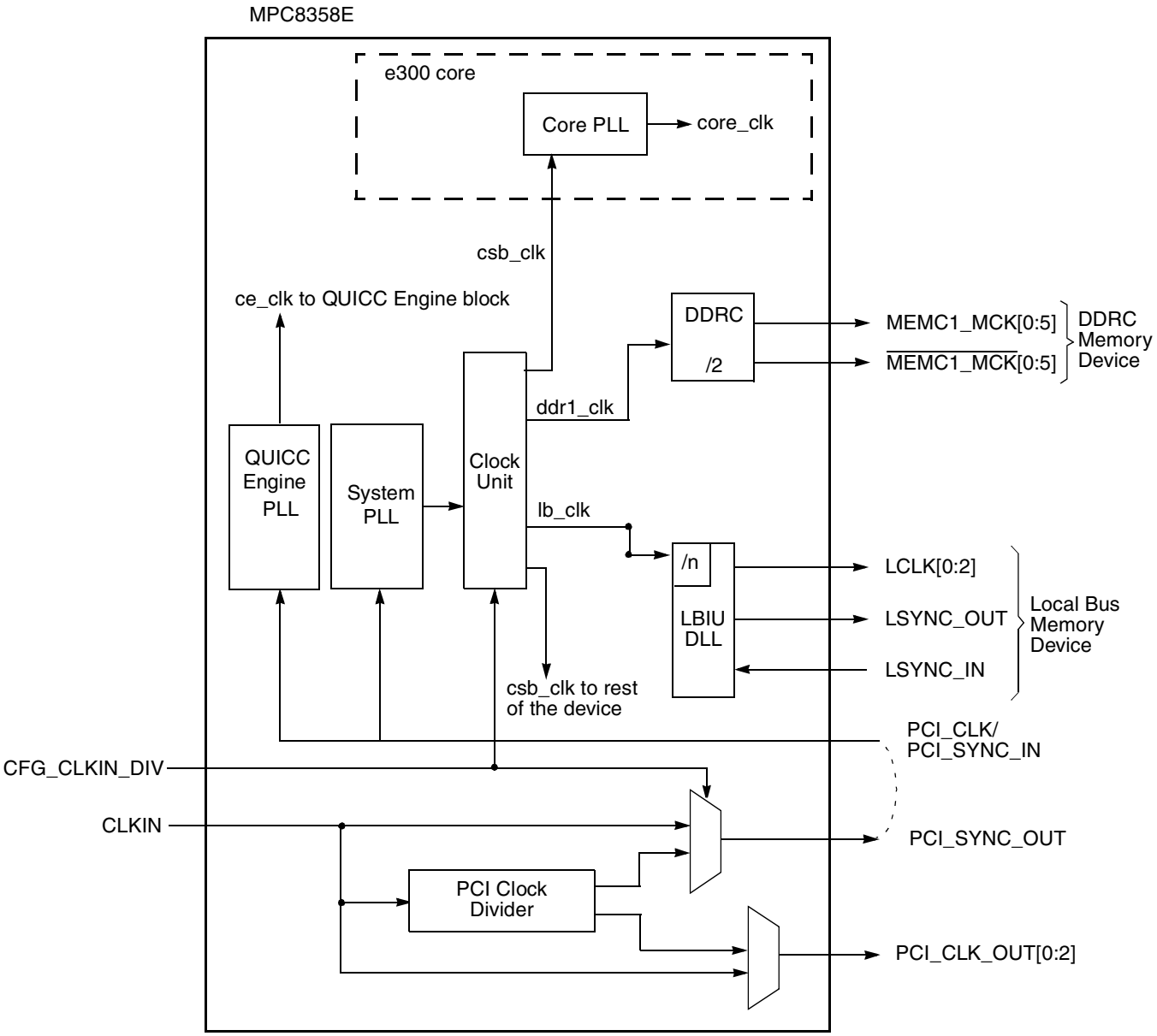


Figure 54. MPC8358E Clock Subsystem

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Note that in PCI host mode, the primary clock input also depends on whether PCI clock outputs are selected with RCWH[PCICKEN]. When the device is configured as a PCI host device (RCWH[PCIHOST] = 1) and PCI clock output is selected (RCWH[PCICKEN] = 1), CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCICD*n*] parameters select whether CLKIN or CLKIN/2 is driven out on the PCI_CLK_OUT*n* signals.The OCCR[PCIOEN*n*] parameters enable the PCI_CLK_OUT*n* respectively.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock. When the device is configured as a PCI agent device the CLKIN and the CFG_CLKIN_DIV signals should be tied to GND.

When the device is configured as a PCI host device (RCWH[PCIHOST] = 1) and PCI clock output is disabled (RCWH[PCICKEN] = 0), clock distribution and balancing done externally on the board. Therefore, PCI_SYNC_IN is the primary input clock.

As shown in Figure 53, the primary clock input (frequency) is multiplied by the QUICC Engine block phase-locked loop (PLL), the system PLL, and the clock unit to create the QUICC Engine clock (*ce_clk*), the coherent system bus clock (*csb_clk*), the internal DDRC1 controller clock (*ddr1_clk*), and the internal clock for the local bus interface unit and DDR2 memory controller (*lb_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = \{PCI\_SYNC\_IN \times (1 + CFG\_CLKIN\_DIV)\} \times SPMF$$

In PCI host mode, PCI_SYNC_IN × (1 + CFG_CLKIN_DIV) is the CLKIN frequency; in PCI agent mode, CFG_CLKIN_DIV must be pulled down (low), so PCI_SYNC_IN × (1 + CFG_CLKIN_DIV) is the PCI_CLK frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, “Reset, Clocking, and Initialization,” in the *MPC8360E Integrated Communications Processor Reference Manual, Rev. 2* for more information on the clock subsystem.

The *ce_clk* frequency is determined by the QUICC Engine PLL multiplication factor (RCWL[CEPMF) and the QUICC Engine PLL division factor (RCWL[CEPDF]) according to the following equation:

$$ce\_clk = (\text{primary clock input} \times CEPMF) \div (1 + CEPDF)$$

The internal *ddr1_clk* frequency is determined by the following equation:

$$ddr1\_clk = csb\_clk \times (1 + RCWL[DDR1CM])$$

Note that the lb_clk clock frequency (for DDRC2) is determined by RCWL[LBCM]. The *internal ddr1_clk* frequency is not the external memory bus frequency; *ddr1_clk* passes through the DDRC1 clock divider (÷2) to create the differential DDRC1 memory bus clock outputs (MEMC1_MCK and $\overline{\text{MEMC1\_MCK}}$). However, the data rate is the same frequency as *ddr1_clk*.

The internal *lb_clk* frequency is determined by the following equation:

$$lb\_clk = csb\_clk \times (1 + RCWL[LBCM])$$

Note that *lb_clk* is not the external local bus or DDRC2 frequency; *lb_clk* passes through the a LB clock divider to create the external local bus clock outputs (LSYNC_OUT and LCLK[0:2]). The LB clock divider ratio is controlled by LCCR[CLKDIV].

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 68 specifies which units have a configurable clock frequency.

Table 68. Configurable Clock Units

Unit	Default Frequency	Options
Security Core	*csb_clk*/3	Off, *csb_clk* [1], *csb_clk*/2, *csb_clk*/3
PCI and DMA complex	csb_clk	Off, *csb_clk*

1 with limitation, only for slow csb_clk rates, up to 166MHz

Table 69 provides the operating frequencies for the TBGA package under recommended operating conditions (see Table 2). All frequency combinations shown in the table below may not be available. Maximum operating frequencies depend on the part ordered, see Section 26.1, "Part Numbers Fully Addressed by this Document" for part ordering details and contact your Freescale Sales Representative or authorized distributor for more information.

Table 69. Operating Frequencies for the TBGA Package

Characteristic [1]	400 MHz	533 MHz	667 MHz [2]	Unit
e300 core frequency (*core_clk*)	266–400	266–533	266–667	MHz
Coherent system bus frequency (*csb_clk*)	133–333			MHz
QUICC Engine frequency [3] (*ce_clk*)	266–500			MHz
DDR and DDR2 memory bus frequency (MCLK) [4]	100–166.67			MHz
Local bus frequency (LCLK*n*) [5]	16.67–133			MHz
PCI input frequency (CLKIN or PCI_CLK)	25–66.67			MHz
Security core maximum internal operating frequency	133	133	166	MHz

1 The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.

2 The 667 MHz core frequency is based on a 1.3 V V_{DD} supply voltage.

3 The 500 MHz QE frequency is based on a 1.3 V V_{DD} supply voltage.

4 The DDR data rate is 2x the DDR memory bus frequency.

5 The local bus frequency is 1/2, 1/4, or 1/8 of the *lb_clk* frequency (depending on LCCR[CLKDIV]) which is in turn 1x or 2x the *csb_clk* frequency (depending on RCWL[LBCM]).

22.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] and RCWL[SVCOD] parameters. Table 70 shows the multiplication factor encodings for the system PLL.

Table 70. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	× 16
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111	× 7
1000	× 8
1001	× 9
1010	× 10
1011	× 11
1100	× 12
1101	× 13
1110	× 14
1111	× 15

The RCWL[SVCOD] denotes the system PLL VCO internal frequency as shown in Table 71.

Table 71. System PLL VCO Divider

RCWL[SVCOD]	VCO Divider
00	4
01	8
10	2
11	Reserved

NOTE

The VCO divider must be set properly so that the system VCO frequency is in the range of 600-1400 MHz.

The system VCO frequency is derived from the following equations:

$$csb\_clk = \{PCI\_SYNC\_IN \times (1 + CFG\_CLKIN\_DIV)\} \times SPMF$$

System VCO Frequency = *csb_clk* × VCO divider

As described in Section 22, "Clocking," the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 72 shows the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

Table 72. CSB Frequency Options

CFG_CLKIN_DIV at reset [1]	SPMF	*csb_clk* : Input Clock Ratio [2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2 : 1				133
Low	0011	3 : 1			100	200
Low	0100	4 : 1		100	133	266
Low	0101	5 : 1		125	166	333
Low	0110	6 : 1	100	150	200	
Low	0111	7 : 1	116	175	233	
Low	1000	8 : 1	133	200	266	
Low	1001	9 : 1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233			
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			

Table 72. CSB Frequency Options (continued)

CFG_CLKIN_DIV at reset [1]	SPMF	*csb_clk* : Input Clock Ratio [2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
High	0010	2 : 1				133
High	0011	3 : 1			100	200
High	0100	4 : 1			133	266
High	0101	5 : 1			166	333
High	0110	6 : 1			200	
High	0111	7 : 1			233	
High	1000	8 : 1				
High	1001	9 : 1				
High	1010	10 : 1				
High	1011	11 : 1				
High	1100	12 : 1				
High	1101	13 : 1				
High	1110	14 : 1				
High	1111	15 : 1				
High	0000	16 : 1				

1 CFG_CLKIN_DIV is only used for host mode; CLKIN must be tied low and CFG_CLKIN_DIV must be pulled down (low) in agent mode.

2 CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

22.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 73 shows the encodings for RCWL[COREPLL]. COREPLL values not listed in Table 73 should be considered reserved.

Table 73. e300 Core PLL Configuration

RCWL[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO divider
0-1	2-5	6		
nn	**0000**	n	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
00	**0001**	0	1:1	÷2
01	**0001**	0	1:1	÷4

Table 73. e300 Core PLL Configuration (continued)

RCWL[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO divider
0-1	2-5	6		
10	**0001**	0	1:1	÷8
11	**0001**	0	1:1	÷8
00	**0001**	1	1.5:1	÷2
01	**0001**	1	1.5:1	÷4
10	**0001**	1	1.5:1	÷8
11	**0001**	1	1.5:1	÷8
00	**0010**	0	2:1	÷2
01	**0010**	0	2:1	÷4
10	**0010**	0	2:1	÷8
11	**0010**	0	2:1	÷8
00	**0010**	1	2.5:1	÷2
01	**0010**	1	2.5:1	÷4
10	**0010**	1	2.5:1	÷8
11	**0010**	1	2.5:1	÷8
00	**0011**	0	3:1	÷2
01	**0011**	0	3:1	÷4
10	**0011**	0	3:1	÷8
11	**0011**	0	3:1	÷8

NOTE

Core VCO frequency = Core frequency × VCO divider. VCO divider (RCWL[COREPLL[0:1]]) must be set properly so that the core VCO frequency is in the range of 800–1800 MHz. Having a core frequency below the CSB frequency is not a possible option because the core frequency must be equal to or greater than the CSB frequency.

22.3 QUICC Engine PLL Configuration

The QUICC Engine PLL is controlled by the RCWL[CEPMF], RCWL[CEPDF], and RCWL[CEVCOD] parameters. Table 74 shows the multiplication factor encodings for the QUICC Engine PLL.

Table 74. QUICC Engine PLL Multiplication Factors

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF] / (1+RCWL[CEPDF])
00000	0	× 16
00001	0	Reserved
00010	0	× 2
00011	0	× 3
00100	0	× 4
00101	0	× 5
00110	0	× 6
00111	0	× 7
01000	0	× 8
01001	0	× 9
01010	0	× 10
01011	0	× 11
01100	0	× 12
01101	0	× 13
01110	0	× 14
01111	0	× 15
10000	0	× 16
10001	0	× 17
10010	0	× 18
10011	0	× 19
10100	0	× 20
10101	0	× 21
10110	0	× 22
10111	0	× 23
11000	0	× 24
11001	0	× 25
11010	0	× 26
11011	0	× 27

Table 74. QUICC Engine PLL Multiplication Factors (continued)

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF] / (1+RCWL[CEPDF])
11100	0	× 28
11101	0	× 29
11110	0	× 30
11111	0	× 31
00011	1	× 1.5
00101	1	× 2.5
00111	1	× 3.5
01001	1	× 4.5
01011	1	× 5.5
01101	1	× 6.5
01111	1	× 7.5
10001	1	× 8.5
10011	1	× 9.5
10101	1	× 10.5
10111	1	× 11.5
11001	1	× 12.5
11011	1	× 13.5
11101	1	× 14.5

Notes

1. Reserved modes are not listed.

The RCWL[CEVCOD] denotes the QE PLL VCO internal frequency as shown in Table 75.

Table 75. QE PLL VCO Divider

RCWL[CEVCOD]	VCO Divider
00	4
01	8
10	2
11	Reserved

NOTE

The VCO divider (RCWL[CEVCOD]) must be set properly so that the QE VCO frequency is in the range of 600–1400 MHz. The QE frequency is not restricted by the CSB and core frequencies. The CSB, core, and QE frequencies should be selected according to the performance requirements.

The QE VCO frequency is derived from the following equations:

ce_clk = (primary clock input × CEPMF) ÷ (1 + CEPDF)

QE VCO Frequency = *ce_clk* × VCO divider × (1 + CEPDF)

22.4 Suggested PLL Configurations

To simplify the PLL configurations, the device might be separated into two clock domains. The first domain contains the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the csb_clk as its input clock. The second clock domain has the QUICC Engine PLL. The clock domains are independent, and each of their PLLs are configured separately. Both of the domains has one common input clock. Table 76 shows suggested PLL configurations for 33 MHz and 66 MHz input clocks and illustrates each of the clock domains separately. Any combination of clock domains setting with same input clock are valid. Refer to Section 22, "Clocking," for the appropriate operating frequencies for your device.

Table 76. Suggested PLL Configurations

Conf No. [1]	SPMF	CORE PLL	CEPMF	CEPDF	Input Clock Freq (MHz)	CSB Freq (MHz)	Core Freq (MHz)	QUICC Engine Freq (MHz)	400 (MHz)	533 (MHz)	667 (MHz)
33 MHz CLKIN / PCI_SYNC_IN Options											
s1	**0100**	**0000100**	æ	æ	33	133	266		∞	∞	∞
s2	**0100**	**0000101**	æ	æ	33	133	333		∞	∞	∞
s3	**0101**	**0000100**	æ	æ	33	166	333		∞	∞	∞
s4	**0101**	**0000101**	æ	æ	33	166	416			∞	∞
s5	**0110**	**0000100**	æ	æ	33	200	400		∞	∞	∞
s6	**0110**	**0000110**	æ	æ	33	200	600				∞
s7	**0111**	**0000011**	æ	æ	33	233	350		∞	∞	∞
s8	**0111**	**0000100**	æ	æ	33	233	466			∞	∞
s9	**0111**	**0000101**	æ	æ	33	233	583				∞
s10	**1000**	**0000011**	æ	æ	33	266	400		∞	∞	∞
s11	**1000**	**0000100**	æ	æ	33	266	533			∞	∞
s12	**1000**	**0000101**	æ	æ	33	266	667				∞
s13	**1001**	**0000010**	æ	æ	33	300	300		∞	∞	∞
s14	**1001**	**0000011**	æ	æ	33	300	450			∞	∞
s15	**1001**	**0000100**	æ	æ	33	300	600				∞

Table 76. Suggested PLL Configurations (continued)

Conf No. [1]	SPMF	CORE PLL	CEPMF	CEPDF	Input Clock Freq (MHz)	CSB Freq (MHz)	Core Freq (MHz)	QUICC Engine Freq (MHz)	400 (MHz)	533 (MHz)	667 (MHz)
s16	**1010**	**0000010**	æ	æ	33	333	333		∞	∞	∞
s17	**1010**	**0000011**	æ	æ	33	333	500			∞	∞
s18	**1010**	**0000100**	æ	æ	33	333	667				∞
c1	æ	æ	**01001**	**0**	33			300	∞	∞	∞
c2	æ	æ	**01100**	**0**	33			400	∞	∞	∞
c3	æ	æ	**01110**	**0**	33			466		∞	∞
c4	æ	æ	**01111**	**0**	33			500		∞	∞
c5	æ	æ	**10000**	**0**	33			533		∞	∞
c6	æ	æ	**10001**	**0**	33			566			∞
66 MHz CLKIN / PCI_SYNC_IN Options											
s1h	**0011**	**0000110**	æ	æ	66	200	400		∞	∞	∞
s2h	**0011**	**0000101**	æ	æ	66	200	500			∞	∞
s3h	**0011**	**0000110**	æ	æ	66	200	600				∞
s4h	**0100**	**0000011**	æ	æ	66	266	400		∞	∞	∞
s5h	**0100**	**0000100**	æ	æ	66	266	533			∞	∞
s6h	**0100**	**0000101**	æ	æ	66	266	667				∞
s7h	**0101**	**0000010**	æ	æ	66	333	333		∞	∞	∞
s8h	**0101**	**0000011**	æ	æ	66	333	500			∞	∞
s9h	**0101**	**0000100**	æ	æ	66	333	667				∞
c1h	æ	æ	**00101**	**0**	66			333	∞	∞	∞
c2h	æ	æ	**00110**	**0**	66			400	∞	∞	∞
c3h	æ	æ	**00111**	**0**	66			466		∞	∞
c4h	æ	æ	**01000**	**0**	66			533		∞	∞
c5h	æ	æ	**01001**	**0**	66			600			∞

[1] The Conf No. consist of prefix, an index and a postfix. The prefix ‘s’ and ‘c’ stands for ‘syset’ and ‘ce’ respectively. the postfix ‘h’ stands for ‘high input clock.’ The index is a serial number.

The following steps describe how to use Table 76. See the example that follows:

1. Choose the up or down sections in the table according to input clock rate 33 MHz or 66 MHz.
2. Select a suitable CSB and core clock rates from Table 76. Copy the SPMF and CORE PLL configuration bits.
3. Select a suitable QUICC Engine clock rate from Table 76. Copy the CEPMF and CEPDF configuration bits.

4. Insert the chosen SPMF, COREPLL, CEPMF and CEPDF to the RCWL fields respectively.

Example:

Index	SPMF	CORE PLL	CEPMF	CEPDF	Input Clock (MHz)	CSB Freq (MHz)	Core Freq (MHz)	QUICC Engine Freq (MHz)	400 (MHz)	533 (MHz)	667 (MHz)
A	**1000**	**0000011**	**01001**	**0**	33	266	400	300	∞	∞	∞
B	**0100**	**0000100**	**00110**	**0**	66	266	533	400	∞	∞	∞

- **Example A.** To configure the device with CSB clock rate of 266 MHz, core rate of 400 MHz, and QUICC Engine clock rate 300 MHz while the input clock rate is 33 MHz. Conf No. “s10” and “c1” are selected from Table 76. SPMF is “1000,” CORPLL is “0000011,” CEPMF is “01001,” and CEPDF is “0.”
- **Example B.** To configure the device with CSBCSB clock rate of 266 MHz, core rate of 533 MHz and QUICC Engine clock rate 400 MHz while the input clock rate is 66 MHz. Conf No. “s5h” and “c2h” are selected from Table 76. SPMF is “0100,” CORPLL is “0000100,” CEPMF is “00110” and CEPDF is “0.”

23 Thermal

This section describes the thermal specifications of the MPC8360E/58E.

23.1 Thermal Characteristics

Table 77 provides the package thermal characteristics for the 740 37.5 mm x 37.5 mm TBGA package.

Table 77. Package Thermal Characteristics for the TBGA Package

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient Natural Convection on single layer board (1s)	$R_{\theta JA}$	15	°C/W	1, 2
Junction-to-ambient Natural Convection on four layer board (2s2p)	$R_{\theta JA}$	11	°C/W	1, 3
Junction-to-ambient (@1 m/s) on single layer board (1s)	$R_{\theta JMA}$	10	°C/W	1, 3
Junction-to-ambient (@ 1 m/s) on four layer board (2s2p)	$R_{\theta JMA}$	8	°C/W	1, 3
Junction-to-ambient (@ 2 m/s) on single layer board (1s)	$R_{\theta JMA}$	9	°C/W	1, 3
Junction-to-ambient (@ 2 m/s) on four layer board (2s2p)	$R_{\theta JMA}$	7	°C/W	1, 3
Junction-to-board thermal	$R_{\theta JB}$	4.5	°C/W	4
Junction-to-case thermal	$R_{\theta JC}$	1.1	°C/W	5

Table 77. Package Thermal Characteristics for the TBGA Package (continued)

Characteristic	Symbol	Value	Unit	Notes
Junction-to-Package Natural Convection on Top	Ψ_{JT}	1	°C/W	6

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 and SEMI G38-87with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal. 1 m/sec is approximately equal to 200 linear feet per minute (LFM).
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

23.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \text{ X } I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers. See Table 6 for typical power dissipations values.

23.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is appropriate for a tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity T_J - T_A) are possible.

23.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction to ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For

many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package will be approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device. At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (°C)

T_B = board temperature at the package perimeter (°C)

$R_{\theta JA}$ = junction to board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

23.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

23.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

In some application environments, a heat sink will be required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Table 78 shows heat sinks and junction-to-case thermal resistance for TBGA package.

Table 78. Heat Sinks and Junction-to-Case Thermal Resistance of TBGA Package

Heat Sink Assuming Thermal Grease	Air Flow	35x35 mm TBGA
		Junction-to-Ambient Thermal Resistance
AAVID 30x30x9.4 mm Pin Fin	Natural Convention	10.7
AAVID 30x30x9.4 mm Pin Fin	1 m/s	6.2
AAVID 30x30x9.4 mm Pin Fin	2 m/s	5.3
AAVID 31x35x23 mm Pin Fin	Natural Convention	8.1
AAVID 31x35x23 mm Pin Fin	1 m/s	4.4
AAVID 31x35x23 mm Pin Fin	2 m/s	3.7
Wakefield, 53x53x25 mm Pin Fin	Natural Convention	5.4
Wakefield, 53x53x25 mm Pin Fin	1 m/s	3.2
Wakefield, 53x53x25 mm Pin Fin	2 m/s	2.4
MEI, 75x85x12 no adjacent board, extrusion	Natural Convention	6.4
MEI, 75x85x12 no adjacent board, extrusion	1 m/s	3.8
MEI, 75x85x12 no adjacent board, extrusion	2 m/s	2.5
MEI, 75x85x12 mm, adjacent board, 40 mm Side bypass	1 m/s	2.8

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
473 Sapena Ct. #15
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Millennium Electronics (MEI) 408-436-8770
Loroco Sites
671 East Brokaw Road
San Jose, CA 95112
Internet: www.mei-millennium.com

Tyco Electronics 800-522-6752
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

Wakefield Engineering 603-635-5102
33 Bridge St.
Pelham, NH 03076
Internet: www.wakefield.com

Interface material vendors include the following:

Chomerics, Inc. 781-935-4850
77 Dragon Ct.
Woburn, MA 01888-4014
Internet: www.chomerics.com

Dow-Corning Corporation 800-248-2481
Dow-Corning Electronic Materials
2200 W. Salzburg Rd.
Midland, MI 48686-0997
Internet: www.dowcorning.com

Shin-Etsu MicroSi, Inc. 888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

The Bergquist Company
18930 West 78th St.
Chanhassen, MN 55317
Internet: www.bergquistcompany.com

800-347-4572

23.3 Heat Sink Attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. Recommended maximum force on the top of the package is 10 lb force (4.5 kg force). If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

23.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction to case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

T_J = junction temperature (°C)

T_C = case temperature of the package (°C)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

P_D = power dissipation (W)

24 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8360E/58E. Additional information can be found in AN3097, *MPC8360E/MPC8358E PowerQUICC™ Design Checklist, Rev. 1*.

24.1 System Clocking

The device includes two PLLs.

1. The platform PLL ($AV_{DD}1$) generates the platform clock from the externally supplied CLKIN input. The frequency ratio between the platform and CLKIN is selected using the platform PLL ratio configuration bits as described in Section 22.1, "System PLL Configuration."
2. The e300 core PLL ($AV_{DD}2$) generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 22.2, "Core PLL Configuration."

24.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins ($AV_{DD}1$, $AV_{DD}2$ respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages will be derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in Figure 55, one to each of the five AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

Figure 55 shows the PLL power supply filter circuit.

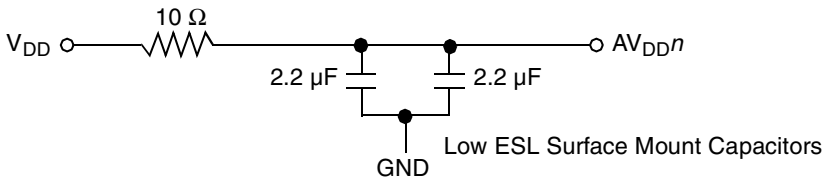


Figure 55. PLL Power Supply Filter Circuit

24.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the device system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pins of the device. These decoupling capacitors should receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, and GND

power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

24.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}, GV_{DD}, or LV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, and GND pins of the device.

24.5 Output Buffer DC Impedance

The device drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 56). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

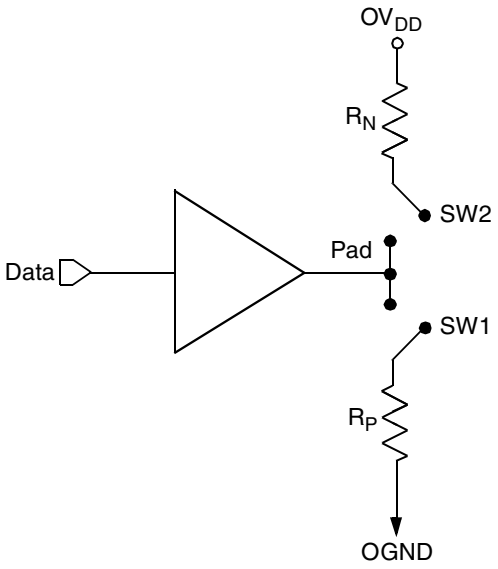


Figure 56. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 79 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 79. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	20 Target	Z_0	W
R_P	42 Target	25 Target	20 Target	Z_0	W
Differential	NA	NA	NA	Z_{DIFF}	W

Note: Nominal supply voltages. See Table 1, T_J = 105°C.

24.6 Configuration Pin Muxing

The device provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled

and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

24.7 Pull-Up Resistor Requirements

The device requires high resistance pull-up resistors (10 kΩ is recommended) on open drain type pins including I^2C pins, Ethernet Management MDIO pin, and EPIC interrupt pins.

For more information on required pull-up resistors and the connections required for the JTAG interface, see *AN3097, MPC8360E/MPC8358E PowerQUICC™ Design Checklist, Rev. 1*.

25 Document Revision History

Table 80 provides a revision history for this hardware specification.

Table 80. Document Revision History

Rev. Number	Date	Substantive Change(s)
0	12/07/2007	Initial release.

26 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 26.1, “Part Numbers Fully Addressed by this Document.”

26.1 Part Numbers Fully Addressed by this Document

Table 81 provides the Freescale part numbering nomenclature for the MPC8360E/58E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 81. Part Numbering Nomenclature [1]

MPC	*nnnn*	*e*	*t*	*pp*	*aa*	*a*	*a*	*A*
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature Range**	**Package [2]**	**Processor Frequency [3]**	**Platform Frequency**	**QUICC Engine Frequency**	**Die Revision**
MPC	8358	Blank = Not included E = included	0°C T_A to 105°C T_J	ZU = TBGA VV = TBGA (no lead)	e300 core speed AD = 266 MHz AG = 400 MHz	D = 266 MHz	E = 300 MHz G = 400 MHz	A=revision 2.1 silicon
	8360				e300 core speed AG = 400 MHz AJ = 533 MHz AL = 667 MHz	D = 266 MHz F = 333 MHz	G = 400 MHz H = 500 MHz	A=revision 2.1 silicon
MPC (rev2.0 silicon only)	8360	Blank = Not included E = included	0°C T_A to 70°C T_J	ZU = TBGA VV = TBGA (no lead)	e300 core speed AH = 500 MHz AL = 667 MHz	F = 333 MHz	G = 400 MHz H = 500 MHz	

1 Not all processor, platform, and QUICC Engine frequency combinations are supported. For available frequency combinations, contact your local Freescale Sales Office or authorized distributor.

2 See Section 21, "Package and Pin Listings," for more information on available package types.

3 Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.

Table 82 shows the SVR settings by device and package type.

Table 82. SVR Settings

Device	Package	SVR (Rev 2.0)	SVR (Rev 2.1)
MPC8360E	TBGA	0x8048_0020	0x8048_0021
MPC8360	TBGA	0x8049_0020	0x8049_0021
MPC8358E	TBGA	0x804A_0020	0x804A_0021
MPC8358	TBGA	0x804B_0020	0x804B_0021

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