

200mA, Low Quiescent Current, Ultra-Low Noise, High PSRR Low Dropout Linear Regulator

FEATURES

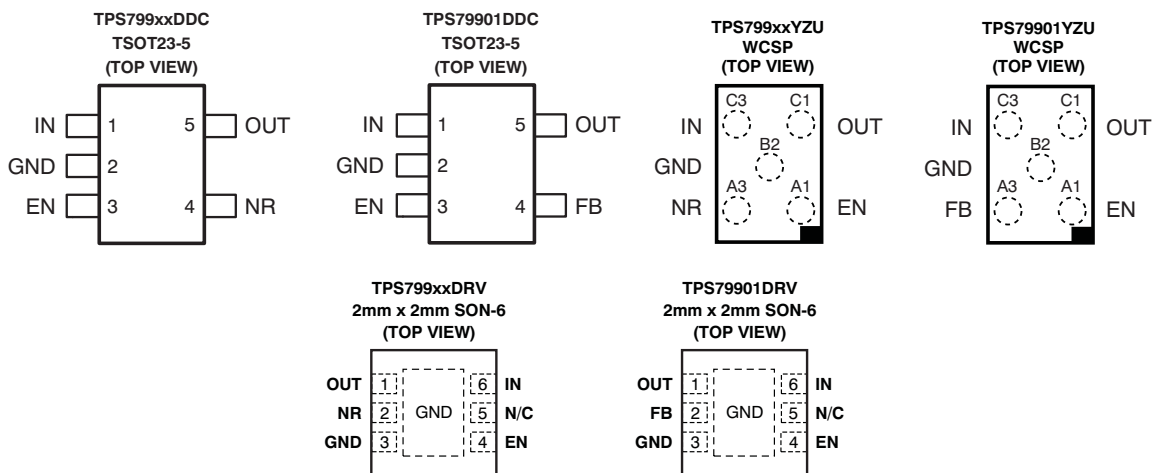
- 200mA Low Dropout Regulator with EN
- Low I_Q : 40 μ A
- Multiple Output Voltage Versions Available:
 - Fixed Outputs of 1.2V to 4.5V Using Innovative Factory EEPROM Programming
 - Adjustable Outputs from 1.20V to 6.5V
- High PSRR: 66dB at 1kHz
- Ultra-low Noise: 29.5 μ V_{RMS}
- Fast Start-Up Time: 45 μ s
- Stable with a Low-ESR, 2.0 μ F Typical Output Capacitance
- Excellent Load/Line Transient Response
- 2% Overall Accuracy (Load/Line/Temp)
- Very Low Dropout: 100mV
- ThinSOT-23, WCSP, and 2mm $\times$ 2mm SON-6 Packages

DESCRIPTION

The TPS799xx family of low-dropout (LDO) low-power linear regulators offer excellent AC performance with very low ground current. High power-supply rejection ratio (PSRR), low noise, fast start-up, and excellent line and load transient response are provided while consuming a very low 40 μ A (typical) ground current. The TPS799xx is stable with ceramic capacitors and uses an advanced BiCMOS fabrication process to yield dropout voltage typically 100mV at 200mA output. The TPS799xx uses a precision voltage reference and feedback loop to achieve overall accuracy of 2% over all load, line, process, and temperature variations. It is fully specified from $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$ and is offered in low profile ThinSOT23, Wafer Chip-Scale (WCSP), and 2mm $\times$ 2mm SON packages, ideal for wireless handsets and WLAN cards.

APPLICATIONS

- Cellular Phones
- Wireless LAN, Bluetooth®
- VCOs, RF
- Handheld Organizers, PDAs



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All other trademarks are the property of their respective owners.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

PRODUCT	V _{OUT} ⁽²⁾
TPS799xxyyyz	XX is nominal output voltage (for example, 28 = 2.8V, 285 = 2.85V, 01 = Adjustable). ⁽³⁾ YYY is package designator. Z is package quantity.

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (2) Output voltages from 1.2V to 4.5V in 50mV increments are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.
- (3) For fixed 1.2V operation, tie FB to OUT.

ABSOLUTE MAXIMUM RATINGS

Over operating temperature range (unless otherwise noted)⁽¹⁾

PARAMETER	TPS799xx	UNIT
V _{IN} range	–0.3 to +7.0	V
V _{EN} range	–0.3 to V _{IN} +0.3	V
V _{OUT} range	–0.3 to V _{IN} +0.3	V
Peak output current	Internally limited	
Continuous total power dissipation	See Dissipation Ratings Table	
Junction temperature range, T _J	–55 to +150	°C
Storage junction temperature range, T _{STG}	–55 to +150	°C
ESD rating, HBM	2	kV
ESD rating, CDM	500	V

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

DISSIPATION RATINGS

BOARD	PACKAGE	R _{θJC}	R _{θJA}	DERATING FACTOR ABOVE T _A = 25°C	T _A < 25°C	T _A = 70°C	T _A = 85°C
Low-K ⁽¹⁾	DDC	90°C/W	280°C/W	3.6mW/°C	360mW	200mW	145mW
High-K ⁽²⁾	DDC	90°C/W	200°C/W	5.0mW/°C	500mW	275mW	200mW
Low-K ⁽¹⁾	YZU	27°C/W	255°C/W	3.9mW/°C	390mW	215mW	155mW
High-K ⁽²⁾	YZU	27°C/W	190°C/W	5.3mW/°C	530mW	295mW	215mW
Low-K ⁽¹⁾	DRV	20°C/W	140°C/W	7.1mW/°C	715mW	395mW	285mW
High-K ⁽²⁾	DRV	20°C/W	65°C/W	15.4mW/°C	1540mW	845mW	615mW

- (1) The JEDEC low-K (1s) board used to derive this data was a 3in × 3in, two-layer board with 2-ounce copper traces on top of the board.
- (2) The JEDEC high-K (2s2p) board used to derive this data was a 3in × 3in, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

ELECTRICAL CHARACTERISTICS

Over operating temperature range ($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$), $V_{IN} = V_{OUT(TYP)} + 0.3\text{V}$ or 2.7V , whichever is greater; $I_{OUT} = 1\text{mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\mu\text{F}$, $C_{NR} = 0.01\mu\text{F}$, unless otherwise noted. For TPS79901, $V_{OUT} = 3.0\text{V}$. Typical values are at $T_J = +25^{\circ}\text{C}$.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range ⁽¹⁾			2.7		6.5	V
V_{FB}	Internal reference (TPS79901)			1.169	1.193	1.217	V
V_{OUT}	Output voltage range (TPS79901)			V_{FB}		$6.5 - V_{DO}$	V
V_{OUT}	Output accuracy	Nominal	$T_J = +25^{\circ}\text{C}$	-1.0		+1.0	%
V_{OUT}	Output accuracy ⁽¹⁾	Over V_{IN} , I_{OUT} , Temp	$V_{OUT} + 0.3\text{V} \leq V_{IN} \leq 6.5\text{V}$ $500\mu\text{A} \leq I_{OUT} \leq 200\text{mA}$	-2.0	± 1.0	+2.0	%
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation ⁽¹⁾		$V_{OUT(NOM)} + 0.3\text{V} \leq V_{IN} \leq 6.5\text{V}$		0.02		%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation		$500\mu\text{A} \leq I_{OUT} \leq 200\text{mA}$		0.002		%/mA
V_{DO}	Dropout voltage ⁽²⁾ ($V_{IN} = V_{OUT(NOM)} - 0.1\text{V}$)	$V_{OUT} < 3.3\text{V}$	$I_{OUT} = 200\text{mA}$		100	175	mV
V_{DO}	Dropout voltage ($V_{IN} = V_{OUT(NOM)} - 0.1\text{V}$)	$V_{OUT} \geq 3.3\text{V}$	$I_{OUT} = 200\text{mA}$		90	160	mV
I_{CL}	Output current limit		$V_{OUT} = 0.9 \times V_{OUT(NOM)}$	200	400	600	mA
I_{GND}	Ground pin current		$500\mu\text{A} \leq I_{OUT} \leq 200\text{mA}$		40	60	μA
I_{SHDN}	Shutdown current (I_{GND})		$V_{EN} \leq 0.4\text{V}$, $2.7\text{V} \leq V_{IN} \leq 6.5\text{V}$		0.15	1.0	μA
I_{FB}	Feedback pin current (TPS79901)			-0.5		0.5	μA
PSRR	Power-supply rejection ratio $V_{IN} = 3.85\text{V}$, $V_{OUT} = 2.85\text{V}$, $C_{NR} = 0.01\mu\text{F}$, $I_{OUT} = 100\text{mA}$		$f = 100\text{Hz}$		70		dB
			$f = 1\text{kHz}$		66		dB
			$f = 10\text{kHz}$		51		dB
			$f = 100\text{kHz}$		38		dB
V_N	Output noise voltage BW = 10Hz to 100kHz, $V_{OUT} = 2.8\text{V}$		$C_{NR} = 0.01\mu\text{F}$		$10.5 \times V_{OUT}$		μV_{RMS}
			$C_{NR} = \text{none}$		$94 \times V_{OUT}$		μV_{RMS}
T_{STR}	Startup time $V_{OUT} = 2.85\text{V}$, $R_L = 14\Omega$, $C_{OUT} = 2.2\mu\text{F}$		$C_{NR} = 0.001\mu\text{F}$		45		μs
			$C_{NR} = 0.047\mu\text{F}$		45		μs
			$C_{NR} = 0.01\mu\text{F}$		50		μs
			$C_{NR} = \text{none}$		50		μs
$V_{EN(HI)}$	Enable high (enabled)			1.2		V_{IN}	V
$V_{EN(LO)}$	Enable low (shutdown)			0		0.4	V
$I_{EN(HI)}$	Enable pin current, enabled		$V_{EN} = V_{IN} = 6.5\text{V}$		0.03	1.0	μA
TSD	Thermal shutdown temperature		Shutdown, temperature increasing		165		$^{\circ}\text{C}$
			Reset, temperature decreasing		145		$^{\circ}\text{C}$
T_J	Operating junction temperature			-40		+125	$^{\circ}\text{C}$
UVLO	Under-voltage lock-out		V_{IN} rising	1.90	2.20	2.65	V
	Hysteresis		V_{IN} falling		70		mV

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.7V , whichever is greater.

(2) V_{DO} is not measured for devices with $V_{OUT(NOM)} < 2.8\text{V}$ because minimum $V_{IN} = 2.7\text{V}$.

DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAMS

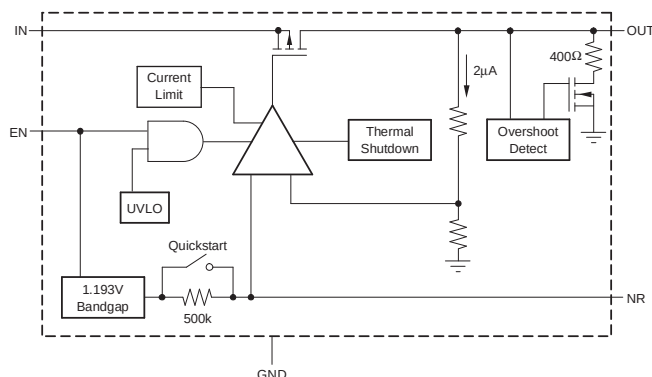


Figure 1. Fixed Voltage Versions

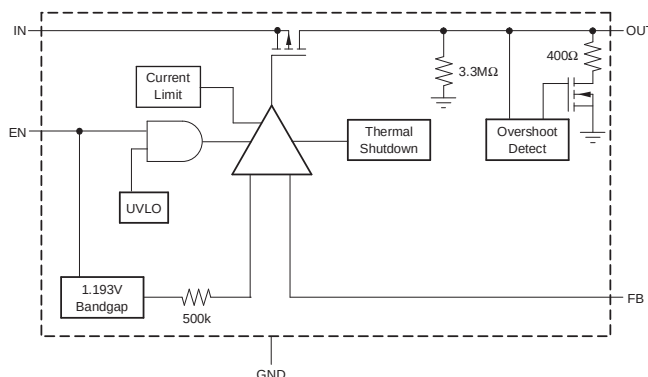


Figure 2. Adjustable Voltage Versions

PIN CONFIGURATIONS

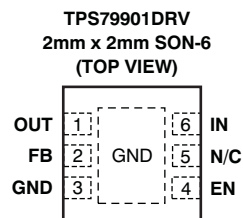
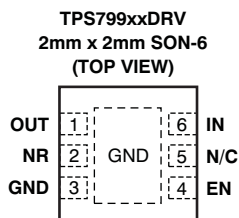
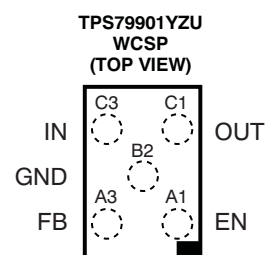
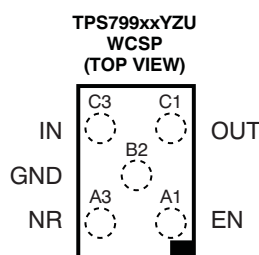
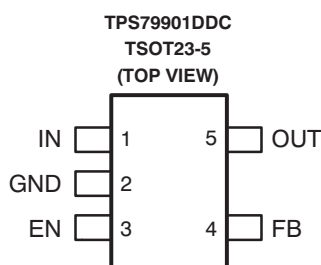
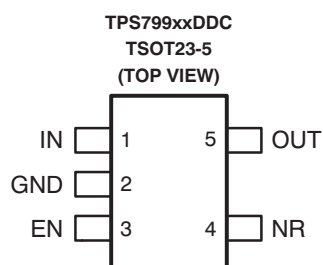


Table 1. PIN DESCRIPTIONS

TPS799xx				DESCRIPTION
NAME	DDC	YZU	DRV	
IN	1	C3	6	Input supply.
GND	2	B2	3, Pad	Ground. The pad must be tied to GND.
EN	3	A1	4	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
NR	4	A3	2	Fixed voltage versions only; connecting an external capacitor to this pin bypasses noise generated by the internal bandgap. This capacitor allows output noise to be reduced to very low levels.
FB	4	A3	2	Adjustable version only; this pin is the input to the control loop error amplifier, and is used to set the output voltage of the device.
OUT	5	C1	1	Output of the regulator. A small capacitor (total typical capacitance $\geq 2.0\mu\text{F}$ ceramic) is needed from this pin to ground to assure stability.
N/C	—	—	5	Not internally connected. This pin must either be left open, or tied to GND.

TYPICAL CHARACTERISTICS

Over operating temperature range ($T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$), $V_{IN} = V_{OUT(TYP)} + 0.3\text{V}$ or 2.7V , whichever is greater; $I_{OUT} = 1\text{mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\mu\text{F}$, $C_{NR} = 0.01\mu\text{F}$, unless otherwise noted. For TPS79901, $V_{OUT} = 3.0\text{V}$. Typical values are at $T_J = +25^\circ\text{C}$.

LOAD REGULATION

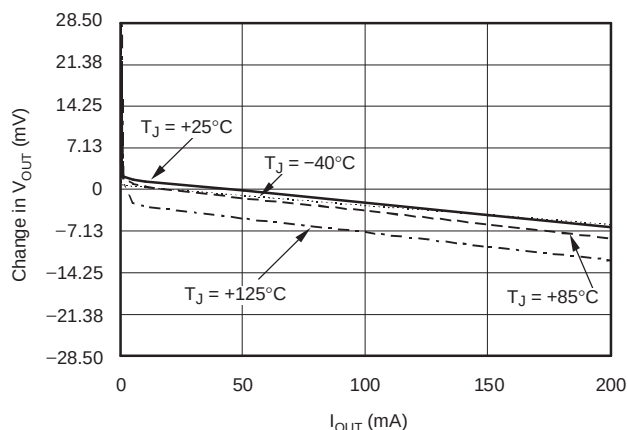


Figure 3.

LINE REGULATION

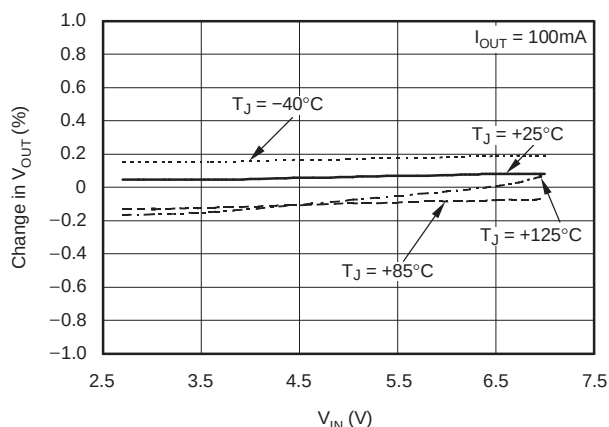


Figure 4.

OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

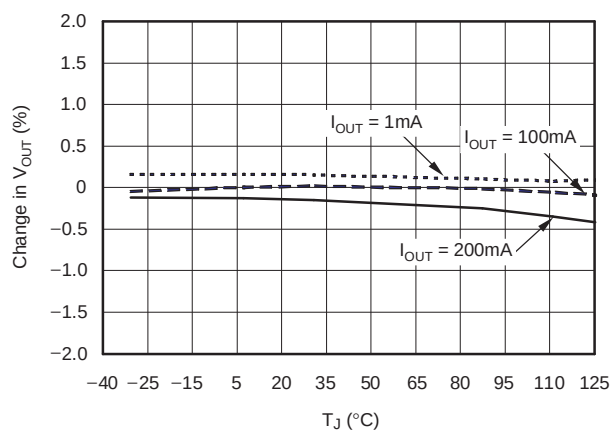


Figure 5.

TPS799285 DROPOUT VOLTAGE vs OUTPUT CURRENT

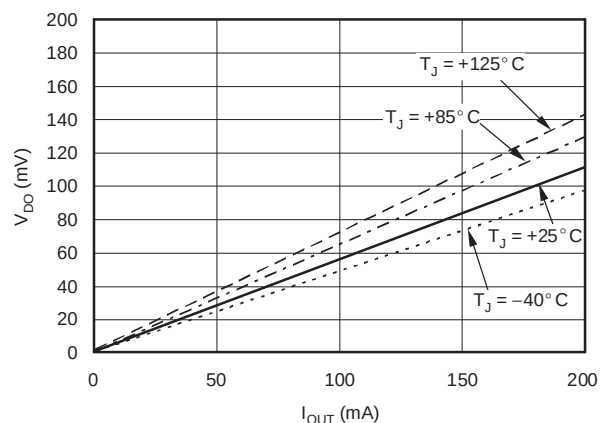


Figure 6.

TPS799285 DROPOUT VOLTAGE vs JUNCTION TEMPERATURE

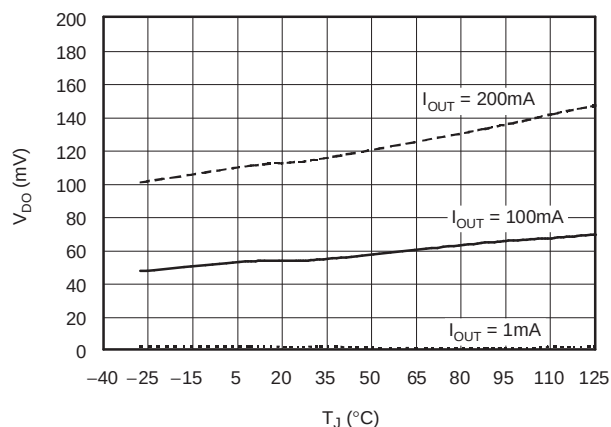


Figure 7.

TPS79901 DROPOUT vs INPUT VOLTAGE

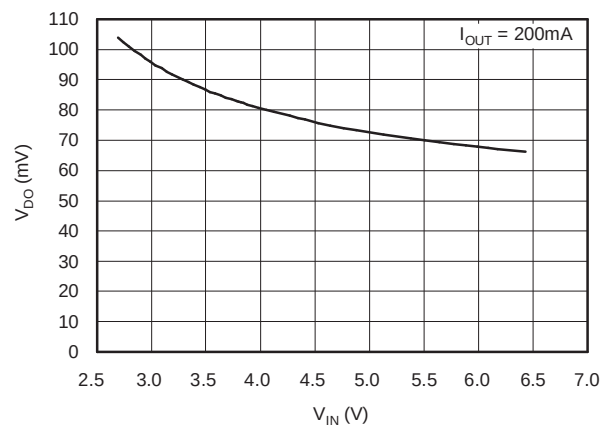
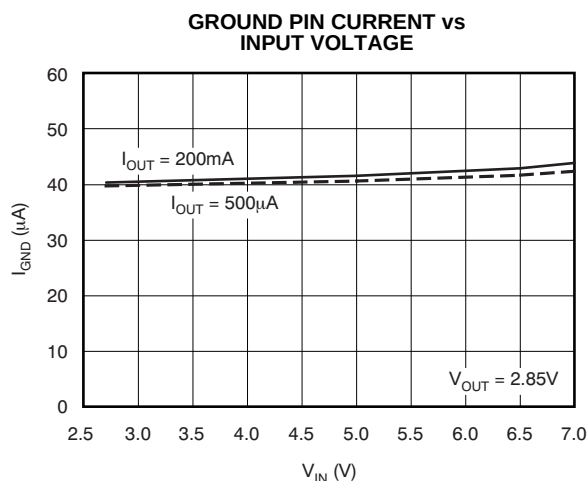
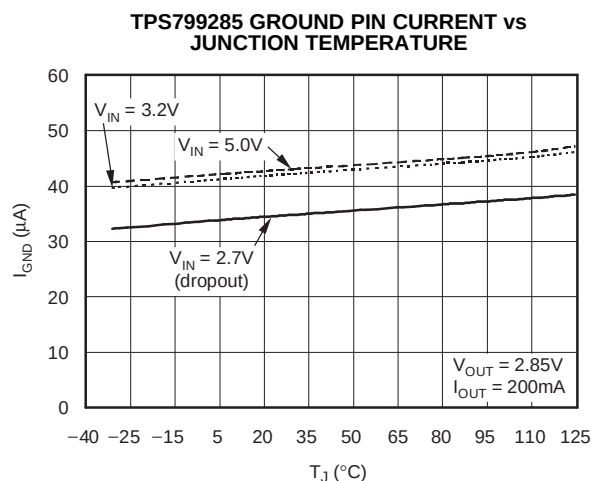
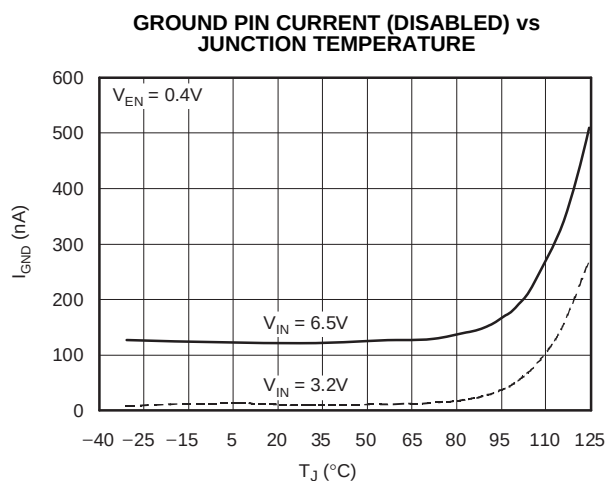
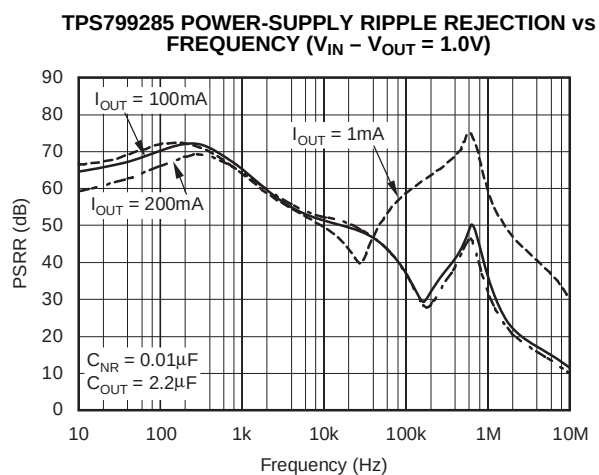


Figure 8.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range ($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$), $V_{IN} = V_{OUT(TYP)} + 0.3\text{V}$ or 2.7V , whichever is greater; $I_{OUT} = 1\text{mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\mu\text{F}$, $C_{NR} = 0.01\mu\text{F}$, unless otherwise noted. For TPS79901, $V_{OUT} = 3.0\text{V}$. Typical values are at $T_J = +25^{\circ}\text{C}$.

**Figure 9.****Figure 10.****Figure 11.****Figure 12.**

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range ($T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$), $V_{IN} = V_{OUT(TYP)} + 0.3\text{V}$ or 2.7V , whichever is greater; $I_{OUT} = 1\text{mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\mu\text{F}$, $C_{NR} = 0.01\mu\text{F}$, unless otherwise noted. For TPS79901, $V_{OUT} = 3.0\text{V}$. Typical values are at $T_J = +25^\circ\text{C}$.

TPS799285 POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY ($V_{IN} - V_{OUT} = 0.5\text{V}$)

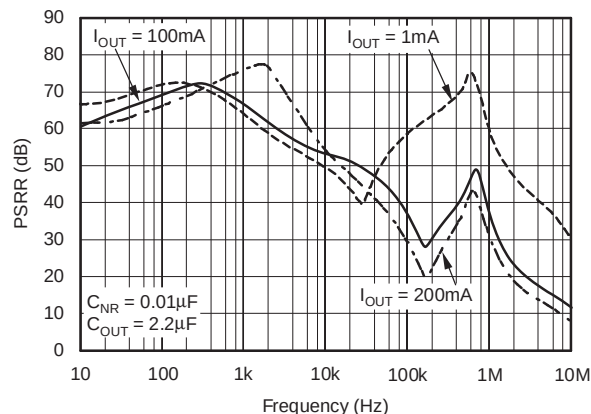


Figure 13.

TPS799285 POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY ($V_{IN} - V_{OUT} = 0.25\text{V}$)

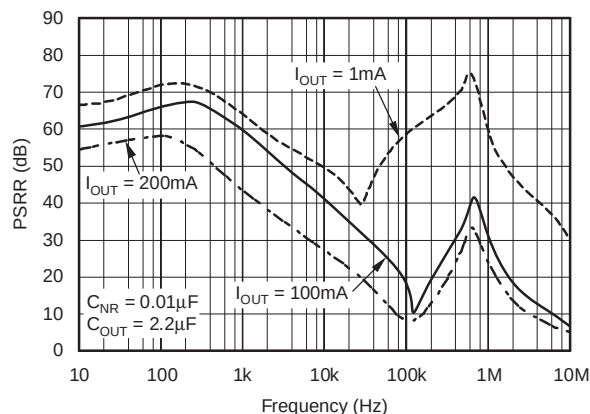


Figure 14.

TPS799285 POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY ($V_{IN} - V_{OUT} = 1.0\text{V}$)

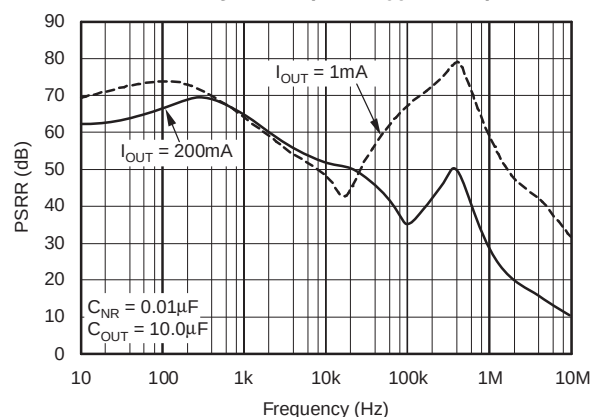


Figure 15.

TPS799285 POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY ($V_{IN} - V_{OUT} = 0.25\text{V}$)

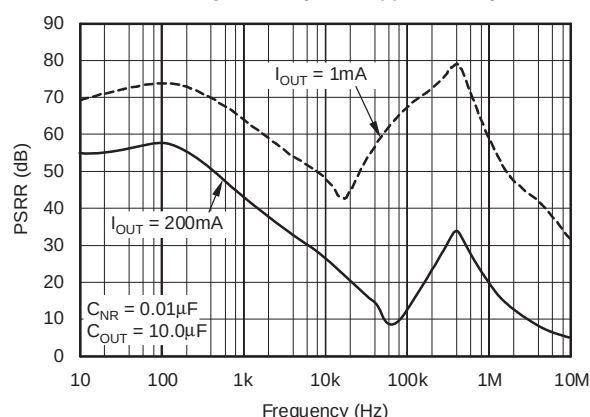


Figure 16.

TPS799285 POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY ($V_{IN} - V_{OUT} = 1.0\text{V}$)

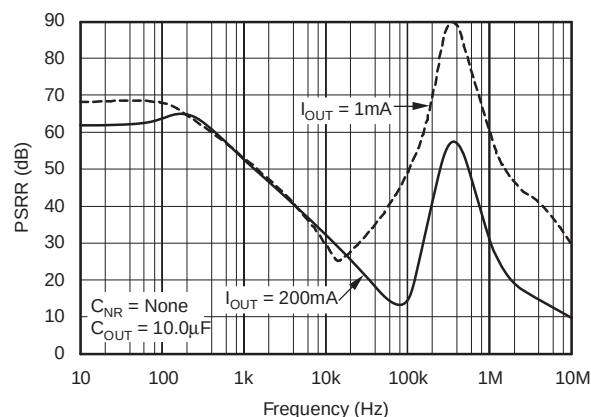


Figure 17.

POWER-SUPPLY RIPPLE REJECTION vs $V_{IN} - V_{OUT}$, $I_{OUT} = 1\text{mA}$

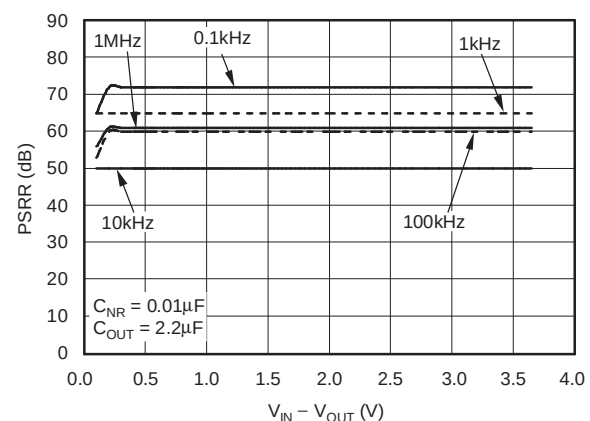


Figure 18.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range ($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$), $V_{IN} = V_{OUT(TYP)} + 0.3\text{V}$ or 2.7V , whichever is greater; $I_{OUT} = 1\text{mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\mu\text{F}$, $C_{NR} = 0.01\mu\text{F}$, unless otherwise noted. For TPS79901, $V_{OUT} = 3.0\text{V}$. Typical values are at $T_J = +25^{\circ}\text{C}$.

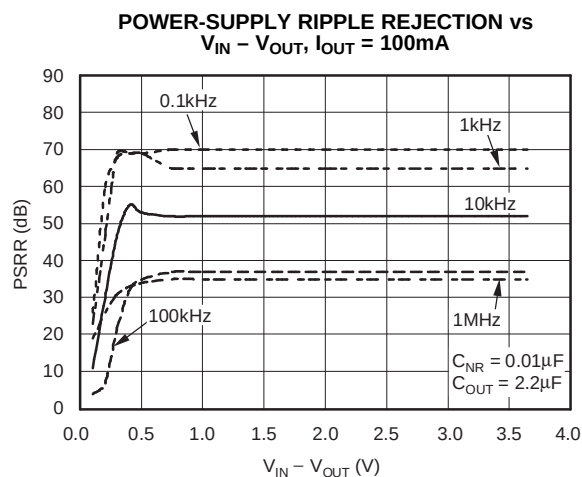


Figure 19.

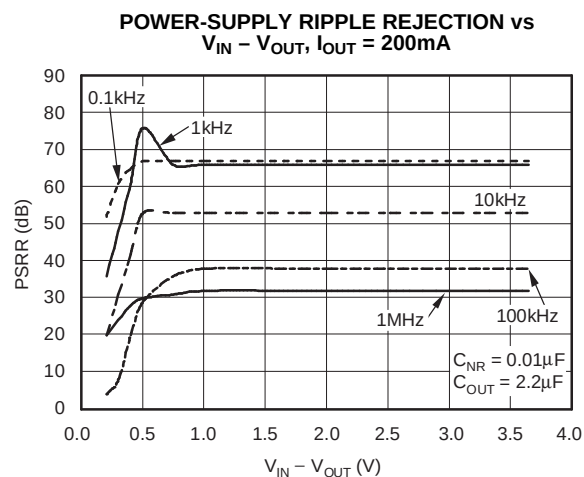


Figure 20.

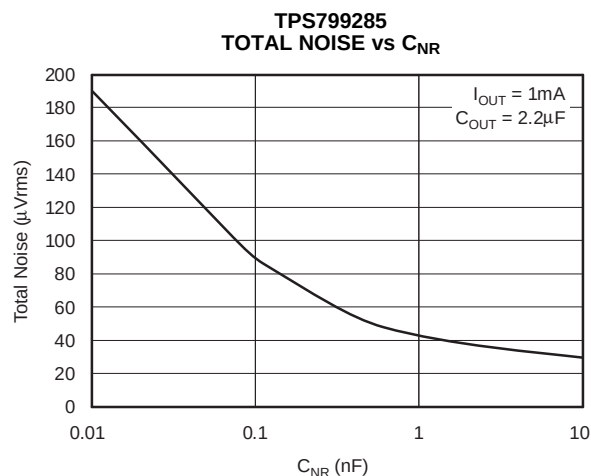


Figure 21.

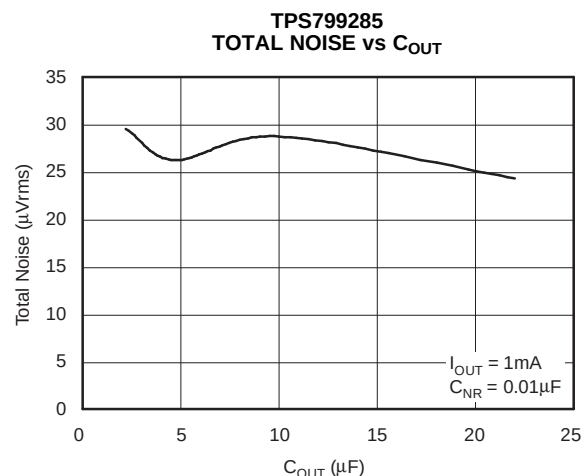


Figure 22.

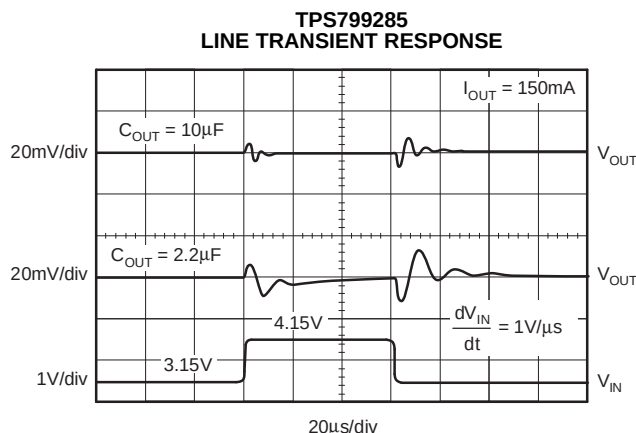


Figure 23.

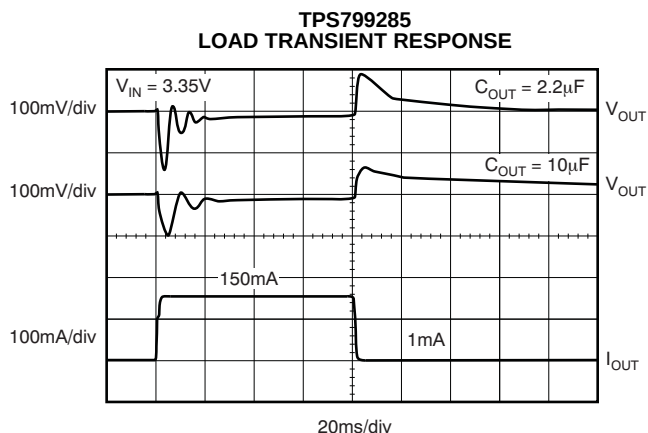


Figure 24.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range ($T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$), $V_{IN} = V_{OUT(TYP)} + 0.3\text{V}$ or 2.7V , whichever is greater; $I_{OUT} = 1\text{mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\mu\text{F}$, $C_{NR} = 0.01\mu\text{F}$, unless otherwise noted. For TPS79901, $V_{OUT} = 3.0\text{V}$. Typical values are at $T_J = +25^\circ\text{C}$.

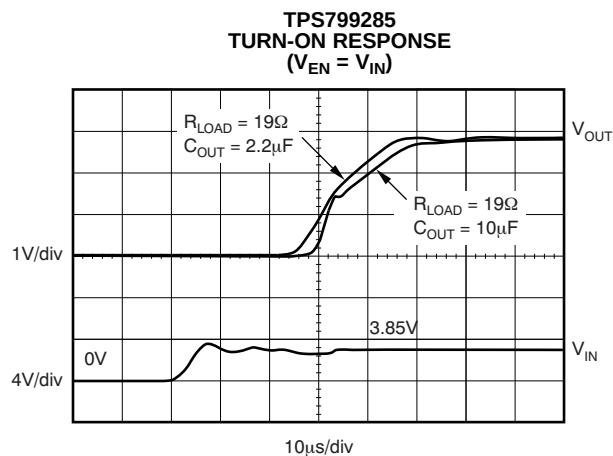


Figure 25.

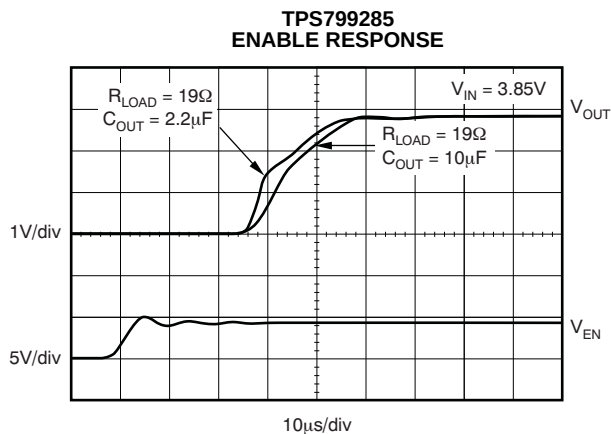


Figure 26.

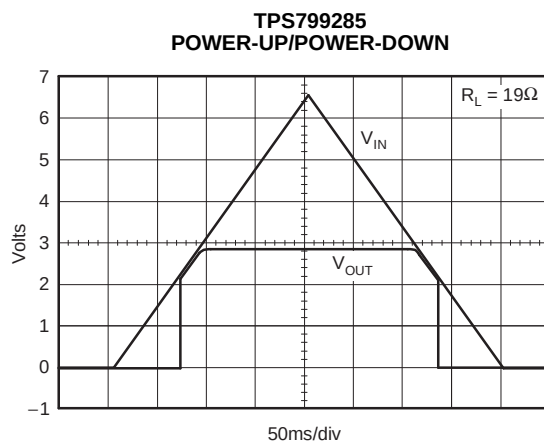


Figure 27.

APPLICATION INFORMATION

The TPS799xx family of LDO regulators combines the high performance required of many RF and precision analog applications with ultra-low current consumption. High PSRR is provided by a high gain, high bandwidth error loop with good supply rejection at very low headroom ($V_{IN} - V_{OUT}$). Fixed voltage versions provide a noise reduction pin to bypass noise generated by the bandgap reference and to improve PSRR while a quick-start circuit fast-charges this capacitor at startup. The combination of high performance and low ground current also make the TPS799xx an excellent choice for portable applications. All versions have thermal and over-current protection and are fully specified from -40°C to $+125^{\circ}\text{C}$.

Figure 28 shows the basic circuit connections for fixed voltage models. Figure 29 gives the connections for the adjustable output version (TPS79901). R_1 and R_2 can be calculated for any output voltage using the formula in Figure 29. Sample resistor values for common output voltages are shown in Figure 29.

Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a $0.1\mu\text{F}$ to $1\mu\text{F}$ low ESR capacitor across the input supply near the regulator. This will counteract reactive input sources and improve transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source. If source impedance is not sufficiently low, a $0.1\mu\text{F}$ input capacitor may be necessary to ensure stability.

The TPS799xx is designed to be stable with standard ceramic capacitors of values $2.2\mu\text{F}$ or larger. X5R and X7R type capacitors are best as they have minimal variation in value and ESR over temperature. Maximum ESR should be $< 1.0\Omega$.

Feedback Capacitor Requirements (TPS79901 only)

The feedback capacitor, C_{FB} , shown in Figure 29 is required for stability. For a parallel combination of R_1 and R_2 equal to $250\text{k}\Omega$, any value from 3pF to 1nF can be used. Fixed voltage versions have an internal 30pF feedback capacitor which is quick-charged at start-up. The adjustable version does not have this quick-charge circuit, so values below 5pF should be used to ensure fast startup; values above 47pF can be used to implement an output voltage soft-start. Larger value capacitors also improve noise slightly. The TPS79901 is stable in unity-gain configuration (OUT tied to FB) without C_{FB} .

Output Noise

In most LDOs, the bandgap is the dominant noise source. If a noise reduction capacitor (C_{NR}) is used with the TPS799xx, the bandgap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a $0.01\mu\text{F}$ noise reduction capacitor; for the adjustable version, smaller value resistors in the output resistor divider reduce noise. A parallel combination that gives $2\mu\text{A}$ of divider current will have the same noise performance as a fixed voltage version. To further optimize noise, equivalent series resistance of the output capacitor can be set to approximately 0.2Ω . This configuration maximizes phase margin in the control loop, reducing total output noise by up to 10%.

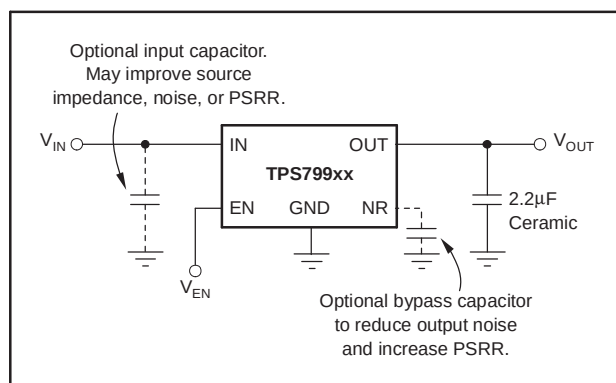


Figure 28. Typical Application Circuit for Fixed Voltage Versions

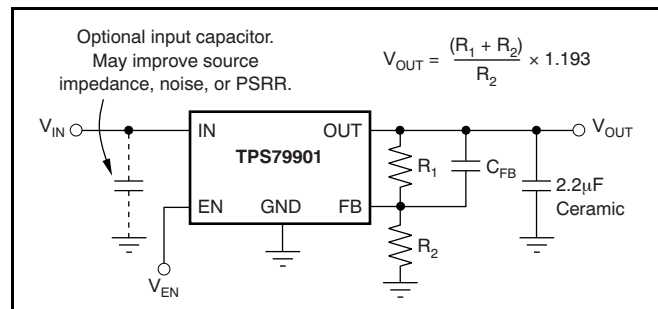


Figure 29. Typical Application Circuit for Adjustable Voltage Version

Noise can be referred to the feedback point (FB pin) such that with $C_{NR} = 0.01\mu\text{F}$ total noise is approximately given by [Equation 1](#):

$$V_N = \frac{10.5\mu\text{V}_{\text{RMS}}}{V} \times V_{\text{OUT}} \quad (1)$$

The TPS79901 adjustable version does not have the noise-reduction pin available, so ultra-low noise operation is not possible. Noise can be minimized according to the above recommendations.

Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT} , with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

Internal Current Limit

The TPS799xx internal current limit helps protect the regulator during fault conditions. During current limit, the output will source a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in current limit for extended periods of time.

The PMOS pass element in the TPS799xx has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

Shutdown

The enable pin (EN) is active high and is compatible with standard and low voltage TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

Dropout Voltage

The TPS799xx uses a PMOS pass transistor to achieve low dropout. When $(V_{\text{IN}} - V_{\text{OUT}})$ is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{\text{DS, ON}}$ of the PMOS pass element. Because the PMOS device behaves like a resistor in dropout, V_{DO} will approximately scale with output current.

As with any linear regulator, PSRR and transient response are degraded as $(V_{\text{IN}} - V_{\text{OUT}})$ approaches dropout. This effect is shown in [Figure 18](#) through [Figure 20](#) in the *Typical Characteristics* section.

Startup

Fixed voltage versions of the TPS799xx use a quick-start circuit to fast-charge the noise reduction capacitor, C_{NR} , if present (see *Functional Block Diagrams*, [Figure 1](#)). This allows the combination of very low output noise and fast start-up times. The NR pin is high impedance so a low leakage C_{NR} capacitor must be used; most ceramic capacitors are appropriate in this configuration.

Note that for fastest startup, V_{IN} should be applied first, then the enable pin (EN) driven high. If EN is tied to IN, startup will be somewhat slower. Refer to [Figure 25](#) and [Figure 26](#) in the *Typical Characteristics* section. The quick-start switch is closed for approximately 135 μs . To ensure that C_{NR} is fully charged during the quick-start time, a 0.01 μF or smaller capacitor should be used.

Transient Response

As with any regulator, increasing the size of the output capacitor will reduce over/undershoot magnitude but increase duration of the transient response. In the adjustable version, adding C_{FB} between OUT and FB will improve stability and transient response. The transient response of the TPS799xx is enhanced by an active pull-down that engages when the output overshoots by approximately 5% or more when the device is enabled. When enabled, the pull-down device behaves like a 350 Ω resistor to ground.

Under-Voltage Lock-Out (UVLO)

The TPS799xx utilizes an under-voltage lock-out circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has a de-glitch feature so that it will typically ignore undershoot transients on the input if they are less than 50 μs duration.

Minimum Load

The TPS799xx is stable and well-behaved with no output load. To meet the specified accuracy, a minimum load of 500 μA is required. Below 500 μA at junction temperatures near +125°C, the output can drift up enough to cause the output pull-down to turn on. The output pull-down will limit voltage drift to 5% typically but ground current could increase by approximately 50 μA . In typical applications, the junction cannot reach high temperatures at light loads since there is no appreciable dissipated power. The specified ground current would then be valid at no load in most applications.

Thermal Information

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +165°C, allowing the device to cool. When the junction temperature cools to approximately +145°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS799xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS799xx into thermal shutdown will degrade device reliability.

Power Dissipation

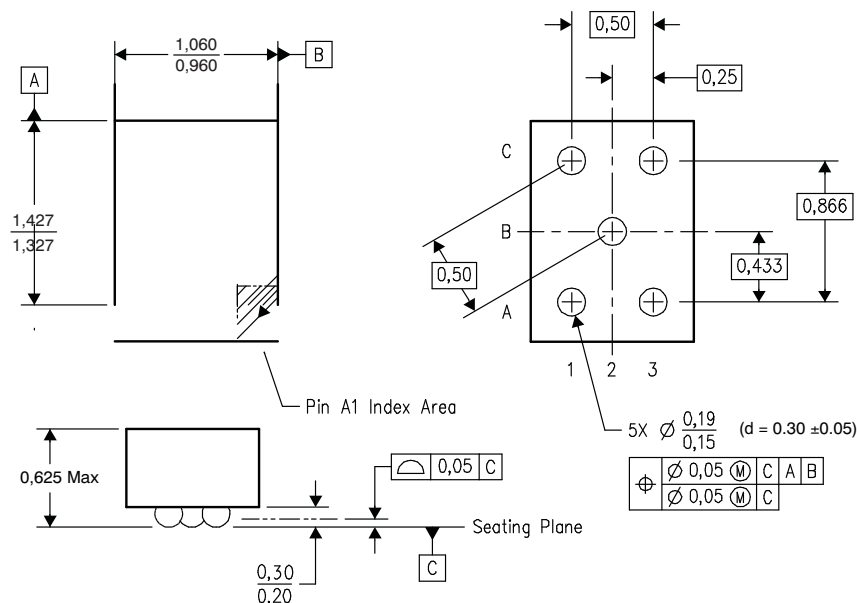
The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Dissipation Ratings* table. Using heavier copper will increase the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers will also improve the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current times the voltage drop across the output pass element, as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT} \quad (2)$$

Package Mounting

Solder pad footprint recommendations for the TPS799xx are available from the Texas Instruments' web site at www.ti.com.



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.

NanoStar is a trademark of Texas Instruments.

Figure 30. YZU Wafer Chip-Scale Package Dimensions (in mm)

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPS79901DDCR	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79901DDCRG4	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79901DDCT	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79901DDCTG4	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79901DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79901DRVRG4	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79901DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79901DRVTG4	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79901YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79901YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79912DDCR	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79912DDCT	ACTIVE	TO/SOT	DDC	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79912YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79912YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79913DDCR	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79913DDCRG4	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79913DDCT	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79913DDCTG4	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79913YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79913YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79915DDCR	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79915DDCRG4	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79915DDCT	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79915DDCTG4	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79915YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPS79915YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79918DDCR	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79918DDCRG4	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79918DDCT	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79918DDCTG4	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79918DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79918DRVRG4	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79918DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79918DRVTG4	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79918YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79918YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS799195DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS799195DRVRG4	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS799195DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS799195DRVTG4	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79919YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79919YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79920YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79920YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79925DDCR	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79925DDCRG4	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79925DDCT	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79925DDCTG4	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79925YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79925YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79926YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPS79926YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS799275YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS799275YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79927DDCR	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79927DDCRG4	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79927DDCT	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79927DDCTG4	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79927DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79927DRVRG4	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79927DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79927DRVTG4	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79927YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79927YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS799285DDCR	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS799285DDCRG4	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS799285DDCT	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS799285DDCTG4	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS799285DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS799285DRVRG4	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS799285DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS799285DRVTG4	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS799285YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS799285YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79928DDCR	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79928DDCRG4	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79928DDCT	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPS79928DDCTG4	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79928DRV	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79928DRVRG4	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79928DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79928DRVTG4	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79928YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79928YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79930DDCR	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79930DDCRG4	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79930DDCT	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79930DDCTG4	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79930YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79930YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79932YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79932YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79933DDCR	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79933DDCRG4	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79933DDCT	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79933DDCTG4	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79933DRV	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79933DRVRG4	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79933DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79933DRVTG4	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79933YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79933YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79942DDCR	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPS79942DDCT	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79945YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79945YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

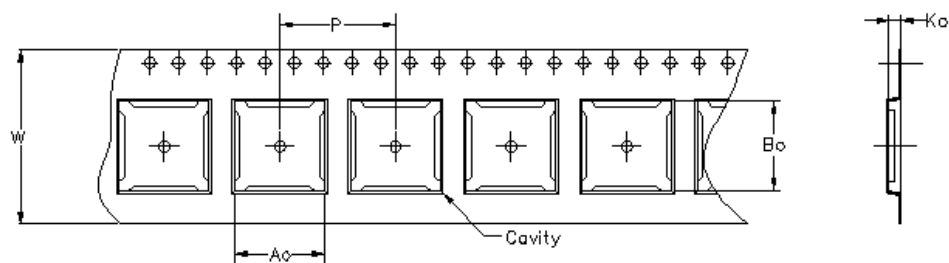
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

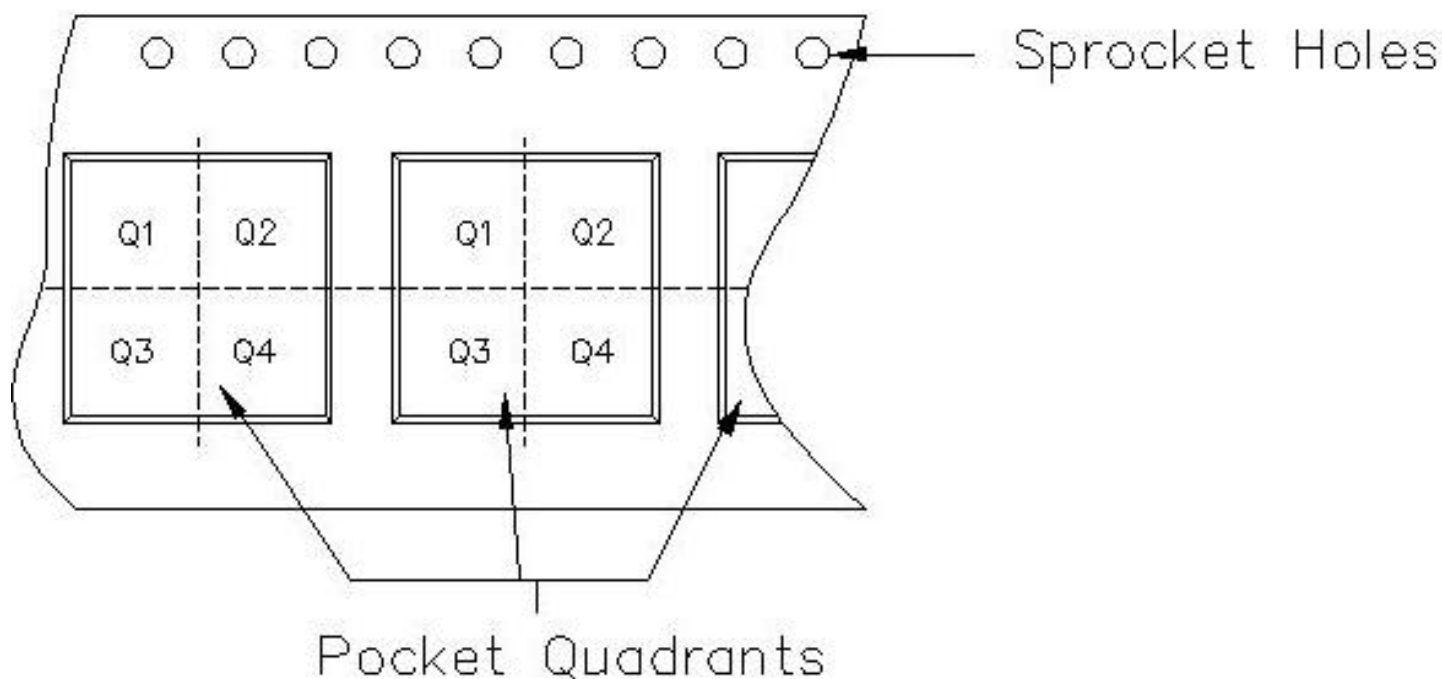
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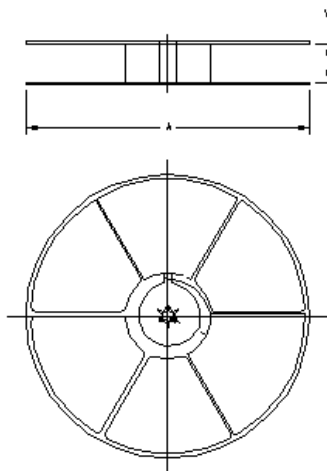
Carrier tape design is defined largely by the component length, width, and thickness.

A_0 = Dimension designed to accommodate the component width.
B_0 = Dimension designed to accommodate the component length.
K_0 = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



TAPE AND REEL INFORMATION

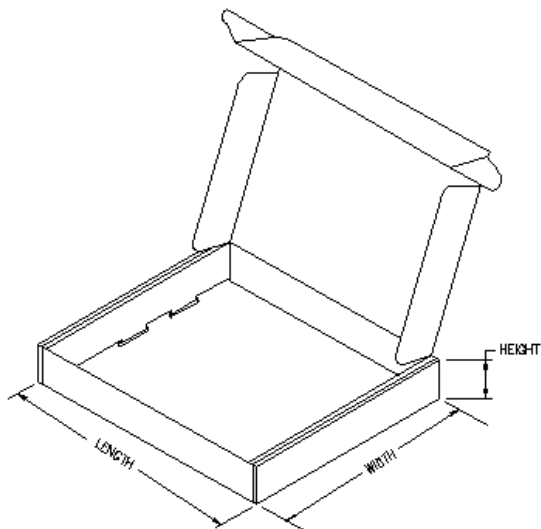
Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79901DDCR	DDC	5	NSE	177	8	3.2	3.2	1.4	4	8	NONE
TPS79901DDCT	DDC	5	NSE	177	8	3.2	3.2	1.4	4	8	NONE
TPS79901DRVR	DRV	6	NSE	177	8	2.2	2.2	1.2	4	8	Q2
TPS79901DRVT	DRV	6	NSE	177	8	2.2	2.2	1.2	4	8	Q2
TPS79901YZUR	YZU	5	FUJIKAT	180	11	1.07	1.52	0.72	4	8	Q1
TPS79901YZUT	YZU	5	FUJIKAT	180	11	1.07	1.52	0.72	4	8	Q1
TPS79912DDCR	DDC	5	NSE	177	8	3.2	3.2	1.4	4	8	Q3
TPS79912DDCT	DDC	6	NSE	177	8	3.2	3.2	1.4	4	8	Q3
TPS79913DDCR	DDC	5	NSE	177	8	3.2	3.2	1.4	4	8	NONE
TPS79913DDCT	DDC	5	NSE	177	8	3.2	3.2	1.4	4	8	NONE
TPS79913YZUR	YZU	5	FUJIKAT	180	11	1.07	1.52	0.72	4	8	Q1
TPS79913YZUT	YZU	5	FUJIKAT	180	11	1.07	1.52	0.72	4	8	Q1
TPS79915DDCR	DDC	5	NSE	177	8	3.2	3.2	1.4	4	8	NONE
TPS79915DDCT	DDC	5	NSE	177	8	3.2	3.2	1.4	4	8	NONE
TPS79918DDCR	DDC	5	NSE	177	8	3.2	3.2	1.4	4	8	NONE
TPS79918DDCT	DDC	5	NSE	177	8	3.2	3.2	1.4	4	8	NONE
TPS79918DRVR	DRV	6	NSE	177	8	2.2	2.2	1.2	4	8	Q2
TPS79918DRVT	DRV	6	NSE	177	8	2.2	2.2	1.2	4	8	Q2
TPS799195DRVR	DRV	6	NSE	177	8	2.2	2.2	1.2	4	8	Q2
TPS799195DRVT	DRV	6	NSE	177	8	2.2	2.2	1.2	4	8	Q2
TPS79925DDCR	DDC	5	NSE	177	8	3.2	3.2	1.4	4	8	NONE
TPS79925DDCT	DDC	5	NSE	177	8	3.2	3.2	1.4	4	8	NONE
TPS79927DDCR	DDC	5	NSE	177	8	3.2	3.2	1.4	4	8	NONE
TPS79927DDCT	DDC	5	NSE	177	8	3.2	3.2	1.4	4	8	NONE
TPS79927DRVR	DRV	6	NSE	177	8	2.2	2.2	1.2	4	8	Q2
TPS79927DRVT	DRV	6	NSE	177	8	2.2	2.2	1.2	4	8	Q2
TPS799285DDCR	DDC	5	NSE	177	8	3.2	3.2	1.4	4	8	NONE
TPS799285DDCT	DDC	5	NSE	177	8	3.2	3.2	1.4	4	8	NONE
TPS799285DRVR	DRV	6	NSE	177	8	2.2	2.2	1.2	4	8	Q2
TPS799285DRVT	DRV	6	NSE	177	8	2.2	2.2	1.2	4	8	Q2
TPS79928DDCR	DDC	5	NSE	177	8	3.2	3.2	1.4	4	8	NONE
TPS79928DDCT	DDC	5	NSE	177	8	3.2	3.2	1.4	4	8	NONE
TPS79928DRVR	DRV	6	NSE	177	8	2.2	2.2	1.2	4	8	Q2
TPS79928DRVT	DRV	6	NSE	177	8	2.2	2.2	1.2	4	8	Q2
TPS79930DDCR	DDC	5	NSE	177	8	3.2	3.2	1.4	4	8	NONE
TPS79930DDCT	DDC	5	NSE	177	8	3.2	3.2	1.4	4	8	NONE
TPS79933DDCR	DDC	5	NSE	177	8	3.2	3.2	1.4	4	8	NONE
TPS79933DDCT	DDC	5	NSE	177	8	3.2	3.2	1.4	4	8	NONE
TPS79933DRVR	DRV	6	NSE	177	8	2.2	2.2	1.2	4	8	Q2
TPS79933DRVT	DRV	6	NSE	177	8	2.2	2.2	1.2	4	8	Q2
TPS79942DDCR	DDC	5	NSE	177	8	3.2	3.2	1.4	4	8	Q3
TPS79942DDCT	DDC	5	NSE	177	8	3.2	3.2	1.4	4	8	Q3



TAPE AND REEL BOX INFORMATION

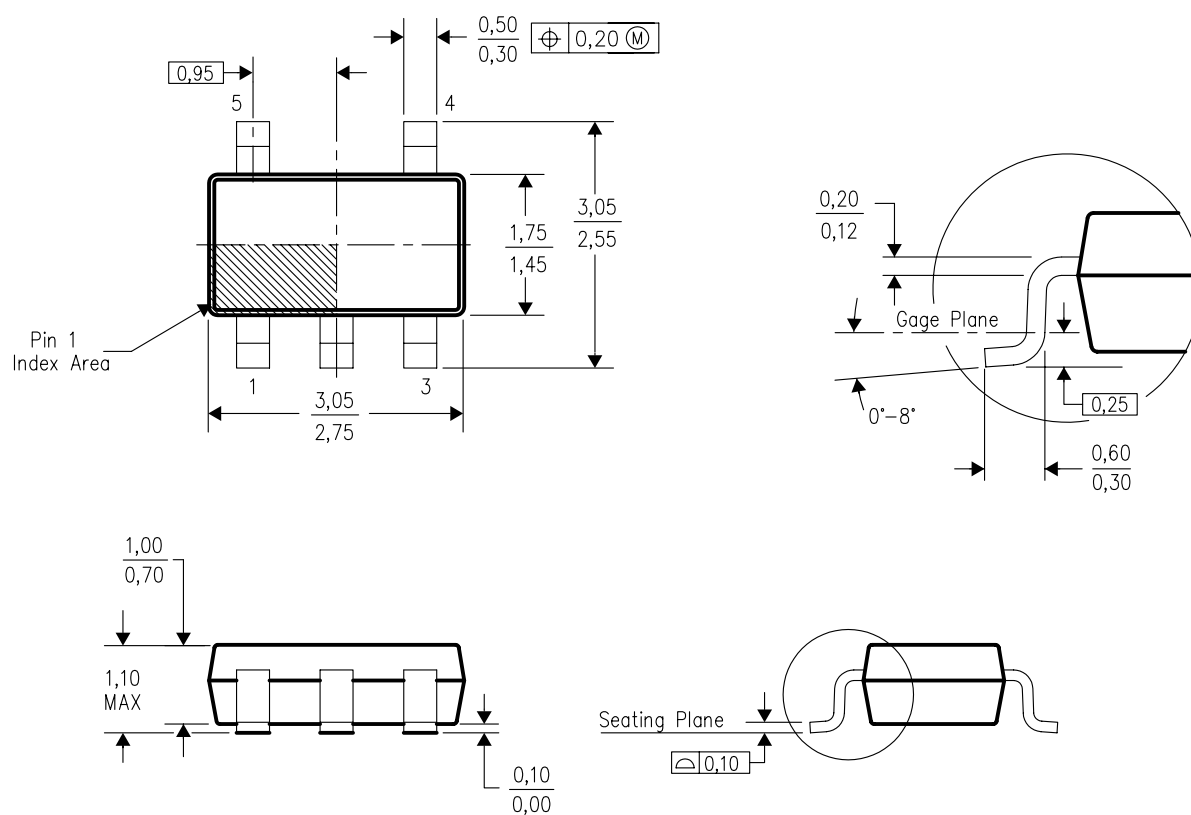
Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TPS79901DDCR	DDC	5	NSE	195.0	200.0	45.0
TPS79901DDCT	DDC	5	NSE	195.0	200.0	45.0
TPS79901DRVR	DRV	6	NSE	195.0	200.0	45.0
TPS79901DRVVT	DRV	6	NSE	195.0	200.0	45.0
TPS79901YZUR	YZU	5	FUJIKAT	195.0	190.0	95.0
TPS79901YZUT	YZU	5	FUJIKAT	195.0	190.0	95.0
TPS79912DDCR	DDC	5	NSE	195.0	200.0	45.0
TPS79912DDCT	DDC	6	NSE	195.0	200.0	45.0
TPS79913DDCR	DDC	5	NSE	195.0	200.0	45.0
TPS79913DDCT	DDC	5	NSE	195.0	200.0	45.0
TPS79913YZUR	YZU	5	FUJIKAT	195.0	190.0	95.0
TPS79913YZUT	YZU	5	FUJIKAT	195.0	190.0	95.0
TPS79915DDCR	DDC	5	NSE	195.0	200.0	45.0
TPS79915DDCT	DDC	5	NSE	195.0	200.0	45.0
TPS79918DDCR	DDC	5	NSE	195.0	200.0	45.0
TPS79918DDCT	DDC	5	NSE	195.0	200.0	45.0
TPS79918DRVR	DRV	6	NSE	195.0	200.0	45.0
TPS79918DRVVT	DRV	6	NSE	195.0	200.0	45.0
TPS799195DRVR	DRV	6	NSE	195.0	200.0	45.0
TPS799195DRVVT	DRV	6	NSE	195.0	200.0	45.0
TPS79925DDCR	DDC	5	NSE	195.0	200.0	45.0
TPS79925DDCT	DDC	5	NSE	195.0	200.0	45.0
TPS79927DDCR	DDC	5	NSE	195.0	200.0	45.0
TPS79927DDCT	DDC	5	NSE	195.0	200.0	45.0

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TPS79927DRVR	DRV	6	NSE	195.0	200.0	45.0
TPS79927DRVT	DRV	6	NSE	195.0	200.0	45.0
TPS799285DDCR	DDC	5	NSE	195.0	200.0	45.0
TPS799285DDCT	DDC	5	NSE	195.0	200.0	45.0
TPS799285DRVR	DRV	6	NSE	195.0	200.0	45.0
TPS799285DRVT	DRV	6	NSE	195.0	200.0	45.0
TPS79928DDCR	DDC	5	NSE	195.0	200.0	45.0
TPS79928DDCT	DDC	5	NSE	195.0	200.0	45.0
TPS79928DRVR	DRV	6	NSE	195.0	200.0	45.0
TPS79928DRVT	DRV	6	NSE	195.0	200.0	45.0
TPS79930DDCR	DDC	5	NSE	195.0	200.0	45.0
TPS79930DDCT	DDC	5	NSE	195.0	200.0	45.0
TPS79933DDCR	DDC	5	NSE	195.0	200.0	45.0
TPS79933DDCT	DDC	5	NSE	195.0	200.0	45.0
TPS79933DRVR	DRV	6	NSE	195.0	200.0	45.0
TPS79933DRVT	DRV	6	NSE	195.0	200.0	45.0
TPS79942DDCR	DDC	5	NSE	195.0	200.0	45.0
TPS79942DDCT	DDC	5	NSE	195.0	200.0	45.0



DDC (R-PDSO-G5)

PLASTIC SMALL-OUTLINE

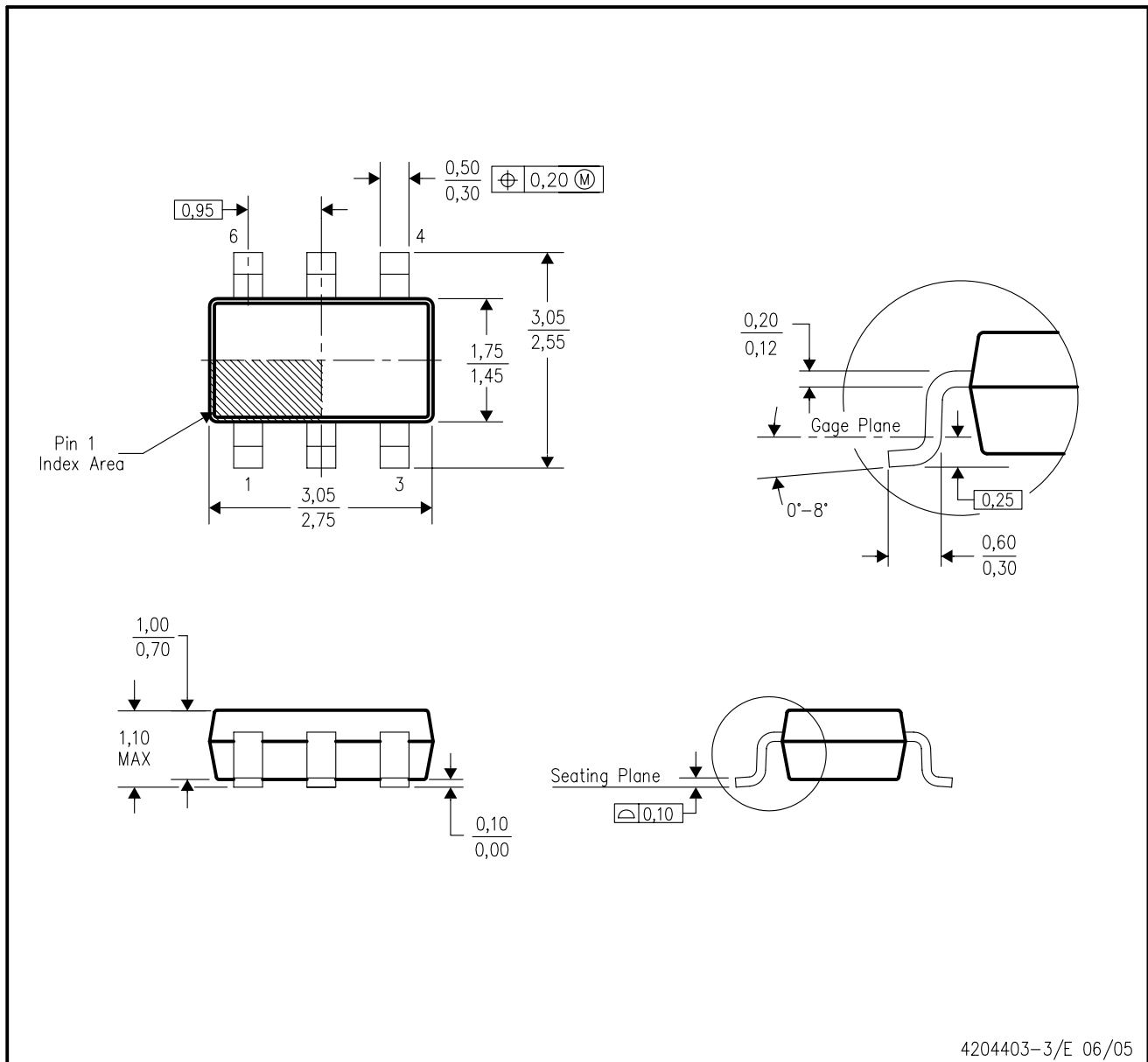


4204403-2/E 06/05

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-193 variation AB (5 pin).

DDC (R-PDSO-G6)

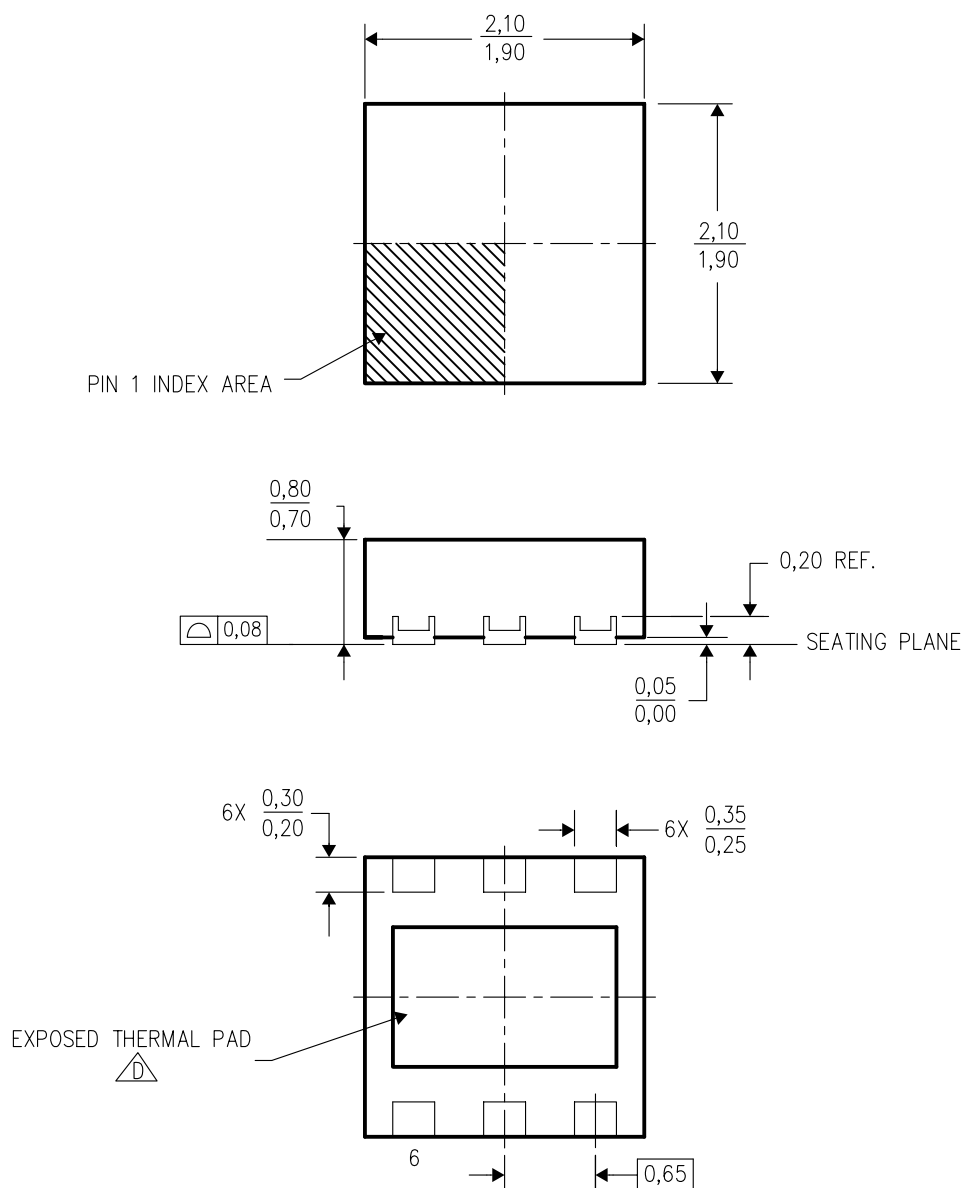
PLASTIC SMALL-OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - Falls within JEDEC MO-193 variation AA (6 pin).

DRV (S-PDSO-N6)

PLASTIC SMALL OUTLINE



4206925/C 01/07

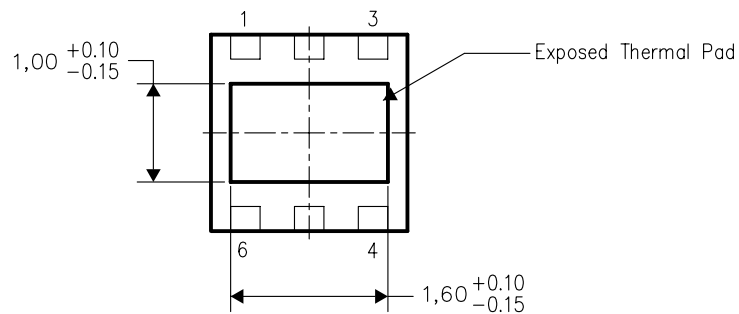
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Small Outline No-Lead (SON) package configuration.
 -  D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

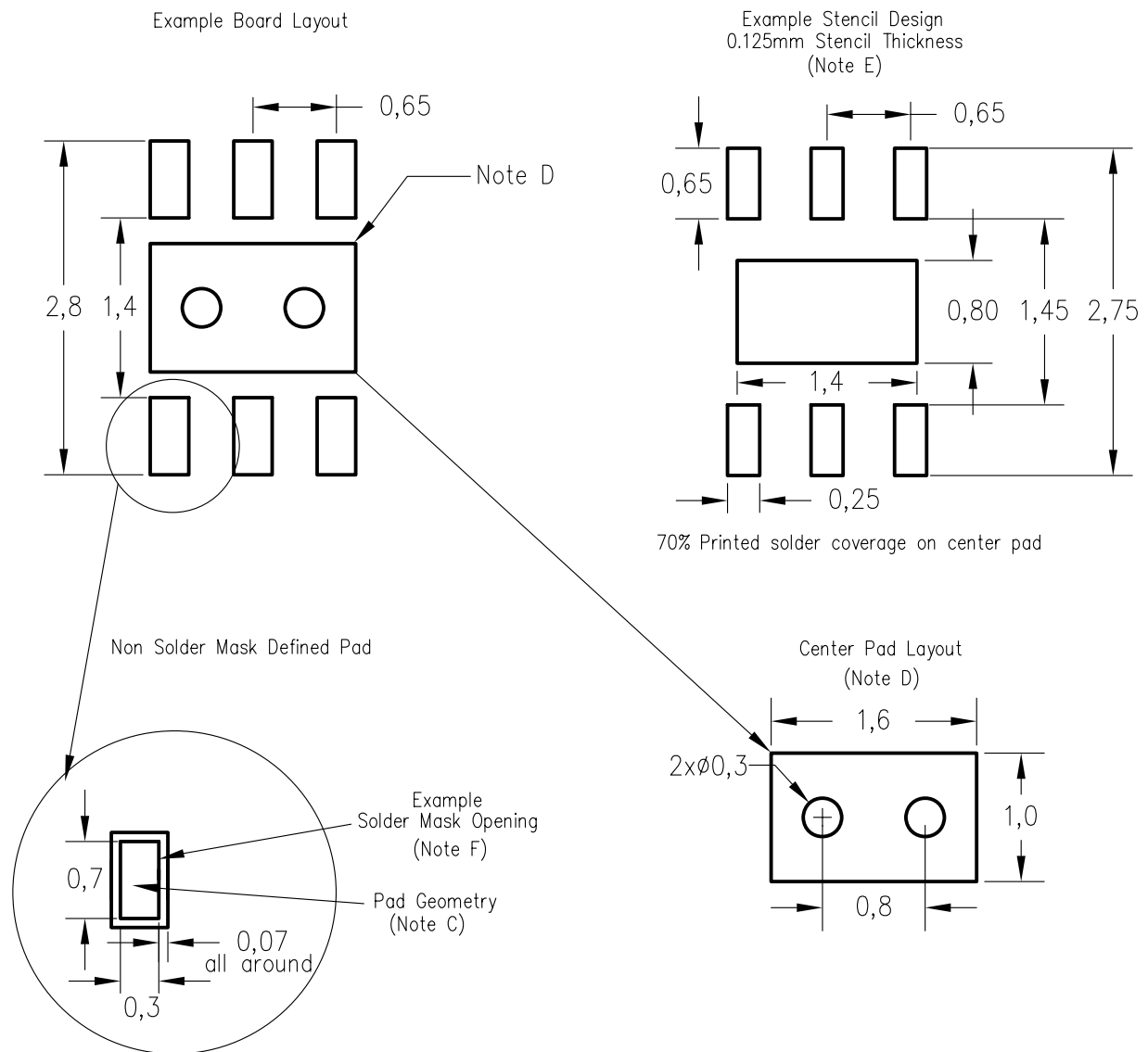


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRV (S-PDSO-N6)

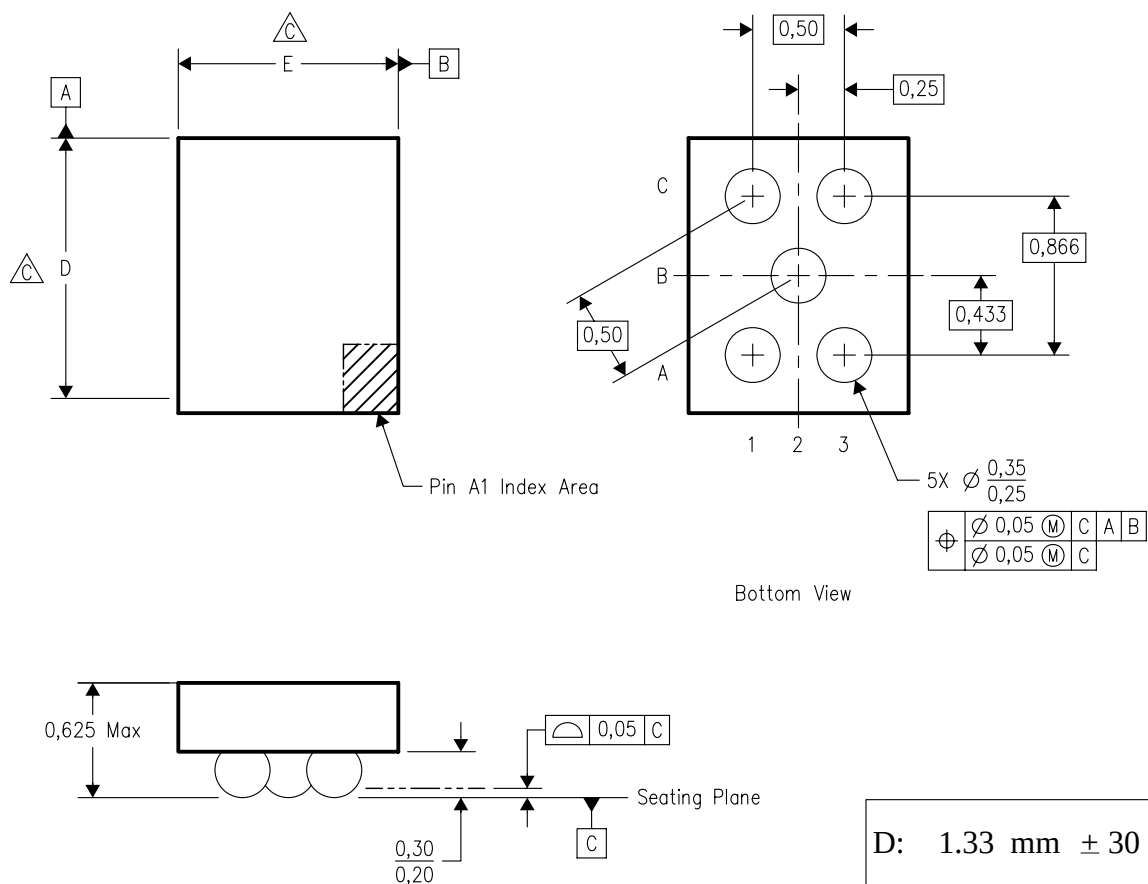


4207812/A 03/06

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for solder mask tolerances.

YZU (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



4205678/C 03/2007

- Notes:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Devices in this YZQ package can have dimension D ranging from 1.25 to 1.75 and dimension E ranging from 0.95 to 1.45. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
 - D. NanoFree™ package configuration.
 - E. This package contains lead-free balls. Refer to the 5 YEU package (drawing 4205430) for tin-lead (SnPb) balls.

NanoFree is a trademark of Texas Instruments.

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