FLASH-ROM MODULE 12MByte (3M x 32-Bit) ,72pin-SIMM, 3.3V
Part No. HMF3M32M6V

GENERAL DESCRIPTION

The HMF3M32M6VA is a high-speed flash read only memory (FROM) module containing 6,291,456 words organized in a x32bit configuration. The module consists of six 1M x 16 FROM mounted on a 72-pin, single-sided, FR4-printed circuit board. Commands are written to the command register using standard microprocessor write timings.
Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other flash or EPROM devices.
Output enable (/OE) and write enable (/WE) can set the memory input and output.
When FROM module is disable condition the module is becoming power standby mode, system designer can get low-power design. All module components may be powered from a single +3.0V DC power supply.

FEATURES

- Access time : 70,80, 90 and 120ns
- High-density 12MByte design
- High-reliability, low-power design
- Single + 3V ± 0.3V power supply
- Easy memory expansion
- Hardware reset pin(RESET#)
- FR4-PCB design
- Low profile 72-pin SIMM
- Minimum 1,000,000 write/erase cycle
- Flexible sector architecture
- Embedded algorithms
- Erase suspend / Erase resume

OPTIONS MARKING

- Timing

70ns access	-70
80ns access	-80
90ns access	-90
120ns access	-120

- Packages

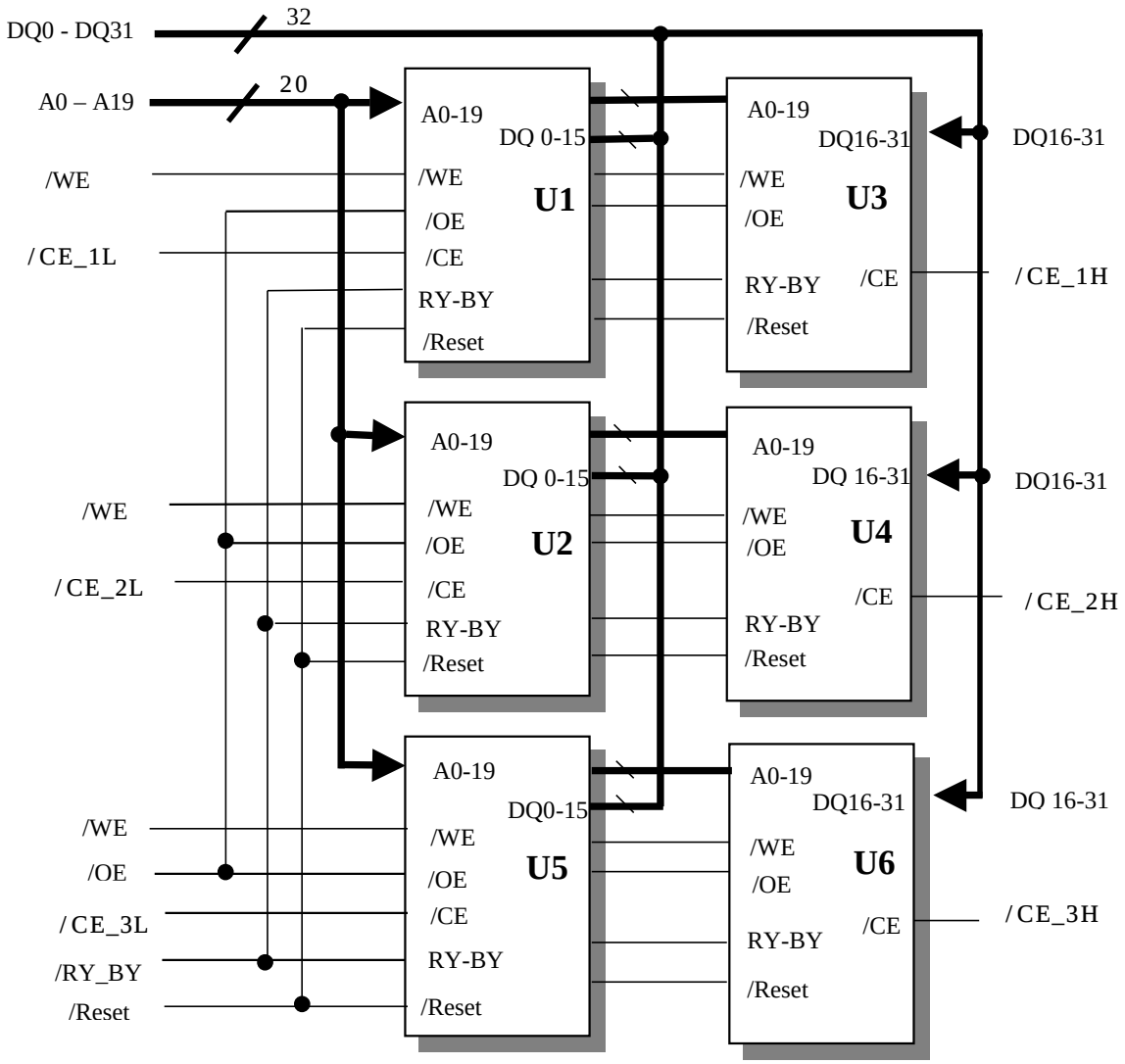
72-pin SIMM	M

PIN ASSIGNMENT

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	25	DQ17	49	/WE
2	/RESET	26	DQ18	50	A18
3	DQ0	27	DQ19	51	A17
4	DQ1	28	DQ20	52	A16
5	DQ2	29	DQ21	53	A15
6	DQ3	30	Vcc	54	A14
7	DQ4	31	DQ22	55	A13
8	DQ5	32	DQ23	56	A12
9	DQ6	33	/CE_1H	57	A11
10	Vcc	34	/CE_2H	58	A10
11	DQ7	35	DQ24	59	Vcc
12	/CE_1L	36	DQ25	60	A9
13	/CE_2L	37	DQ26	61	A8
14	DQ8	38	DQ27	62	A7
15	DQ9	39	Vss	63	A6
16	DQ10	40	DQ28	64	A5
17	DQ11	41	DQ29	65	A4
18	DQ12	42	DQ30	66	A3
19	DQ13	43	DQ31	67	A2
20	DQ14	44	NC	68	A1
21	DQ15	45	NC	69	A0
22	NC	46	/CE_3L	70	NC
23	/CE_3H	47	A19	71	NC
24	DQ16	48	/OE	72	Vss

72-PIN SIMM
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5V to +4.0V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5V to +4.0V
Power Dissipation	P_D	6W
Storage Temperature	T_{STG}	-65°C to +150°C
Operating Temperature	T_A	-55°C to +125°C

w Stresses greater than those listed under " Absolute Maximum Ratings" may cause perman ent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP.	MAX
Supply Voltage	V_{CC}	2.7V	3.0V	3.6V
Ground	V_{SS}	0	0	0
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3V
Input Low Voltage	V_{IL}	-0.5	-	0.8V

DC CHARACTERISTICS (CMOS Compatible)

PARAMETER	DESCRIPTION	TEST CONDITIONS		MIN	TYP.	MAX	UNIT
I_{LI}	Input Load Current	V_{IN}=Vss to Vcc, Vcc=Vcc max				±1.0	uA
I_{LIT}	A9 Input Load Current	Vcc= Vcc max ; A9=12.5V				35	uA
I_{LO}	Output Leakage Current	V_{OUT}= Vss to Vcc, Vcc= Vcc max				±1.0	uA
I_{CC1}	Vcc Active Read Current (Note1)	/CE=V_{IK}, /OE=V_{IH} Byte Mode	5MHZ		9	16	mA
			1MHZ		2	4	
		/CE=V_{IL}, /OE=V_{IH} Word Mode	5MHZ		9	16	
			1MHZ		2	4	
I_{CC2}	Vcc Active Write Current (Note 2 and 4)	/CE=V_{IL}, /OE=V_{IH}			20	30	mA
I_{CC3}	Vcc Standby Current	Vcc=Vcc max ; /CE,/Reset=Vcc±0.3V			0.2	5	uA
I_{CC4}	Vcc Standby Current During Reset	Vcc=Vcc max ; /Reset=Vss±0.3V			0.2	5	uA
I_{CC5}	Automatic Sleep Mode(Note3)	V_{IH}=Vcc±0.3V; V_{IL}=Vss±0.3V			0.2	5	uA
V_{IL}	Input Low Voltage			-0.5		0.8	V
V_{IH}	Input High Voltage			0.7xVcc		Vcc+0.3	V

V_{ID}	Voltage for Autoselect and Temporary Unprotect	Vcc=3.3V	11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL}=4.0mA, Vcc=Vcc min			0.45	V
V_{OH1}	Output High Voltage	I_{OH}=-2.0mA, Vcc=Vcc min	0.85xVcc			V
V_{OH2}		I_{OH}=-100uA, Vcc= Vcc min	Vcc-0.4			V
V_{LKO}	Low Vcc Lock-Out Voltage		2.3		2.5	V

Note :

1. The Icc current listed is typically less 2mA/MHz, with /OE at V_{IH}. Typical Vcc is 3.0V.
2. Icc active while Embedded Erase or Embedded Program is progress.
3. Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC}+30ns. Typical sleep mode current is 200nA.
4. Not 100% tested.

LATCHUP CHARACTERISTICS

DESCRIPTION	MIN	MAX
Input Voltage with respect to Vss on all pins except I/O Pins (Including A9,/OE, and /Reset)	-1.0V	12.5V
Input Voltage with respect to Vss on all I/O Pins	-1.0V	Vcc+1.0V
Vcc Current	-100mA	+100mA

Includes all pins except Vcc. Test conditions: Vcc=3.0V, one pin at a time.

DATA RETENTION

PARAMETER	TEST CONDITIONS	MIN	UNIT
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER		TYP (NOTE1)	MAX (NOTE2)	UNIT	COMMENTS
Sector Erase Time		0.7	15	s	Excludes 00h programming prior to erasure (Note4)
Chip Erase Time		25		s	
Byte Programming Time		9	300	us	Excludes system level overhead (Note5)
Word Programming Time		11	360	us	
Chip Programming Time (Note3)	Byte Mode	18	54	s	
	Word Mode	12	36	s	

Notes :

1. Typical program and erase times assume the following conditions: 25 ^{O}C, 3.0V Vcc, 1,000,000 cycles. Additionally programming typical assume checkerboard pattern.
2. Under worst case conditions of 90^{O}C, Vcc=2.7V, 1,000,000 cycles.
3. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed
4. In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.
5. System-level overhead is the time required to excute the two-or four-bus-cycle sequence for the program command. See table 9 for further information on command definitions.
6. The device has a minimum erase and program cycle endurance of 1,000,000 cycles.

SOP/TSOP PIN CAPACITANCE

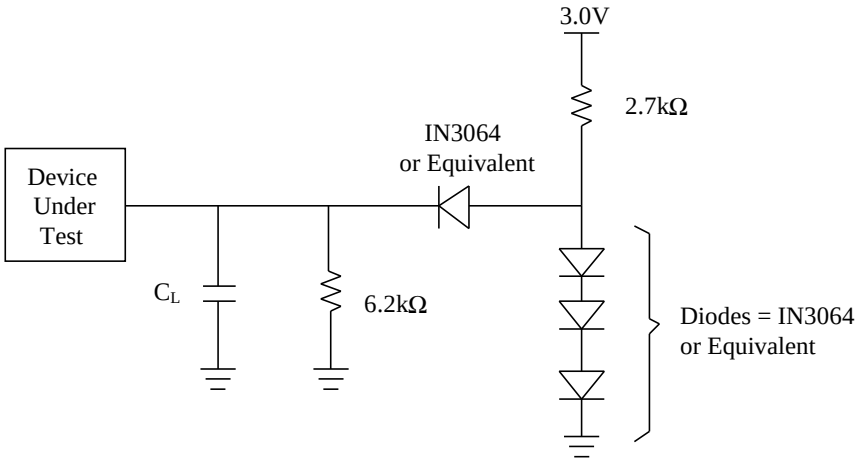
PARAMETER SYMBOL	PARAMETER DESCRIPTION	TEST SETUP	TYP.	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes : 1. Sampled, not 100% tested

2.Test conditions T_A = 25^{o} C, f=1.0 MHz.

TEST SPECIFICATIONS

TEST CONDITION	80R	-90/ -120	UNIT
Output load	1TTL gate		
Output load capacitance, C_L (Including jig capacitance)	30	100	pF
Input rise and fall times	5		ns
Input pulse levels	0.0 - 3.0		V
Input timing measurement reference levels	1.5		V
Output timing measurement reference levels	1.5		V



Note : C_L = 100pF including jig capacitance

AC CHARACTERISTICS

u Erase / Program Operations

PARAMETER SYMBOLS		DESCRIPTION			-80	-90	UNIT
JEDEC	Standard						
t_{AVAV}	t_{WC}	Write Cycle Time (Note1)		Min	80	90	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0		ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45	45	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	35	45	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0		ns
	t_{OES}	Output Enable Setup Time		Min	0		ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (/OE High to /WE Low)		Min	0		ns
t_{ELWL}	t_{CS}	/CE Setup Time		Min	0		ns
t_{WHEH}	t_{CH}	/CE Hold Time		Min	0		ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35	35	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	30		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note2)	Byte	Typ	9		us
			Word	Typ	11		us
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note2)		Typ	0.7		sec
	t_{VCS}	Vcc Setup Time (Note1)		Min	50		us
	t_{RB}	Recovery Time from RY//BY		Min	0		ns
	t_{BUSY}	Program/ Erase Valid to RY//BY Delay		Min	90		ns

Note:

1. Not 100% tested.

2. See the "Erase and Programming Performance" section for more Information

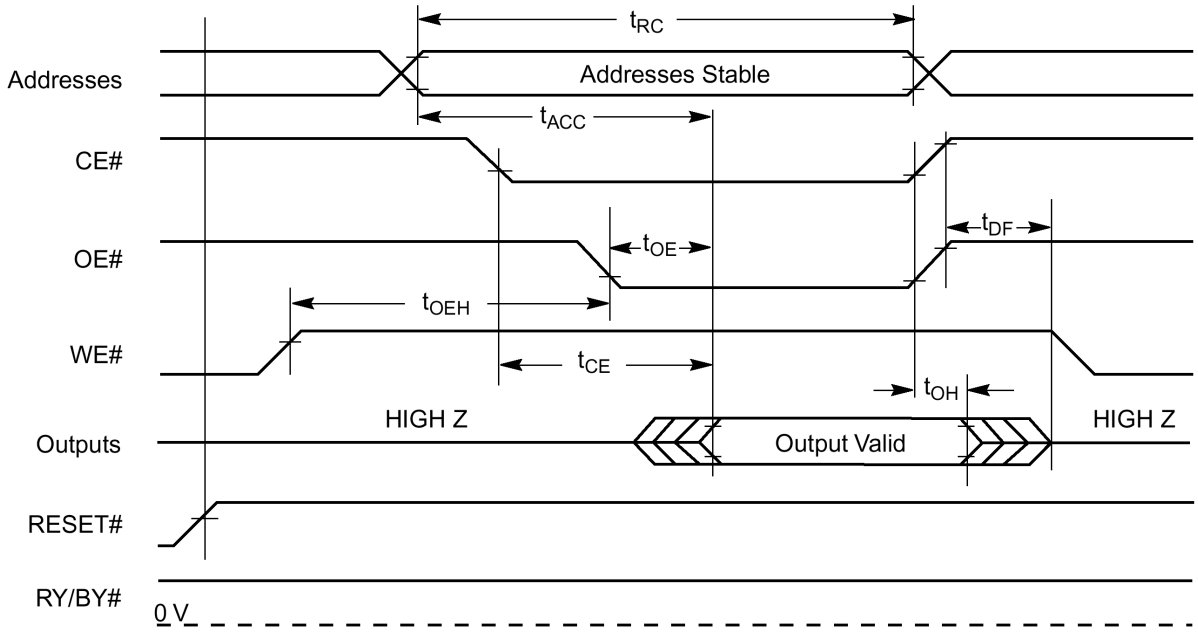
u Alternate /CE Controlled Erase/ Program Operations

PARAMETER SYMBOLS		DESCRIPTION			-80	-90	UNIT
JEDEC	Standard						
t_{AVAV}	t_{WC}	Write Cycle Time (Note1)		Min	80	90	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0		ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45	45	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	35	45	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0		ns
	t_{OES}	Output Enable Setup Time		Min	0		ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (/OE High to /WE Low)		Min	0		ns
t_{WLEL}	t_{WS}	/WE Setup Time		Min	0		ns
t_{EHWH}	t_{WH}	/WE Hold Time		Min	0		ns
t_{ELEH}	t_{CP}	/CE Pulse Width		Min	35	35	ns
t_{EHEL}	t_{CPH}	/CE Pulse Width High		Min	30		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note2)	Byte	Min	9		us
			Word	Min	11		us
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note2)		Min	0.7		

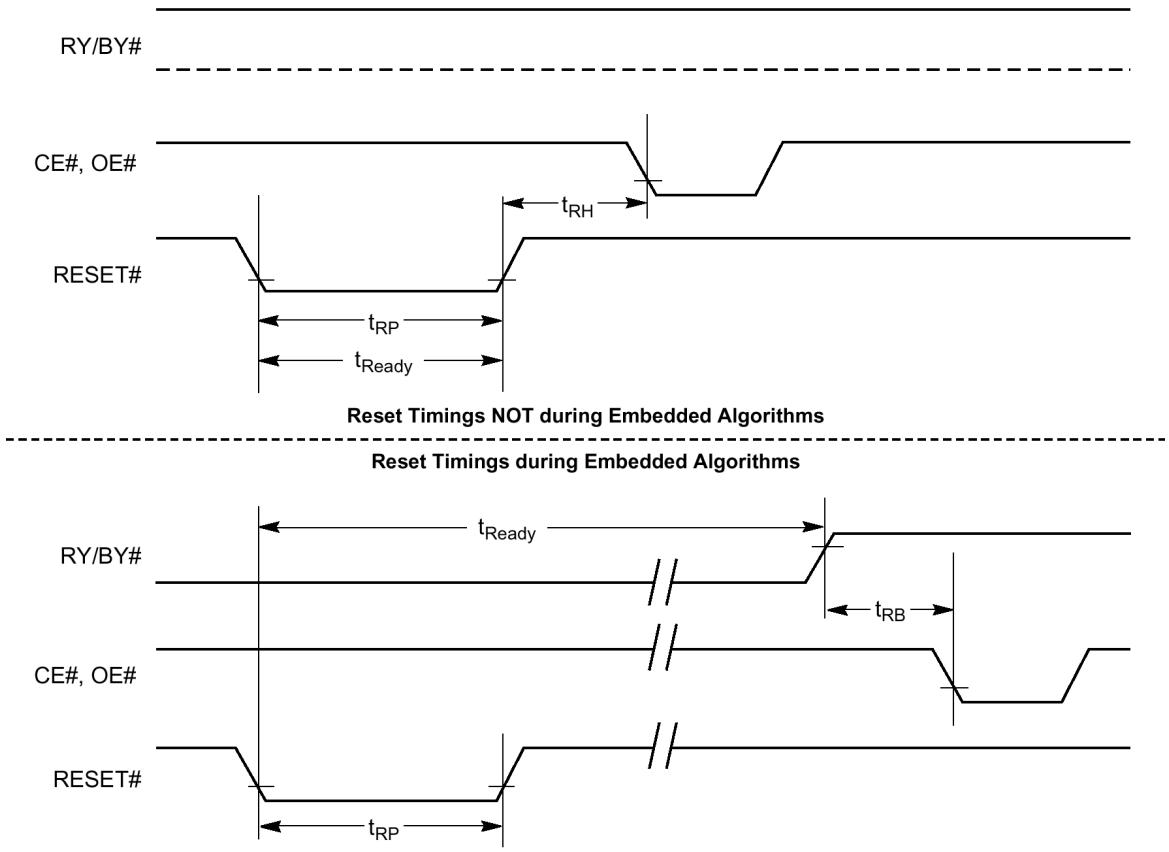
Note: 1. Not 100% tested.

2. See the "Erase and Programming Performance" section for more Information.

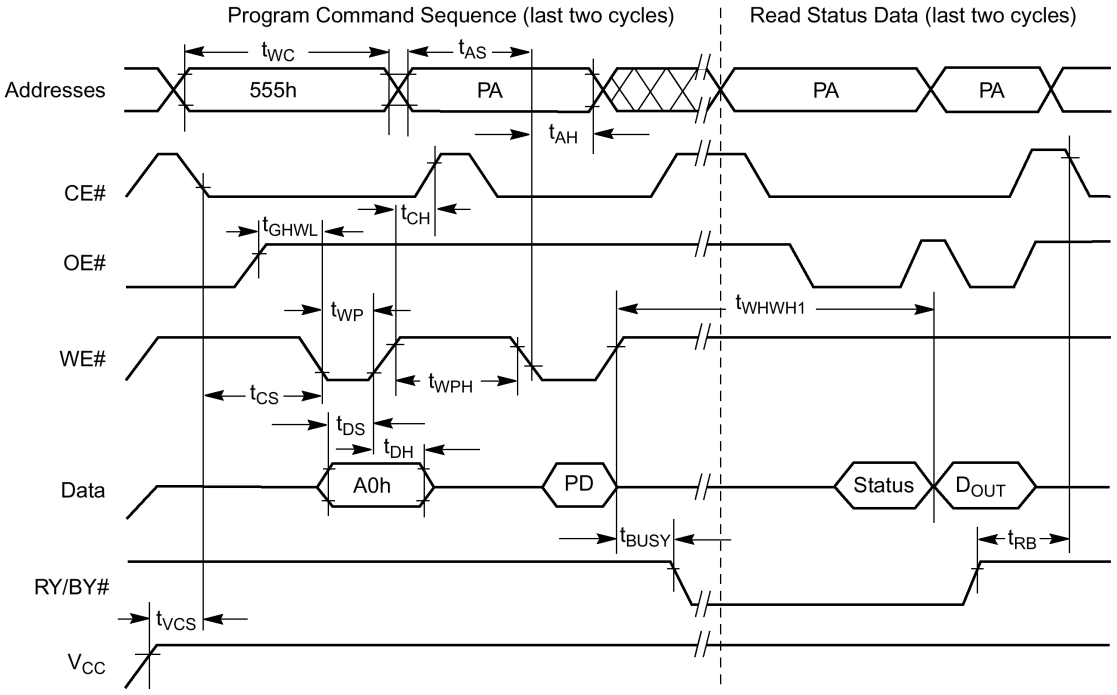
u READ OPERATIONS TIMING



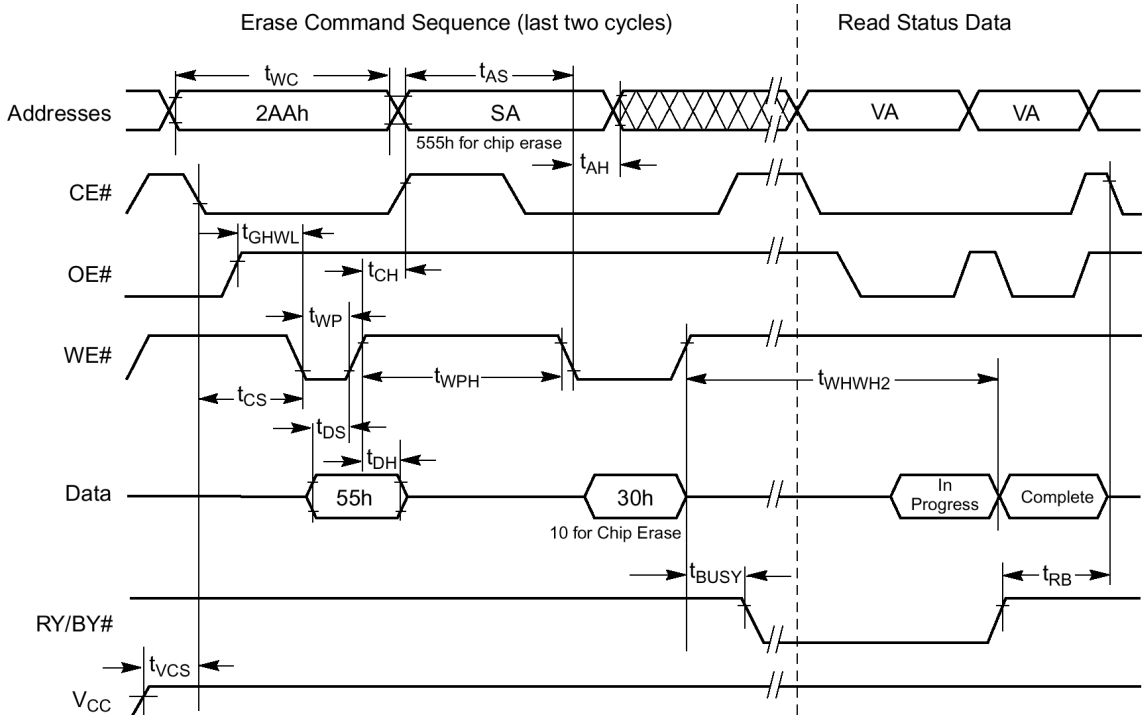
u RESET TIMING



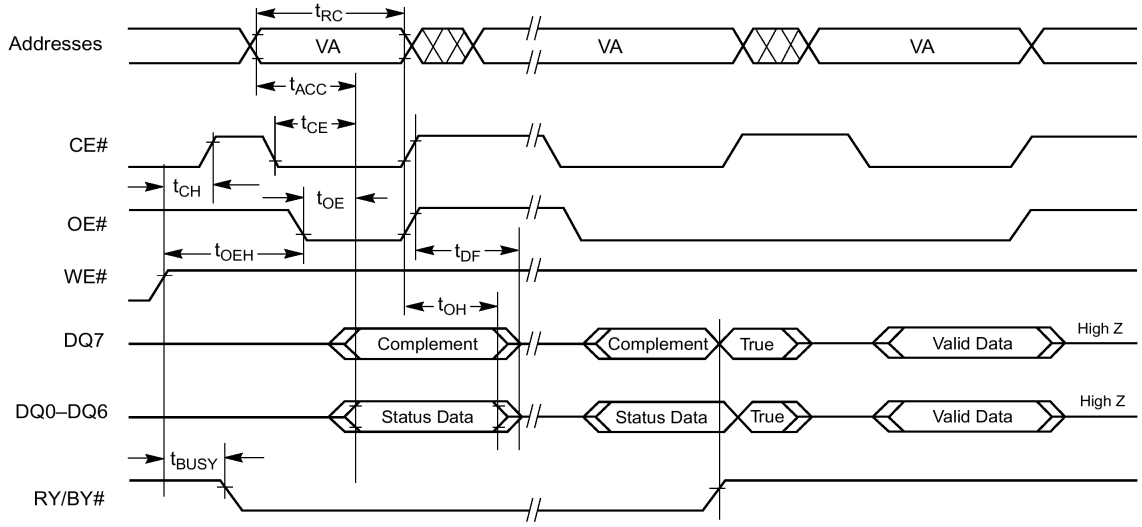
u PROGRAM OPERATIONS TIMING



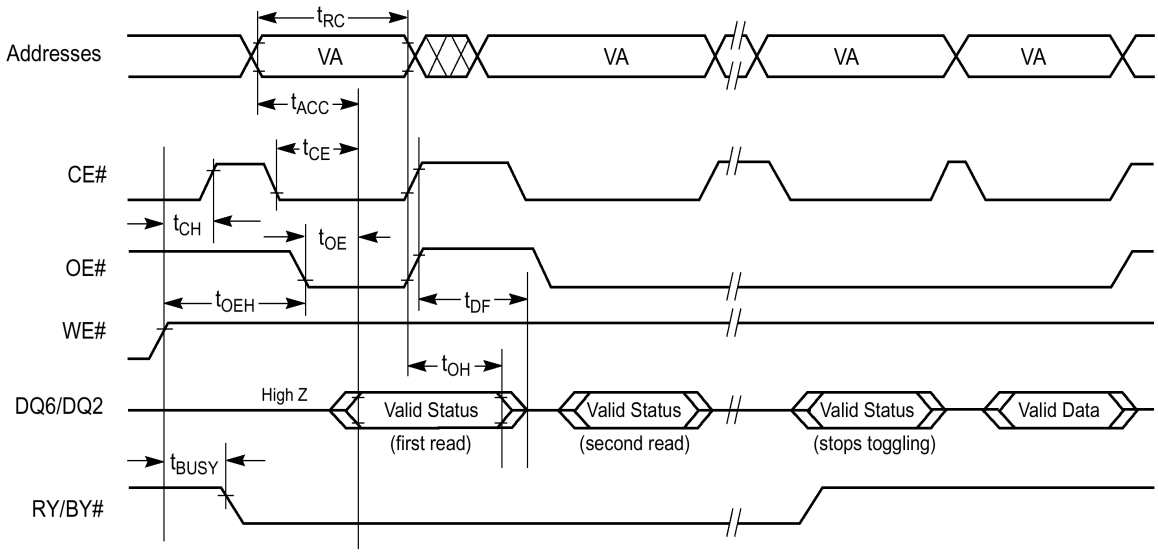
u CHIP/SECTOR ERASE OPERATION TIMINGS



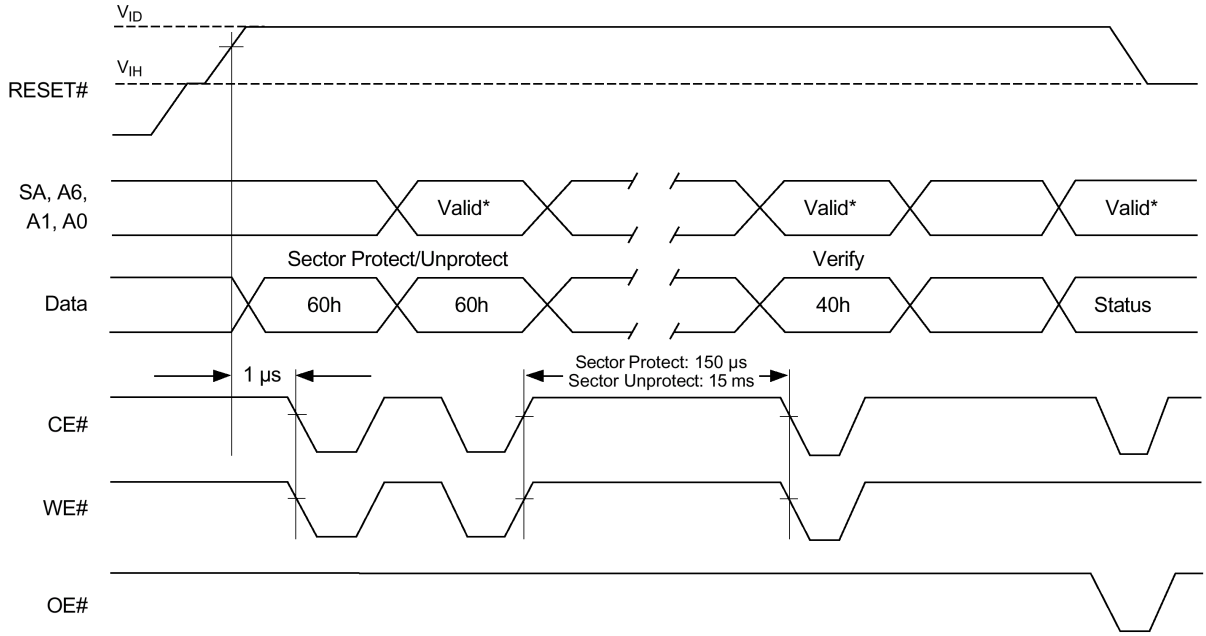
u DATA# POLLING TIMES(DURING EMBEDDED ALGORITHMS)



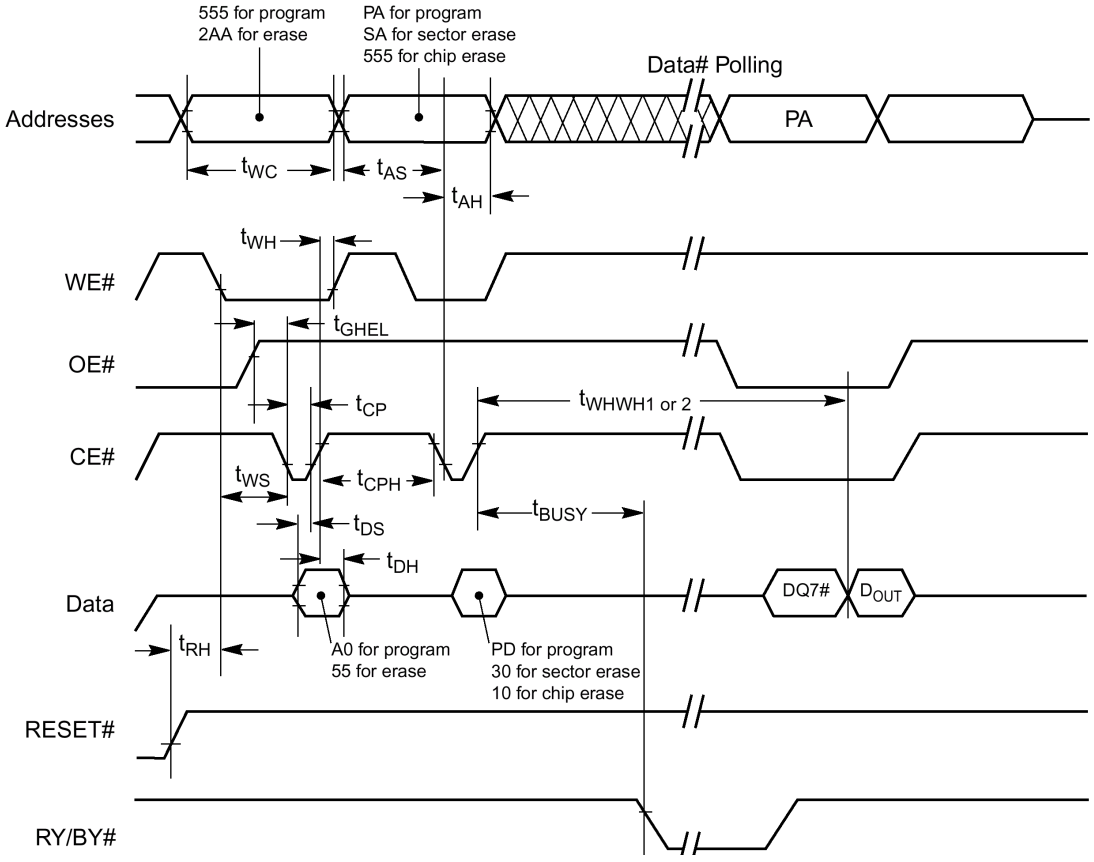
u TOGGLE# BIT TIMINGS (DURING EMBEDDED ALGORITHMS)



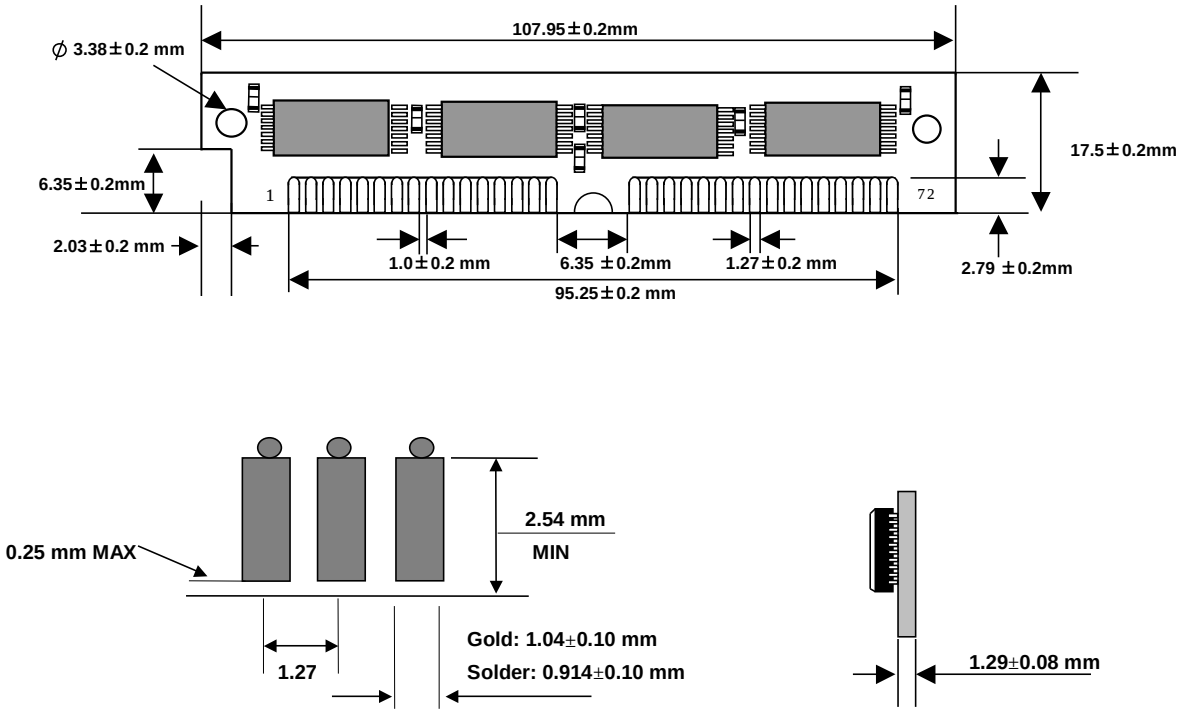
u SECTOR PROTECT UNPROTECT TIMEING DIAGRAM



u ALTERNATE CE# CONTROLLED WRITE OPERATING TIMINGS



PACKAGE DIMENSIONS



(Solder & Gold Plating)

ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	Speed
HMF3M32M6V-70	12MByte	3MX 32bit	72 Pin-SIMM	6EA	3.3V	70ns
HMF3M32M6V-80	12MByte	3MX 32bit	72 Pin-SIMM	6EA	3.3V	80ns
HMF3M32M6V-90	12MByte	3MX 32bit	72 Pin-SIMM	6EA	3.3V	90ns
HMF3M32M6V-120	12MByte	3MX 32bit	72 Pin-SIMM	6EA	3.3V	120ns