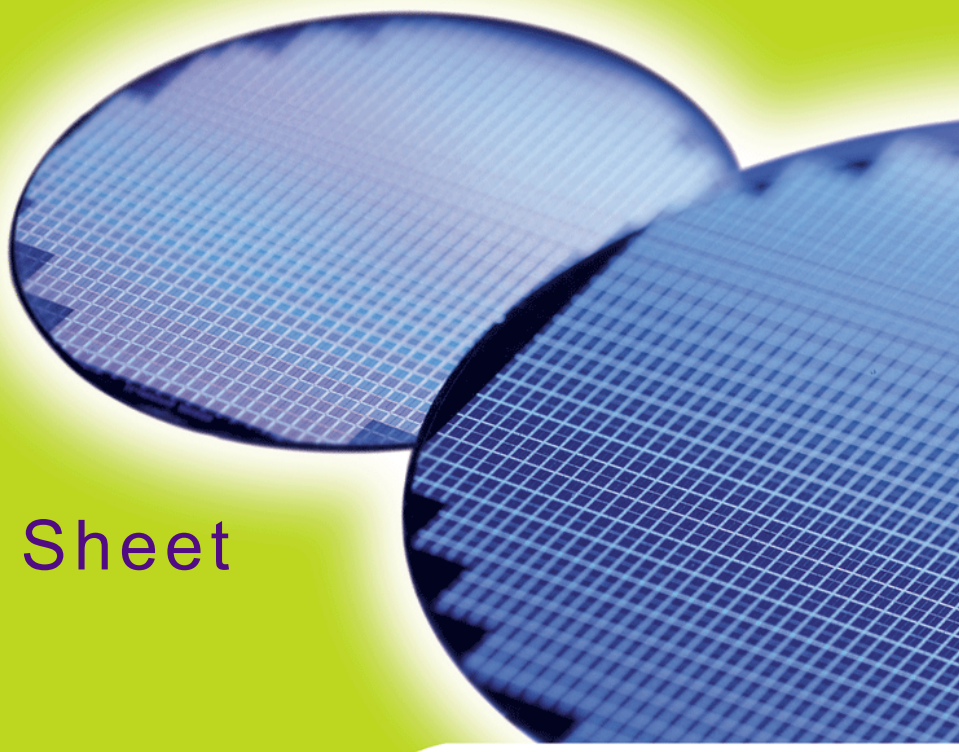
Nov 2006

HYB18M512160BF-6
HYE18M512160BF-6
HYB18M512160BF-7.5
HYE18M512160BF-7.5

DRAMs for Mobile Applications
512-Mbit DDR Mobile-RAM
RoHS compliant



Internet Data Sheet

Rev.1.80

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HYB18M512160BF-6; HYE18M512160BF-6 HYE18M512160BF-7.5

Revision History:	**Rev.1.80**	**2006-11**
Previous Version:	1.70	
all	converted into QAG template	
18	table 15: added typ. values	

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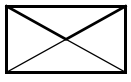


1 Overview

1.1 Features

- 4 banks × 8 Mbit × 16 organization
- Double-data-rate architecture : two data transfers per clock cycle
- Bidirectional data strobe (DQS) is transmitted / received with data; to be used in capturing data at the receiver
- DQS is edge-aligned with data for READs and center-aligned with data for WRITEs
- Differential clock input (CK / $\overline{CK}$)
- Commands entered on positive CK edge; data and mask data are referenced to both edges of DQS
- Four internal banks for concurrent operation
- Programmable CAS latency: 2 and 3
- Programmable burst length: 2, 4, 8 and 16
- Programmable drive strength (full, half, quarter)
- Auto refresh and self refresh modes
- 8192 refresh cycles / 64ms
- Auto precharge
- Commercial (0°C to +70°C) and Extended (-25°C to +85°C) operating temperature range
- 60-ball Very Thin FBGA package (10.5 × 10.5 × 1.0 mm)
- RoHS Compliant Product[1)]

Power Saving Features

- Low supply voltages: V_{DD} = 1.70 V – 1.90 V, V_{DDQ} = 1.70 V – 1.90 V
- Optimized operating (I_{DD0} , I_{DD4}), self refresh (I_{DD6}) and standby currents (I_{DD2} , I_{DD3})
- DDR I/O scheme with no DLL
- Programmable Partial Array Self Refresh (PASR)
- Temperature Compensated Self-Refresh (TCSR), controlled by on-chip temperature sensor
- Clock Stop, Power-Down and Deep Power-Down modes

Table 1 Performance

Part Number Speed Code		- 6	- 7.5	Unit
Clock Frequency (f_{CKmax})	CL = 3	166	133	MHz
	CL = 2	83	66	MHz
Access Time (t_{ACmax})		5.5	6.5	ns

Table 2 Memory Addressing Scheme

Item	Addresses
Banks	BA0, BA1
Rows	A0 - A12
Columns	A0 - A9

1)RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

green Product

Table 3 Ordering Information

Type[1)]	Package	Description
Commercial Temperature Range		
HYB18M512160BF-6	P-VFBGA-60-1	166 MHz 4 Banks × 8 Mbit × 16 Low Power DDR SDRAM
HYB18M512160BF-7.5	P-VFBGA-60-1	133 MHz 4 Banks × 8 Mbit × 16 Low Power DDR SDRAM
Extended Temperature Range		
HYE18M512160BF-6	P-VFBGA-60-1	166 MHz 4 Banks × 8 Mbit × 16 Low Power DDR SDRAM
HYE18M512160BF-7.5	P-VFBGA-60-1	133 MHz 4 Banks × 8 Mbit × 16 Low Power DDR SDRAM

1) HYB / HYE: Designator for memory products (HYB: standard temp. range; HYE: extended temp. range)
18M: 1.8V DDR Mobile-RAM
512: 512 MBit density
160: 16 bit interface width
B: die revision
F: green product
-6/-7.5: speed grades (min. clock cycle time)

1.2 Pin Configuration

1	2	3		7	8	9
V_{SS}	DQ15	V_{SSQ}	A	V_{DDQ}	DQ0	V_{DD}
V_{DDQ}	DQ13	DQ14	B	DQ1	DQ2	V_{SSQ}
V_{SSQ}	DQ11	DQ12	C	DQ3	DQ4	V_{DDQ}
V_{DDQ}	DQ9	DQ10	D	DQ5	DQ6	V_{SSQ}
V_{SSQ}	UDQS	DQ8	E	DQ7	LDQS	V_{DDQ}
V_{SS}	UDM	NC	F	NC	LDM	V_{DD}
CKE	CK	$\overline{CK}$	G	$\overline{WE}$	$\overline{CAS}$	$\overline{RAS}$
A9	A11	A12	H	$\overline{CS}$	BA0	BA1
A6	A7	A8	J	A10/AP	A0	A1
V_{SS}	A4	A5	K	A2	A3	V_{DD}

Figure 1 Standard Ballout 512-Mbit DDR Mobile-RAM (Top View)

1.3 Description

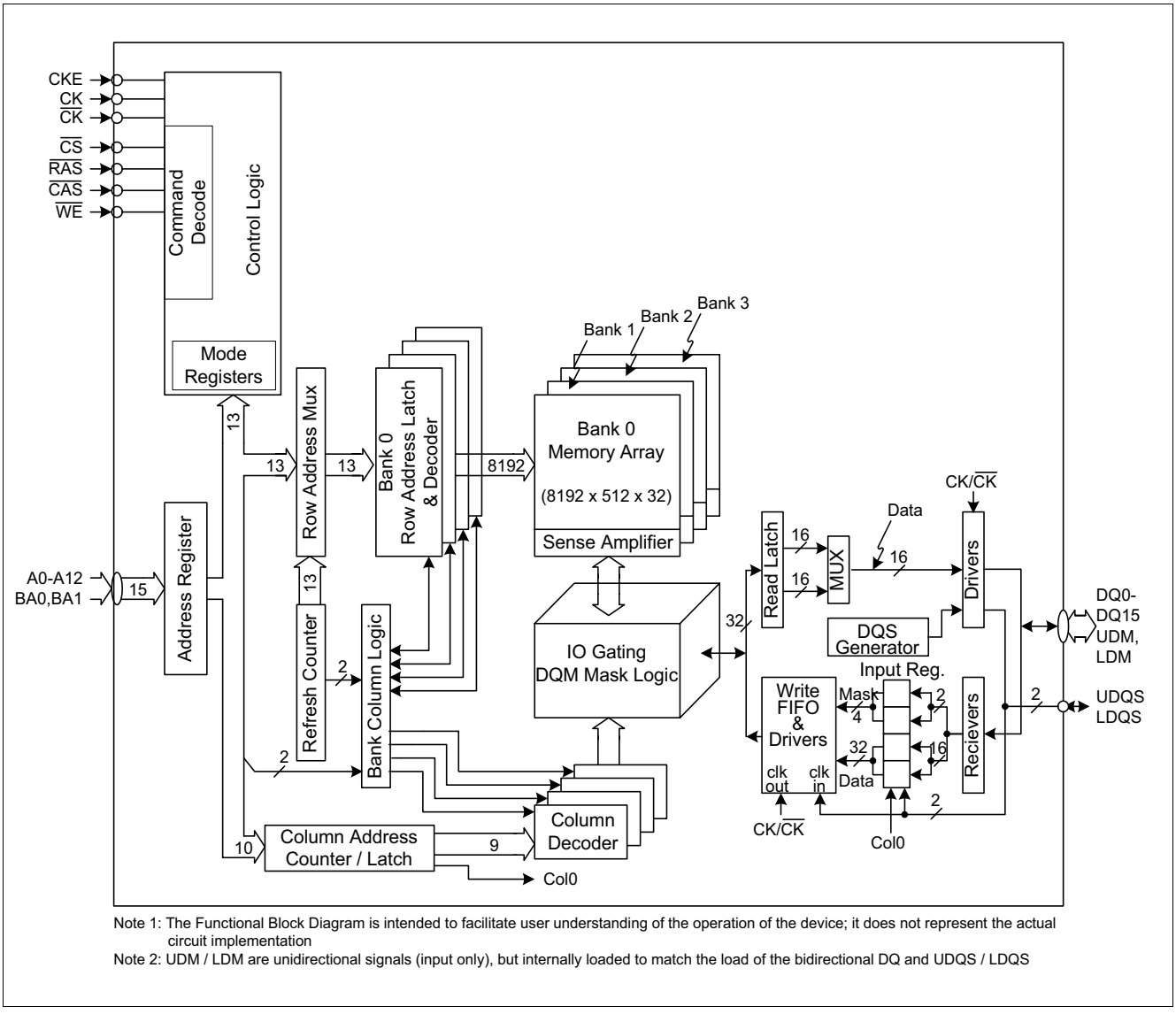
The HY[B/E]18M512160BF is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM.

The HY[B/E]18M512160BF uses a double-data-rate architecture to achieve high-speed operation. The double-data-rate architecture is essentially a *2n* prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE access for the DDR Mobile-RAM consists of a single *2n*-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

The HY[B/E]18M512160BF is especially designed for mobile applications. It operates from a 1.8V power supply. Power consumption in self refresh mode is drastically reduced by an On-Chip Temperature Sensor (OCTS); it can further be reduced by using the programmable Partial Array Self Refresh (PASR).

A conventional data-retaining Power-Down (PD) mode is available as well as a non-data-retaining Deep Power-Down (DPD) mode. For further power-savings the clock may be stopped during idle periods.

The HY[B/E]18M512160BF is housed in a 60-ball very thin FBGA package. It is available in Commercial (0°C to 70°C) and Extended (-25°C to +85°C) temperature range.



Note 1: The Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent the actual circuit implementation
Note 2: UDM / LDM are unidirectional signals (input only), but internally loaded to match the load of the bidirectional DQ and UDQS / LDQS

Figure 2 Functional Block Diagram

1.4 Pin Definition and Description

Table 4 Pin Description

Ball	Type	Detailed Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control inputs are sampled on crossing of the positive edge of CK and negative edge of $\overline{CK}$.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides precharge power-down and self refresh operation (all banks idle), or active power-down (row active in any bank). CKE must be maintained HIGH throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during power-down. Input buffers, excluding CKE are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DQ0 - DQ15	I/O	**Data Inputs/Output:** Bi-directional data bus (16 bit)
LDQS, UDQS	I/O	**Data Strobe:** output with read data, input with write data. Edge-aligned with read data, centered with write data. Used to capture write data. LDQS corresponds to the data on DQ0 - DQ7; UDQS to the data on DQ8 - DQ15.
LDM, UDM	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. DM may be driven HIGH, LOW, or floating during READs. LDM corresponds to the data on DQ0 - DQ7; UDM to the data on DQ8 - DQ15.
BA0, BA1	Input	**Bank Address Inputs:** BA0 and BA1 define to which bank an ACTIVATE, READ, WRITE or PRECHARGE command is being applied. BA0, BA1 also determine which mode register is to be loaded during a MODE REGISTER SET command (MRS or EMRS).
A0 - A12	Input	**Address Inputs:** Provide the row address for ACTIVE commands and the column address and Auto Precharge bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 (=AP) is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10=LOW) or all banks (A10=HIGH). If only one bank is to be precharged, the bank is selected by BA0 and BA1. The address inputs also provide the op-code during a MODE REGISTER SET command.
V_{DDQ}	Supply	**I/O Power Supply:** Isolated power for DQ output buffers for improved noise immunity: V_{DDQ} = 1.70 V – 1.90 V
V_{SSQ}	Supply	**I/O Ground**
V_{DD}	Supply	**Power Supply:** Power for the core logic and input buffers, V_{DD} = 1.70 V – 1.90 V
V_{SS}	Supply	**Ground**
N.C.	–	**No Connect**

2 Functional Description

The 512-Mbit DDR Mobile-RAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM.

READ and WRITE accesses to the DDR Mobile-RAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the banks, A0 - A12 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the DDR Mobile-RAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command description and device operation.

2.1 Register Definition

2.1.1 Mode Register

The Mode Register is used to define the specific mode of operation of the DDR Mobile-RAM. This definition includes the selection of a burst length (bits A0-A2), a burst type (bit A3) and a CAS latency (bits A4-A6). The Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power.

The Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements results in unspecified operation.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

MR
Mode Register Definition **(BA[1:0] = 00_B)**

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**CL**			**BT**	**BL**		

Field	Bits	Type	Description
CL	[6:4]	w	**CAS Latency** 010 2 011 3 *Note: All other bit combinations are RESERVED.*
BT	3	w	**Burst Type** 0 Sequential 1 Interleaved
BL	[2:0]	w	**Burst Length** 001 2 010 4 011 8 100 16 *Note: All other bit combinations are RESERVED.*

2.2 Function Truth Tables

Table 5 Truth Table - CKE

CKEn-1	CKEn	Current State	Command	Action	Notes
L	L	Power-Down	X	Maintain Power-Down	1)2)3)4)
		Self Refresh	X	Maintain Self Refresh	1) to 4)
		Deep Power-Down	X	Maintain Deep Power-Down	1) to 4)
L	H	Power-Down	DESELECT or NOP	Exit Power-Down	1) to 5)
		Self Refresh	DESELECT or NOP	Exit Self Refresh	1) to 5)
		Deep Power-Down	X	Exit Deep Power-Down	1) to 4), 6)
H	L	All Banks Idle	DESELECT or NOP	Enter Precharge Power-Down	1) to 4)
		Bank(s) Active	DESELECT or NOP	Enter Active Power-Down	1) to 4)
		All Banks Idle	AUTO REFRESH	Enter Self Refresh	1) to 4)
		All Banks Idle	BURST TERMINATE	Enter Deep Power-Down	1) to 4)
H	H	see Table 6 and Table 7			1) to 4)

1) CKEn is the logic state of CKE at clock edge n; CKEn-1 was the state of CKE at the previous clock edge.
2) Current state is the state immediately prior to clock edge n.
3) COMMAND n is the command registered at clock edge n; ACTION n is a result of COMMAND n.
4) All states and sequences not shown are illegal or reserved.
5) DESELECT or NOP commands should be issued on any clock edges occurring during t_{XP} or t_{XSR} period.
6) Exit from DEEP POWER DOWN requires the same command sequence as for power-up initialization.

Table 6 Current State Bank n - Command to Bank n

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command / Action	Notes
Any	H	X	X	X	DESELECT (NOP / continue previous operation)	1)2)3)4)5)6)
	L	H	H	H	NO OPERATION (NOP / continue previous operation)	1) to 6)
Idle	L	L	H	H	ACTIVE (select and activate row)	1) to 6)
	L	L	L	H	AUTO REFRESH	1) to 7)
	L	L	L	L	MODE REGISTER SET	1) to 7)
Row Active	L	H	L	H	READ (select column and start Read burst)	1) to 6), 8)
	L	H	L	L	WRITE (select column and start Write burst)	1) to 6), 8)
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	1) to 6), 9)
Read (Auto-Precharge Disabled)	L	H	L	H	READ (truncate Read and start new Read burst)	1) to 6), 8)
	L	H	L	L	WRITE (truncate Read and start new Write burst)	1) to 6), 8), 10)
	L	L	H	L	PRECHARGE (truncate Read and start Precharge)	1) to 6), 9)
	L	H	H	L	BURST TERMINATE	1) to 6), 11)
Write (Auto-Precharge	L	H	L	H	READ (truncate Write and start Read burst)	1) to 6), 8), 12)
	L	H	L	L	WRITE (truncate Write and start Write burst)	1) to 6), 8)
	L	L	H	L	PRECHARGE (truncate Write burst, start Precharge)	1) to 6), 9),12)

1) This table applies when CKEn-1 was HIGH and CKEn is HIGH (see **Table 5**) and after t_{XP} or t_{XSR} has been met (if the previous state was power-down or self refresh).

2) This table is bank-specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.

3) Current state definitions:
   - Idle: The bank has been precharged, and t_{RP} has been met.
   - Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts / accesses and no register accesses are in progress.
   - Read: A READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   - Write: A WRITE burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

4) The following states must not be interrupted by a command issued to the same bank. DESELECT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and according to **Table 7**.
   - Precharging: Starts with registration of a PRECHARGE command and ends when t_{RP} is met. Once t_{RP} is met, the bank is in the “idle” state.
   - Row Activating: Starts with registration of an ACTIVE command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank is in the “row active” state.
   - Read with AP Enabled: Starts with registration of a READ command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.
   - Write with AP Enabled: Starts with registration of a WRITE command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.

5) The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.
   - Refreshing: Starts with registration of an AUTO REFRESH command and ends when t_{RC} is met. Once t_{RC} is met, the DDR Mobile-RAM is in the “all banks idle” state.
   - Accessing Mode Register: Starts with registration of a MODE REGISTER SET command and ends when t_{MRD} has been met. Once t_{MRD} is met, the DDR Mobile-RAM is in the “all banks idle” state.
   - Precharging All: Starts with registration of a PRECHARGE ALL command and ends when t_{RP} is met. Once t_{RP} is met, all banks are in the idle state.

6) All states and sequences not shown are illegal or reserved.
7) Not bank-specific; requires that all banks are idle and no bursts are in progress.
8) Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.
9) May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
10) A WRITE command may be applied after the completion of the Read burst; otherwise, a BURST TERMINATE command must be used to end the Read burst prior to issuing a WRITE command.
11) Not bank-specific; BURST TERMINATE affects the most recent Read burst, regardless of bank.
12) Requires appropriate DM masking.

Table 7 Current State Bank n - Command to Bank m (different bank)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command / Action	Notes
Any	H	X	X	X	DESELECT (NOP / continue previous operation)	1)2)3)4)5)6)
	L	H	H	H	NO OPERATION (NOP / continue previous operation)	1) to 6)
Idle	X	X	X	X	Any command otherwise allowed to bank m	1) to 6)
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	1) to 6)
	L	H	L	H	READ (select column and start Read burst)	1) to 7)
	L	H	L	L	WRITE (select column and start Write burst)	1) to 7)
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	1) to 6)
Read (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	1) to 6)
	L	H	L	H	READ (truncate Read and start new Read burst)	1) to 7)
	L	H	L	L	WRITE (truncate Read and start Write burst)	1) to 8)
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	1) to 6)
Write (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	1) to 6)
	L	H	L	H	READ (truncate Write and start Read burst)	1) to 7), 9)
	L	H	L	L	WRITE (truncate Write and start new Write burst)	1) to 7)
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	1) to 6)
Read (with Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	1) to 6)
	L	H	L	H	READ (truncate Read and start new Read burst)	1) to 7)
	L	H	L	L	WRITE (truncate Read and start Write burst)	1) to 8)
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	1) to 6)
Write (with Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	1) to 6)
	L	H	L	H	READ (truncate Write and start Read burst)	1) to 7)
	L	H	L	L	WRITE (truncate Write and start new Write burst)	1) to 7)
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	1) to 6)

1) This table applies when CKEn-1 was HIGH and CKEn is HIGH (see **Table 5**) and after t_{XP} or t_{XSR} has been met (if the previous state was power-down or self refresh).
2) This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.

3) Current state definitions:
   - Idle: The bank has been precharged, and t_{RP} has been met.
   - Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts / accesses and no register accesses are in progress.
   - Read: A READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   - Write: A WRITE burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   - Read with AP Enabled: see following text.
   - Write with AP Enabled: see following text.

   3a. The Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states can each be broken into two parts: the access period and the precharge period. For Read with Auto Precharge, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For Write with Auto Precharge, the precharge period begins when t_{WR} ends, with t_{WR} measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or t_{RP}) begins. During the precharge period of the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states, ACTIVE, PRECHARGE, READ and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other bank may be applied. In either case, all other related limitations apply (e.g. contention between READ data and WRITE data must be avoided).

4) AUTO REFRESH, SELF REFRESH and MODE REGISTER SET commands may only be issued when all banks are idle.
5) A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6) All states and sequences not shown are illegal or reserved.
7) Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.
8) A WRITE command may be applied after the completion of the Read burst; otherwise, a BURST TERMINATE command must be used to end the Read burst prior to issuing a WRITE command.
9) Requires appropriate DM masking.

3 Electrical Characteristics

3.1 Operating Conditions

Table 8 Absolute Maximum Ratings

Parameter		Symbol	Values		Unit
			min.	max.	
Power Supply Voltage		V_{DD}	-0.3	2.7	V
Power Supply Voltage for Output Buffer		V_{DDQ}	-0.3	2.7	V
Input Voltage		V_{IN}	-0.3	V_{DDQ} + 0.3	V
Output Voltage		V_{OUT}	-0.3	V_{DDQ} + 0.3	V
Operation Case Temperature	Commercial	T_C	0	+70	°C
	Extended	T_C	-25	+85	°C
Storage Temperature		T_{STG}	-55	+150	°C
Power Dissipation		P_D	–	0.7	W
Short Circuit Output Current		I_{OUT}	–	50	mA

Attention: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 9 Pin Capacitances[1)2)3)]

Parameter	Symbol	Values		Unit
		min.	max.	
Input capacitance: CK, $\overline{CK}$	C_{I1}	1.5	2.5	pF
Delta input capacitance: CK, $\overline{CK}$	CD_{I1}	–	0.25	pF
Input capacitance: all other input-only pins	C_{I2}	1.5	2.5	pF
Delta input capacitance: all other input-only pins	CD_{I2}	–	0.5	pF
Input/output capacitance: DQ, DQS, DM	C_{IO}	3.5	4.5	pF
Delta input/output capacitance: DQ, DQS, DM	CD_{IO}	–	0.5	pF

1) These values are not subject to production test but verified by device characterization.

2) Input capacitance is measured according to JEP147 procedure for measuring capacitance using a vector network analyzer. VDD, VDDQ are applied and all other pins (except the pin under test) are floating. DQ's should be in high impedance state. This may be achieved by pulling CKE to low level.

3) Although DM is an input-only pin, it's input capacitance models the input capacitance of the DQ and DQS pins.

Table 10 Electrical Characteristics[1)2)]

Parameter	Symbol	Values		Unit	Notes
		min.	max.		
Power Supply Voltage	V_{DD}	1.70	1.90	V	–
Power Supply Voltage for DQ Output Buffer	V_{DDQ}	1.70	1.90	V	–
Input leakage current	I_{IL}	-1.0	1.0	µA	–
Output leakage current	I_{OL}	-1.5	1.5	µA	–
Address and Command Inputs (BA0, BA1, A0 - A12, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)					
Input high voltage	V_{IH}	$0.8 \times V_{DDQ}$	V_{DDQ} + 0.3	V	–
Input low voltage	V_{IL}	-0.3	$0.2 \times V_{DDQ}$	V	–
Clock Inputs (CK, $\overline{CK}$)					
DC input voltage	V_{IN}	-0.3	V_{DDQ} + 0.3	V	–
DC input differential voltage	$V_{ID(DC)}$	$0.4 \times V_{DDQ}$	V_{DDQ} + 0.6	V	3)
AC input differential voltage	$V_{ID(AC)}$	$0.6 \times V_{DDQ}$	V_{DDQ} + 0.6	V	3)
AC differential cross point voltage	V_{IX}	$0.4 \times V_{DDQ}$	$0.6 \times V_{DDQ}$	V	4)
Data Inputs (DQ0 - DQ15, LDM, UDM, LDQS, UDQS)					
DC input high voltage	$V_{IHD(DC)}$	$0.7 \times V_{DDQ}$	V_{DDQ} + 0.3	V	–
DC input low voltage	$V_{ILD(DC)}$	-0.3	0.3 x V_{DDQ}	V	–
AC input high voltage	$V_{IHD(AC)}$	$0.8 \times V_{DDQ}$	V_{DDQ} + 0.3	V	–
AC input low voltage	$V_{ILD(AC)}$	-0.3	$0.2 \times V_{DDQ}$	V	–
Data Outputs (DQ0 - DQ15, LDQS, UDQS)					
Output high voltage	V_{OH}	$0.9 \times V_{DDQ}$	–	V	–
Output low voltage	V_{OL}	–	$0.1 \times V_{DDQ}$	V	–

1) 0 °C ≤ T_C ≤ 70 °C (comm.); -25 °C ≤ T_C ≤ 85 °C (ext.);
All voltages referenced to V_{SS}. V_{SS} and V_{SSQ} must be at same potential.

2) See **Table 13** and **Figure 3** for overshoot and undershoot definition.

3) V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

4) The value of V_{IX} is expected to be equal to 0.5 x V_{DDQ} and must track variations in the DC level.

3.2 AC Characteristics

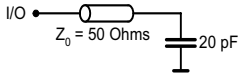
Table 11 AC Characteristics[1)2)3)4)]

Parameter		Symbol	- 6		- 7.5		Unit	Notes
			min.	max.	min.	max.		
DQ output access time from CK/$\overline{CK}$		t_{AC}	2	5.5	2.0	6.5	ns	5)6)
DQS output access time from CK/$\overline{CK}$		t_{DQSCK}	2	5.5	2.0	6.5	ns	5)6)
Clock high-level width		t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	–
Clock low-level width		t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	–
Clock half period		t_{HP}	min(t_{CL},t_{CH})		min(t_{CL},t_{CH})		ns	7)8)
Clock cycle time	CL = 3	t_{CK}	6	–	7.5	–	ns	9)
	CL = 2		12	–	15	–		
DQ and DM input setup time	fast slew rate	t_{DS}	0.6	–	0.75	–	ns	10)11)12)
	slow slew rate		TBD	–	0.85	–		10)11)13)
DQ and DM input hold time	fast slew rate	t_{DH}	0.6	–	0.75	–	ns	10)11)12)
	slow slew rate		TBD	–	0.85	–		10)11)13)
DQ and DM input pulse width		t_{DIPW}	2.1	–	1.7	–	ns	14)
Address and control input setup time	fast slew rate	t_{IS}	1.1	–	1.3	–	ns	12)15)16)
	slow slew rate		1.3	–	1.5	–		13)15)16)
Address and control input hold time	fast slew rate	t_{IH}	1.1	–	1.3	–	ns	12)15)16)
	slow slew rate		1.3	–	1.5	–		13)15)16)
Address and control input pulse width		t_{IPW}	2.7	–	3.0	–	ns	14)
DQ & DQS low-impedance time from CK/$\overline{CK}$		t_{LZ}	1.0	–	1.0	–	ns	17)
DQ & DQS high-impedance time from CK/$\overline{CK}$		t_{HZ}	–	5.5	–	6.5	ns	17)
DQS - DQ skew		t_{DQSQ}	–	0.5	–	0.6	ns	18)
DQ / DQS output hold time from DQS		t_{QH}	t_{HP}-t_{QHS}	–	t_{HP}-t_{QHS}	–	ns	8)
Data hold skew factor		t_{QHS}	–	0.65	–	0.75	ns	8)
Write command to 1st DQS latching transition		t_{DQSS}	0.75	1.25	0.75	1.25	t_{CK}	–
DQS input high-level width		t_{DQSH}	0.4	0.6	0.4	0.6	t_{CK}	–
DQS input low-level width		t_{DQSL}	0.4	0.6	0.4	0.6	t_{CK}	–
DQS falling edge to CK setup time		t_{DSS}	0.2	–	0.2	–	t_{CK}	–
DQS falling edge hold time from CK		t_{DSH}	0.2	–	0.2	–	t_{CK}	–
MODE REGISTER SET command period		t_{MRD}	2	–	2	–	t_{CK}	–
Write preamble setup time		t_{WPRES}	0	–	0	–	ns	19)
Write postamble		t_{WPST}	0.4	0.6	0.4	0.6	t_{CK}	20)
Write preamble		t_{WPRE}	0.25	–	0.25	–	t_{CK}	–
Read preamble	CL = 3	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	21)
	CL = 2		–	–	0.7	1.1		
Read postamble		t_{RPST}	0.4	0.6	0.4	0.6	t_{CK}	–
ACTIVE to PRECHARGE command period		t_{RAS}	42	70,000	45	70,000	ns	22)
ACTIVE to ACTIVE command period		t_{RC}	60	–	65	–	ns	22)
AUTO REFRESH to ACTIVE/AUTO REFRESH command period		t_{RFC}	72	–	75	–	ns	22)
ACTIVE to READ or WRITE delay		t_{RCD}	18	–	22.5	–	ns	22)
PRECHARGE command period		t_{RP}	18	–	22.5	–	ns	22)
ACTIVE bank A to ACTIVE bank B delay		t_{RRD}	12	–	15	–	ns	22)
WRITE recovery time		t_{WR}	15	–	15	–	ns	22)

Table 11 AC Characteristics[1)2)3)4)] (cont'd)

Parameter	Symbol	- 6		- 7.5		Unit	Notes
		min.	max.	min.	max.		
Auto precharge write recovery + precharge time	t_{DAL}	(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})				t_{CK}	23)
Internal write to Read command delay	t_{WTR}	1	–	1	–	t_{CK}	–
Self refresh exit to next valid command delay	t_{XSR}	120	–	120	–	ns	22)
Exit power down delay	t_{XP}	$t_{CK}+t_{IS}$	–	$t_{CK}+t_{IS}$	–	ns	
CKE minimum high or low time	t_{CKE}	2	–	2	–	t_{CK}	–
Refresh period	t_{REF}	–	64	–	64	ms	–
Average periodic refresh interval (8192 rows)	t_{REFI}	–	7.8	–	7.8	µs	24)

1) 0 °C ≤ T_C ≤ 70 °C (comm.); -25 °C ≤ T_C ≤ 85 °C (ext.); V_{DD} = V_{DDQ} = 1.70 V - 1.90 V. All voltages referenced to V_{SS}.
2) All parameters assume proper device initialization.
3) The CK/$\overline{CK}$ input reference level (for timing referenced to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross; the input reference level for signals other than CK/$\overline{CK}$ is V_{DDQ}/2.
4) All AC timing characteristics assume an input slew rate of 1.0 V/ns.
5) The output timing reference level is V_{DDQ}/2.
6) Parameters t_{ac} and t_{DQSCK} are specified for full drive strength and a reference load as shown below. This circuit is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. For half drive strength with a nominal load of 10pF parameters t_{AC} and t_{DQSCK} are expected to be in the same range. However, these parameters are not subject to production test but are estimated by device characterization. Use of IBIS or other simulation tools for system validation is suggested.



7) Min (t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).
8) t_{QH} = t_{HP} - t_{QHS}, where t_{HP} = minimum half clock period for any given cycle and is defined by clock high or clock low (t_{CL}, t_{CH}). t_{QHS} accounts for 1) the pulse duration distortion of on-chip clock circuits; and 2) the worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
9) The only time that the clock frequency is allowed to change is during power-down, self-refresh or clock stop modes.
10) DQ, DM and DQS input slew rate is measured between $V_{ILD(DC)}$ and $V_{IHD(AC)}$ (rising) or $V_{IHD(DC)}$ and $V_{ILD(AC)}$ (falling).
11) DQ, DM and DQS input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.
12) Input slew rate ≥ 1.0 V/ns..
13) Input slew rate ≥ 0.5V/ns and < 1.0 V/ns.
14) These parameters guarantee device timing. They are verified by device characterization but are not subject to production test.
15) The transition time for address and command inputs is measured between V_{IH} and V_{IL}.
16) A CK/$\overline{CK}$ differential slew rate of 2.0 V/ns is assumed for this parameter.
17) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
18) t_{DQSQ} consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
19) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.
20) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

21) A low level on DQS may be maintained during High-Z states (DQS drivers disabled) by adding a weak pull-down element in the system. It is recommended to turn off the weak pull-down element during read and write bursts (DQS drivers enabled).

22) These parameters account for the number of clock cycles and depend on the operating frequency, as follows: *no. of clock cycles = specified delay / clock period ; round to the next higher integer*.

23) t_{DAL} = (t_{WR} / t_{CK}) + (t_{RP} / t_{CK}): for each of the terms above, if not already an integer, round to the next higher integer.

24) A maximum of eight AUTOREFRESH commands can be posted to the DDR Mobile-RAM device, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 8 * tREFI.

Table 12 Output Slew Rate Characteristics [1)]

Parameter	Typical Range	Minimum	Maximum	Unit	Notes
Pullup and Pulldown Slew Rate (Full Drive Buffer)	TBD	0.7	2.5	V/ns	2)
Pullup and Pulldown Slew Rate (Half Drive Buffer)	TBD	0.3	1.0	V/ns	2)
Output Slew Rate Matching Ratio (Pullup to Pulldown)	-	0.7	1.4	-	3)

1) Output slew rate is measured between $V_{ILD(DC)}$ and $V_{IHD(AC)}$ (rising) or $V_{IHD(DC)}$ and $V_{ILD(AC)}$ (falling).

2) The parameter is measured using a 20pF capacitive load connected to VSSQ.

3) The ratio of the pullup slew rate to the pulldown slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

Table 13 AC Overshoot / Undershoot Specification

Parameter	Maximum	Unit	Notes
Maximum peak amplitude allowed for overshoot	0.9	V	–
Maximum peak amplitude allowed for undershoot	0.9	V	–
Maximum overshoot area above VDD	3.0	V-ns	–
Maximum undershoot area below VSS	3.0	V-ns	–

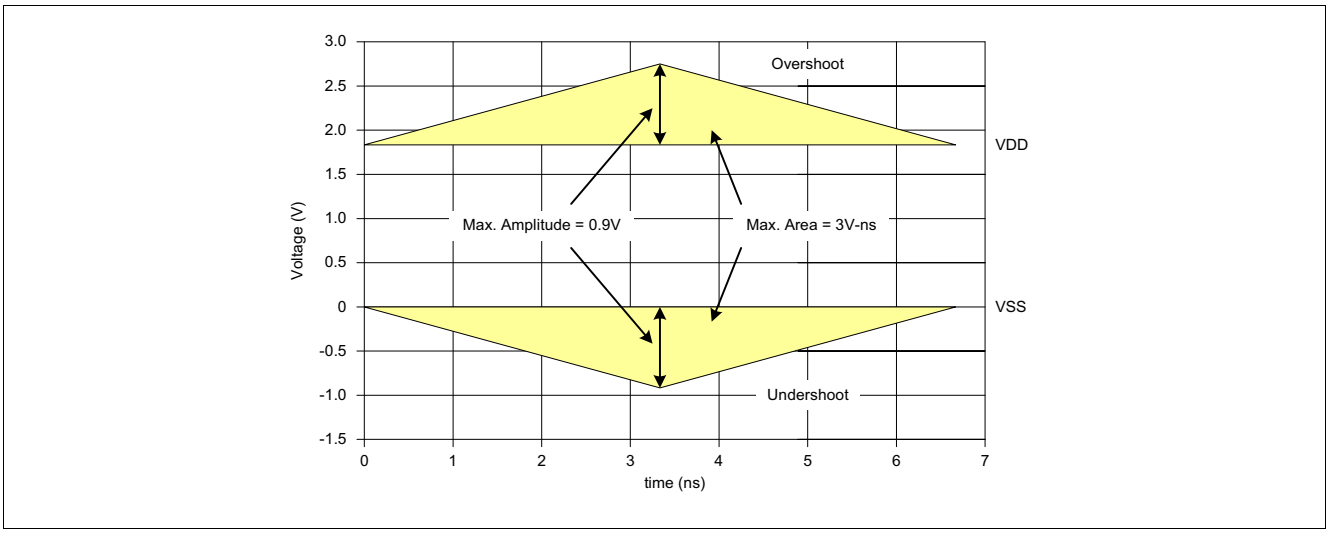


Figure 3 AC Overshoot and Undershoot Definition

3.3 Operating Currents

Table 14 Maximum Operating Currents[1)2)3)4)5)]

Parameter & Test Conditions	Symbol	Values		Unit
		- 6	- 7.5	
Operating one bank active-precharge current: $t_{RC} = t_{RCmin}$; $t_{CK} = t_{CKmin}$; CKE is HIGH; $\overline{CS}$ is HIGH between valid commands; address inputs are SWITCHING; data bus inputs are STABLE	I_{DD0}	70	50	mA
Precharge power-down standby current: all banks idle, CKE is LOW; $\overline{CS}$ is HIGH, $t_{CK} = t_{CKmin}$; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD2P}	0.70	0.70	mA
Precharge power-down standby current with clock stop: all banks idle, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD2PS}	0.60	0.60	mA
Precharge non power-down standby current: all banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, $t_{CK} = t_{CKmin}$; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD2N}	18	15	mA
Precharge non power-down standby current with clock stop: all banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD2NS}	1.5	1.5	mA
Active power-down standby current: one bank active, CKE is LOW; $\overline{CS}$ is HIGH, $t_{CK} = t_{CKmin}$; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD3P}	2	2	mA
Active power-down standby current with clock stop: one bank active, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD3PS}	1.5	1.5	mA
Active non power-down standby current: one bank active, CKE is HIGH; $\overline{CS}$ is HIGH, $t_{CK} = t_{CKmin}$; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD3N}	25	22	mA
Active non power-down standby current with clock stop: one bank active, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD3NS}	2.5	2.5	mA
Operating burst read current: one bank active; BL = 4; CL = 3; $t_{CK} = t_{CKmin}$; continuous read bursts; I_{OUT} = 0 mA; address inputs are SWITCHING; 50% data change each burst transfer	I_{DD4R}	105	75	mA
Operating burst write current: one bank active; BL = 4; $t_{CK} = t_{CKmin}$; continuous write bursts; address inputs are SWITCHING; 50% data change each burst transfer	I_{DD4W}	110	75	mA
Auto-Refresh current: $t_{RC} = t_{RFCmin}$; $t_{CK} = t_{CKmin}$; burst refresh; CKE is HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD5}	185	135	mA
Self refresh current: CKE is LOW; CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are STABLE; data bus inputs are STABLE	I_{DD6}	see Table 15		µA
Deep Power Down current	I_{DD8}	25[6)]		µA

1) 0 °C ≤ T_C ≤ 70 °C (comm.); -25 °C ≤ T_C ≤ 85 °C (ext.); V_{DD} = V_{DDQ} = 1.70 V - 1.90 V. Recommended Operating Conditions unless otherwise noted

2) IDD specifications are tested after the device is properly intialized and measured at 133 MHz for -7.5 and 166 MHz for -6 speed grade.

3) Input slew rate is 1.0 V/ns.
4) Definitions for IDD:
   LOW is defined as $V_{IN} \leq 0.1 * V_{DDQ}$;
   HIGH is defined as $V_{IN} \geq 0.9 * V_{DDQ}$;
   STABLE is defined as inputs stable at a HIGH or LOW level;
   SWITCHING is defined as:
   - address and command: inputs changing between HIGH and LOW once per two clock cycles;
   - data bus inputs: DQ changing between HIGH and LOW once per clock cycle; DM and DQS are STABLE
5) All parameters are measured with no output loads.
6) I_{DD8} current is typical.

Table 15 Self Refresh Currents

Parameter & Test Conditions	Max. Temperature	Symbol	Values		Units	Notes 1)2)3)
			typ.	max.		
Self Refresh Current: Self refresh mode, full array activation (PASR = 000)	85 °C	I_{DD6}	710	900	µA	–
	70 °C		510	–		
	45 °C		320	–		
	25 °C		280	–		
Self Refresh Current: Self refresh mode, half array activation (PASR = 001)	85 °C		540	780		
	70 °C		370	–		
	45 °C		240	–		
	25 °C		210	–		
Self Refresh Current: Self refresh mode, quarter array activation (PASR = 010)	85 °C		420	670		
	70 °C		290	–		
	45 °C		210	–		
	25 °C		170	–		

1) 0 °C ≤ T_C ≤ 70 °C (comm.); -25 °C ≤ T_C ≤ 85 °C (ext.); V_{DD} = V_{DDQ} = 1.70 V - 1.90 V.
2) The On-Chip Temperature Sensor (OCTS) adjusts the refresh rate in self refresh mode to the component's actual temperature with a much finer resolution than supported by the 4 imperature levels as defined by JEDEC for TCSR. At production test the sensor is calibrated, and IDD6 max. current is measured at 85°C. Typ. values are obtained from device characterization.
3) For commercial temperature range part (HYB), the max. value indicated for 85°C applies to 70°C.

3.4 Pullup and Pulldown Characteristics

Table 16 Full Drive Strength and Half Drive Strength[1)]

Voltage (V)	Full Drive Strength				Half Drive Strength			
	PD Current (mA)		PU Current (mA)		PD Current (mA)		PU Current (mA)	
	min.	max.	min.	max.	min.	max.	min.	max.
0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.10	2.80	18.53	-2.80	-18.53	1.27	8.42	-1.27	-8.42
0.20	5.60	26.80	-5.60	-26.80	2.55	12.30	-2.55	-12.30
0.30	8.40	32.80	-8.40	-32.80	3.82	14.95	-3.82	-14.95
0.40	11.20	37.05	-11.20	-37.05	5.09	16.84	-5.09	-16.84
0.50	14.00	40.00	-14.00	-40.00	6.36	18.20	-6.36	-18.20
0.60	16.80	42.50	-16.80	-42.50	7.64	19.30	-7.64	-19.30
0.70	19.60	44.57	-19.60	-44.57	8.91	20.30	-8.91	-20.30
0.80	22.40	46.50	-22.40	-46.50	10.16	21.20	-10.16	-21.20
0.85	23.80	47.48	-23.80	-47.48	10.80	21.60	-10.80	-21.60
0.90	23.80	48.50	-23.80	-48.50	10.80	22.00	-10.80	-22.00
0.95	23.80	49.40	-23.80	-49.40	10.80	22.45	-10.80	-22.45
1.00	23.80	50.05	-23.80	-50.05	10.80	22.73	-10.80	-22.73
1.10	23.80	51.35	-23.80	-51.35	10.80	23.21	-10.80	-23.21
1.20	23.80	52.65	-23.80	-52.65	10.80	23.67	-10.80	-23.67
1.30	23.80	53.95	-23.80	-53.95	10.80	24.14	-10.80	-24.14
1.40	23.80	55.25	-23.80	-55.25	10.80	24.61	-10.80	-24.61
1.50	23.80	56.55	-23.80	-56.55	10.80	25.08	-10.80	-25.08
1.60	23.80	57.85	-23.80	-57.85	10.80	25.54	-10.80	-25.54
1.70	23.80	59.15	-23.80	-59.15	10.80	26.01	-10.80	-26.01
1.80		60.45		-60.45		26.48		-26.48
1.90		61.75		-61.75		26.95		-26.95

1) Above characteristics are specified under best and worst process variation / condition.
Temperature (T_{case}): Minimum = 0 °C / -25°C, Maximum = 70°C / 85°C V_{DDQ}: Minimum = 1.70 V, Maximum = 1.90 V

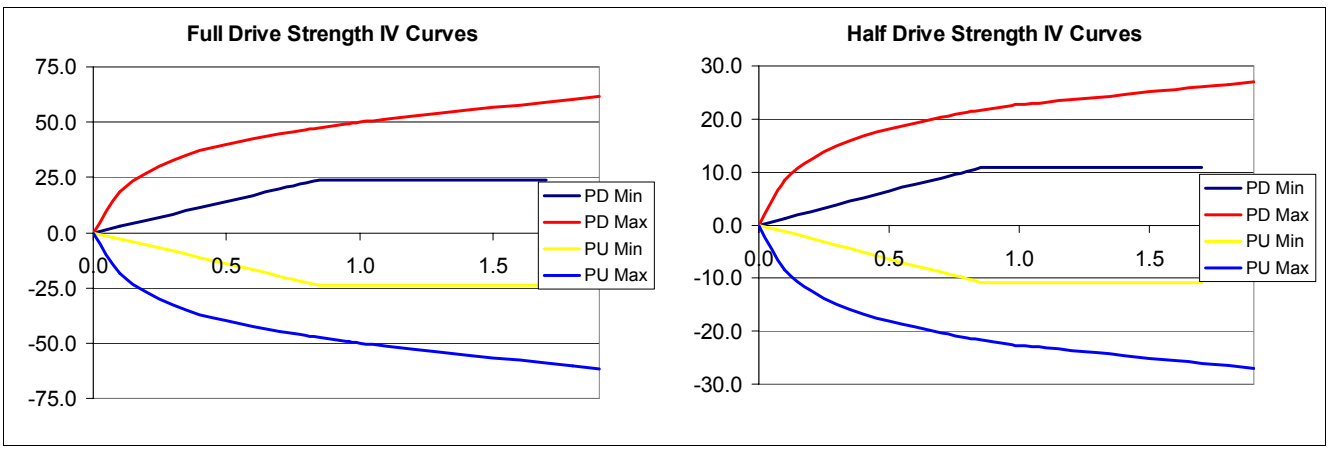


Figure 4 Full Drive Strength and Half Drive Strength

4 Package Outlines

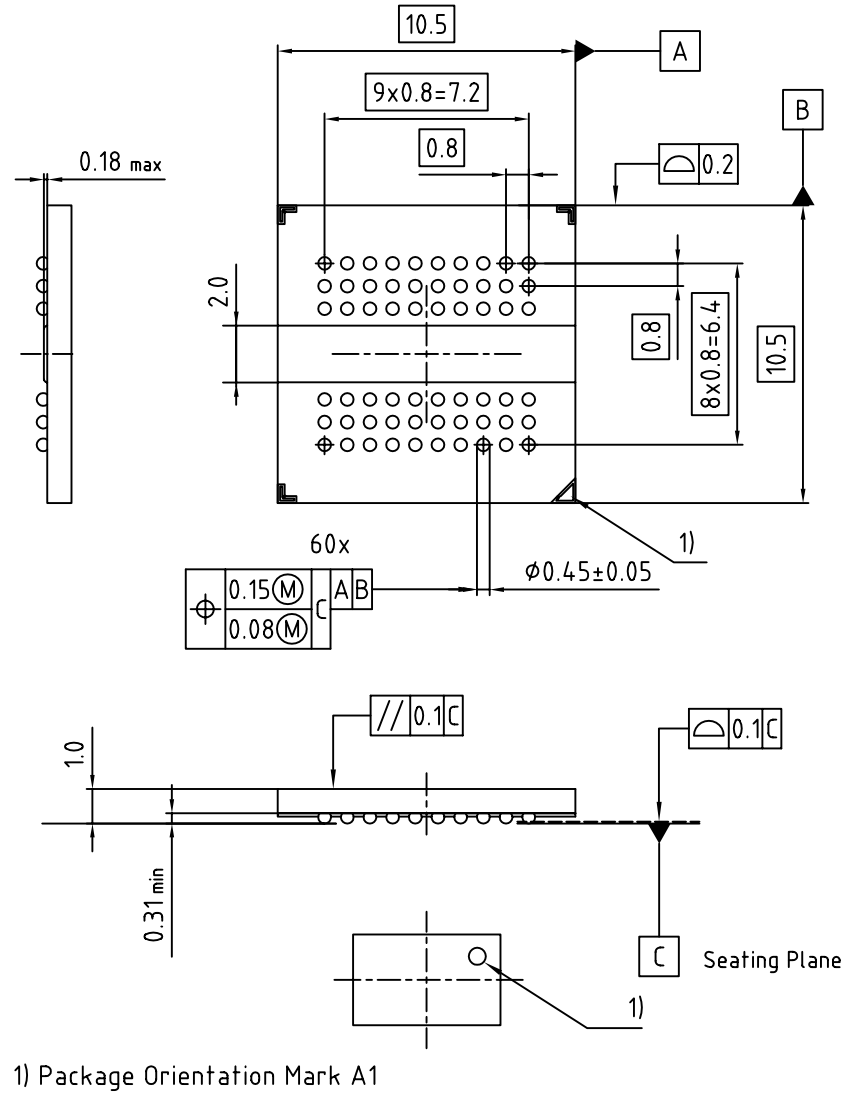


Figure 5 **P-VFBGA-60-1** (Plastic Very Thin Fine Ball Grid Array Package)

You can find all of our packages, sorts of packing and others in our Qimonda Internet Page “Products”: **http://www.qimonda.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

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