LSI/CSI

LS7083N
LS7084N

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QUADRATURE CLOCK CONVERTER

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FEATURES:
- x1 and x4 mode selection
- Up to 16MHz output clock frequency
- Programmable output clock pulse width
- On-chip filtering of inputs for optical or magnetic encoder applications.
- TTL and CMOS compatible I/Os
- +3V to +12V operation (V_{DD} - V_{SS})
- **LS7083N**, **LS7084N** (DIP); **LS7083N**-S, **LS7084N**-S (SOIC) - See Figure 1

Applications:
- Interface incremental encoders to Up / Down Counters (See Figure 6A and Figure 6B)
- Interface rotary encoders to Digital Potentiometers (See Figure 7)

DESCRIPTION:
The **LS7083N** and **LS7084N** are CMOS quadrature clock converters. Quadrature clocks derived from optical or magnetic encoders, when applied to the A and B inputs of the **LS7083N** or **LS7084N**, are converted to strings of Up Clocks and Down Clocks (**LS7083N**) or to a Clock and an Up/Down direction control (**LS7084N**). These outputs can be interfaced directly with standard Up/Down counters for direction and position sensing of the encoder.

INPUT/OUTPUT DESCRIPTION:

RBIAS (Pin 1)
Input for external component connection. A resistor connected between this input and V_{SS} adjusts the output clock pulse width (Tow). For proper operation, the output clock pulse width must be less than or equal to the A, B pulse separation ($T_{OW} \leq T_{PS}$).

V_{DD} (Pin 2)
Supply Voltage positive terminal.

V_{SS} (Pin 3)
Supply Voltage negative terminal**.**

A (Pin 4)
Quadrature Clock Input A. This input has a filter circuit to validate input logic level and eliminate encoder dither.

B (Pin 5)
Quadrature Clock Input B. This input has a filter circuit identical to input A.

Mode (Pin 6)
Mode is a 3-state input to select resolutions x1, x2 or x4. The selected resolution multiplies the input quadrature clock rate by 1, 2 and 4, respectively, in producing the outputs UPCK / DNCK and CLK (see Figure 2).

The Mode input logic levels selects resolutions as follows:
Logic 0 = x1 Float = x2 Logic 1 = x4

PIN ASSIGNMENT - TOP VIEW

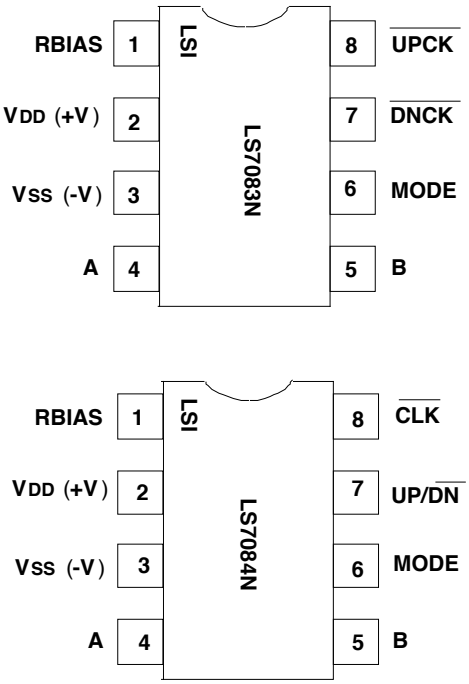


FIGURE 1

LS7083N - $\overline{\text{DNCK}}$ (Pin 7)
In **LS7083N**, this is the DOWN Clock Output. This output consists of low-going pulses generated when A input lags the B input.

LS7084N - UP/$\overline{\text{DN}}$ (Pin 7)
In **LS7084N**, this is the count direction indication output. When A input leads the B input, the UP/$\overline{\text{DN}}$ output goes high indicating that the count direction is UP. When A input lags the B input, UP/$\overline{\text{DN}}$ output goes low, indicating that the count direction is DOWN.

LS7083N - $\overline{\text{UPCK}}$ (Pin 8)
In **LS7083N**, this is the UP Clock output. This output consists of low-going pulses generated when A input leads the B input.

LS7084N - $\overline{\text{CLK}}$ (Pin 8)
In **LS7084N**, this is the combined UP Clock and DOWN Clock output. The count direction at any instant is indicated by the UP/$\overline{\text{DN}}$ output (Pin 7).

NOTE: For the **LS7084N**, the timing of $\overline{\text{CLK}}$ and UP/$\overline{\text{DN}}$ requires that the counter interfacing with **LS7084N** counts on the rising edge of the $\overline{\text{CLK}}$ pulses.

ABSOLUTE MAXIMUM RATINGS:

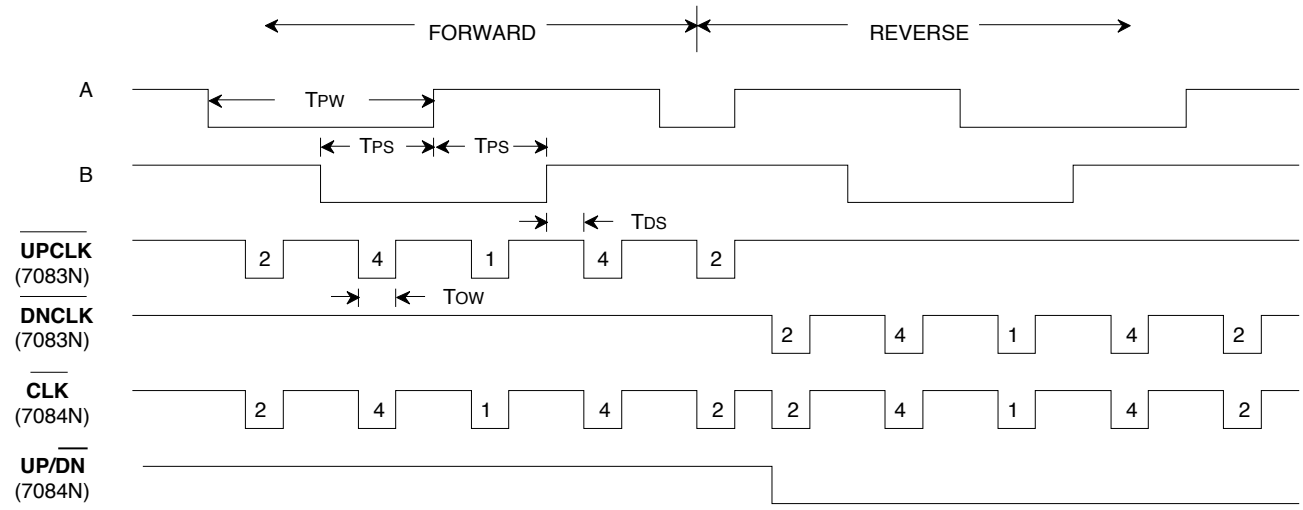
PARAMETER	SYMBOL	VALUE	UNITS
DC Supply Voltage	V_{DD} - V_{SS}	16.0	V
Voltage at any input	V_{IN}	V_{SS} - 0.3 to V_{DD} + 0.3	V
Operating temperature	T_A	0 to +70	°C
Storage temperature	T_{STG}	-55 to +150	°C

DC ELECTRICAL CHARACTERISTICS:
(V_{SS}, T_A = 0°C to 70°C.)

PARAMETER	SYMBOL	MIN	MAX	UNITS	CONDITION
Supply voltage	V_{DD}	3.0	12.0	V	-
Supply current	I_{DD}	-	10.0	μA	V_{DD} = 12V, All input frequencies = 0Hz RBIAS = 2MΩ
MODE Logic Low	V_{IL}	-	0.5V_{DD}	V	
A, B Logic Low	V_{IL}	-	0.7	V	V_{DD} = 3V
		-	1.0	V	V_{DD} = 5V
		-	2.8	V	V_{DD} = 12V
MODE Logic High	V_{IH}	V_{DD} - 0.5	-	V	-
A, B Logic High	V_{IH}	2.0	-	V	V_{DD} = 3V
		3.0	-	V	V_{DD} = 5V
		6.6	-	V	V_{DD} = 12V
ALL OUTPUTS:					
Sink Current	I_{OL}	1.3	-	mA	V_{DD} = 3V
V_{OL} = 0.4V		1.9	-	mA	V_{DD} = 5V
		2.9	-	mA	V_{DD} = 12V
Source Current	I_{OH}	0.83	-	mA	V_{DD} = 3V
V_{OH} = V_{DD} - 0.5V		1.1	-	mA	V_{DD} = 5V
		1.6	-	mA	V_{DD} = 12V

TRANSIENT CHARACTERISTICS:
(T_A = 0°C to 70°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	CONDITION
A, B inputs:					
Validation Delay	T_{VD}	-	250	ns	V_{DD} = 3V
		-	170	ns	V_{DD} = 5V
		-	71	ns	V_{DD} = 12V
A, B inputs:					
Pulse Width	T_{PW}	T_{VD} + T_{OW}	Infinite	ns	-
A to B or **B to A**					
Phase Delay	T_{PS}	T_{OW}	Infinite	ns	-
A, B frequency	$f_{A, B}$	-	$\frac{1}{2T_{PW}}$	Hz	-
Input to Output Delay	T_{DS}	-	280	ns	V_{DD} = 3V
		-	220	ns	V_{DD} = 5V
		-	120	ns	V_{DD} = 12V Includes input validation delay
Output Clock Pulse Width	T_{OW}	50	-	ns	See Fig. 4 & 5



NOTE: Output clocks labeled 1, 2 and 4 have the following interpretations.

1. Generated in x1, x2 and x4 modes.
2. Generated in x2 and x4 modes only.
3. Generated in x4 mode only.

FIGURE 2. LS7083N / LS7084N INPUT / OUTPUT TIMING

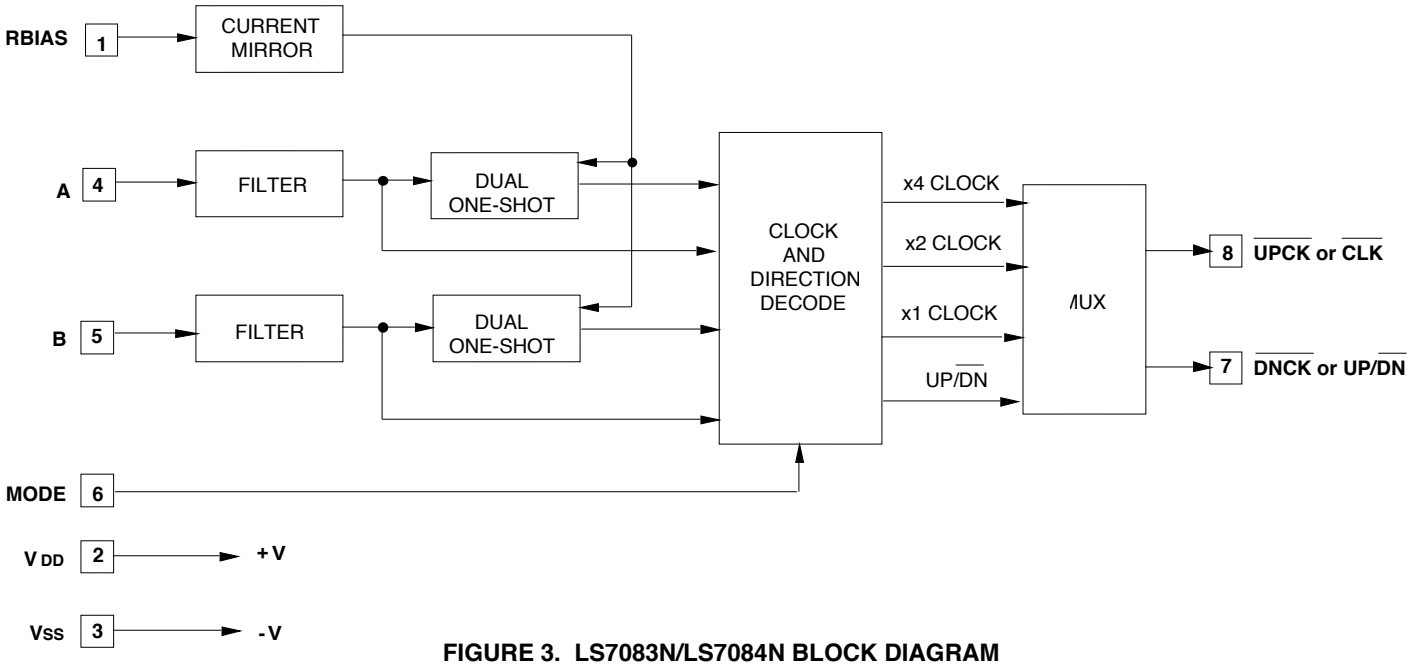


FIGURE 3. LS7083N/LS7084N BLOCK DIAGRAM

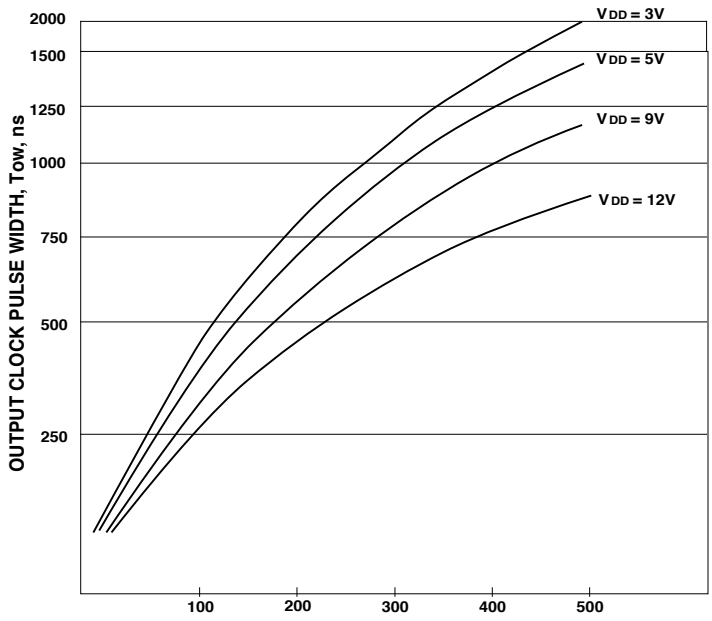


Figure 4. Tow vs RBIAS, kΩ

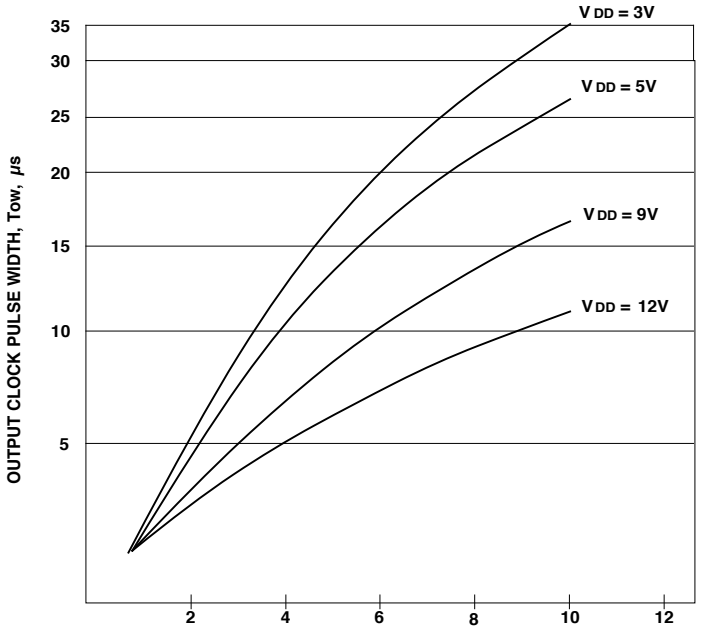


Figure 5. Tow vs RBIAS, MΩ

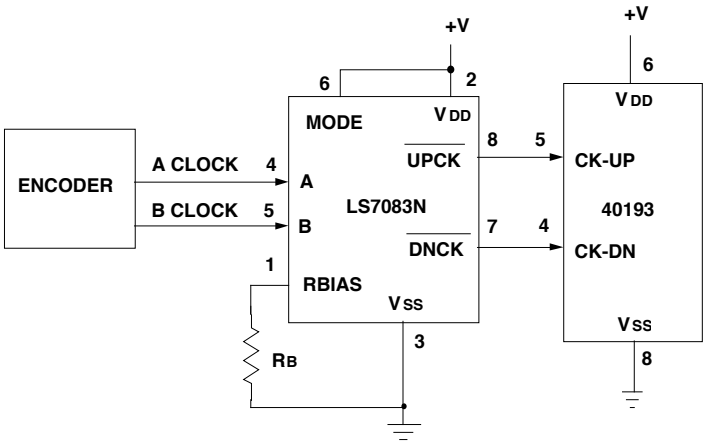


FIGURE 6A. TYPICAL APPLICATION FOR LS7083N in x4 MODE

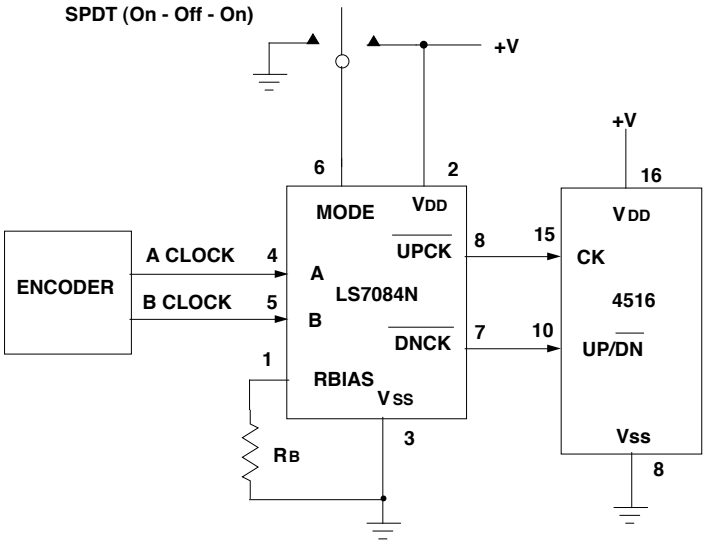
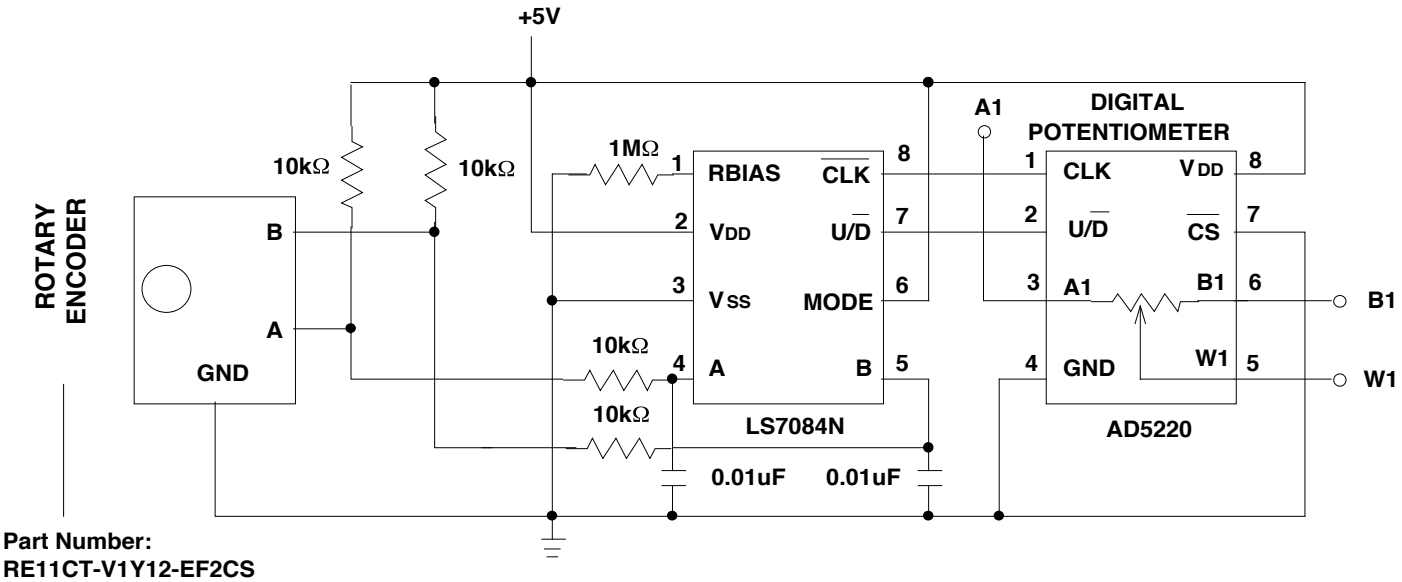


FIGURE 6B*. TYPICAL APPLICATION FOR LS7084N in x2 MODE

*See NOTE at bottom right of Page 1



Part Number:
RE11CT-V1Y12-EF2CS

FIGURE 7. Rotary Encoder Control of Digital Potentiometer