FAIRCHILD SEMICONDUCTOR®

June 2006

# FHP3350, FHP3450
# Triple and Quad Voltage Feedback Amplifiers

## Features at ±5V

- 0.1dB gain flatness to 30MHz
- 0.07%/0.03˚ differential gain/phase error
- 210MHz full power -3dB bandwidth at G = 2
- 1,100V/µs slew rate
- ±55mA output current (drives dual video load)
- ±83mA output short circuit current
- Output swings to within 1.3V of either rail
- 3.6mA supply current per amplifier
- Minimum stable gain of 3dB or 1.5V/V
- FHP3350 - improved replacement for RC6333
- FHP3450 - improved replacement for RC6334
- Fully specified at +5V, and ±5V supplies

## Applications

- Video driver
- RGB driver
- ADC buffer
- S-video amp
- Active Filters

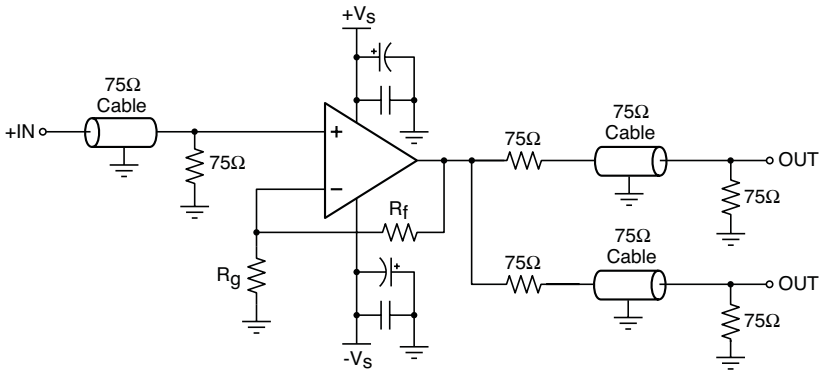
## Description

The FHP3350 and FHP3450 are low cost, high performance, voltage feedback amplifiers designed for video applications. These triple and quad amplifiers consume only 3.6mA of supply current per channel and are capable of driving dual (75Ω) video loads while providing 0.1dB of gain flatness to 30MHz. Consumer video applications will also benefit from their low 0.07% differential gain and 0.03˚ differential phase errors. The FHP3350 offers three outputs that can be put into a high impedance disable state to allow for video multiplexing or minimize power consumption.

These amplifiers are designed to operate from 5V (±2.5V) to 12V (±6V) supplies. The outputs swing to within 1.3V of either supply rail to accommodate video signals on a single 5V supply.

The FHP3350 and FHP3450 are designed on a complementary bipolar process. They provide 210MHz of full power bandwidth and 1,100V/µs of slew rate at a supply voltage of ±5V. The combination of high performance, low power, and excellent video performance make these amplifiers well suited for use in many digital consumer video appliances as well as many general purpose high speed applications.

## Typical Application – Driving Dual Video Loads

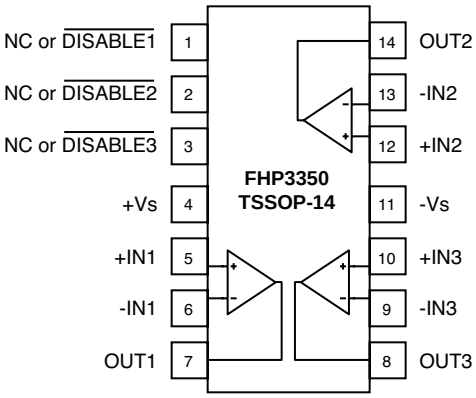



## Ordering Information

| Part Number | Package | Lead Free | Operating Temp Range | Packaging Method |
|---|---|---|---|---|
| FHP3350IMTC14X | TSSOP-14 | Yes | -40°C to +85°C | Reel |
| FHP3350IM14X | SOIC-14 | Yes | -40°C to +85°C | Reel |
| FHP3450IMTC14X | TSSOP-14 | Yes | -40°C to +85°C | Reel |
| FHP3450IM14X | SOIC-14 | Yes | -40°C to +85°C | Reel |

Moisture sensitivity level for all parts is MSL-1.

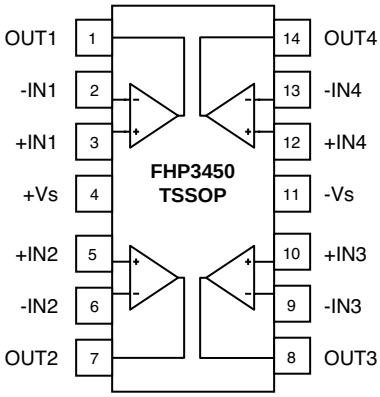
## FHP3350 Pin Configurations




## FHP3350 Pin Assignments

| Pin# | Pin | Description |
|---|---|---|
| 1 | NC or $\overline{\text{DISABLE1}}$ | Channel 1 ENABLED if pin is left open or pulled above $V_{ON}$, DISABLED if pin is grounded or pulled below $V_{OFF}$ |
| 2 | NC or $\overline{\text{DISABLE2}}$ | Channel 2 ENABLED if pin is left open or pulled above $V_{ON}$, DISABLED if pin is grounded or pulled below $V_{OFF}$ |
| 3 | NC or $\overline{\text{DISABLE3}}$ | Channel 3 ENABLED if pin is left open or pulled above $V_{ON}$, DISABLED if pin is grounded or pulled below $V_{OFF}$ |
| 4 | +Vs | Positive supply |
| 5 | +IN1 | Positive Input, channel 1 |
| 6 | -IN1 | Negative Input, channel 1 |
| 7 | OUT1 | Output, channel 1 |
| 8 | OUT3 | Output, channel 3 |
| 9 | -IN3 | Negative Input, channel 3 |
| 10 | +IN3 | Positive Input, channel 3 |
| 11 | -Vs | Negative supply |
| 12 | +IN2 | Positive Input, channel 2 |
| 13 | -IN2 | Negative Input, channel 2 |
| 14 | OUT2 | Output, channel 2 |

## FHP3450 Pin Configurations




## FHP3450 Pin Assignments

| Pin# | Pin | Description |
|---|---|---|
| 1 | OUT1 | Output, channel 1 |
| 2 | -IN1 | Negative Input, channel 1 |
| 3 | +IN1 | Positive Input, channel 1 |
| 4 | +Vs | Positive supply |
| 5 | +IN2 | Positive Input, channel 2 |
| 6 | -IN2 | Negative Input, channel 2 |
| 7 | OUT2 | Output, channel 2 |
| 8 | OUT3 | Output, channel 3 |
| 9 | -IN3 | Negative Input, channel 3 |
| 10 | +IN3 | Positive Input, channel 3 |
| 11 | -Vs | Negative supply |
| 12 | +IN4 | Positive Input, channel 4 |
| 13 | -IN4 | Negative Input, channel 4 |
| 14 | OUT4 | Output, channel 4 |

## Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table defines the conditions for actual device operation.

| Parameter | Min. | Max. | Unit |
|---|---|---|---|
| Supply Voltage | 0 | 12.6 | V |
| Input Voltage Range | $-V_S$ - 0.5V | $+V_S$ +0.5V | V |

## Reliability Information

| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| Junction Temperature | | | 150 | ˚C |
| Storage Temperature Range | -65 | | 150 | ˚C |
| Lead Temperature (Soldering, 10s) | | | 300 | ˚C |
| 14-Lead TSSOP[1] | | 160 | | ˚C/W |
| 14-Lead SOIC[1] | | 148 | | ˚C/W |

Note:

1. Package thermal resistance ($\theta_{JA}$), JDEC standard, multi-layer test boards, still air. Assumed power is concentrated in one channel $\theta_{JA}$ will be lower, if power is distributed in all channels.

## ESD Protection

| ESD Protection | FHP3350 | | FHP3450 | |
|---|---|---|---|---|
| Package | SOIC | TSSOP | SOIC | TSSOP |
| Human Body Model (HBM) | 1500V | 1500V | 2000V | 2000V |
| Charged Device Model (CDM) | 2000V | 1500V | 2000V | 1500V |

## Recommended Operating Conditions

| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| Operating Temperature Range | -40 | | +85 | ˚C |
| Supply Voltage Range | 3 | | 12 | V |

## Electrical Characteristics at +5V

$T_c$ = 25˚C, $V_S$ = 5V, $R_f$ = 249Ω, $R_L$ = 150Ω to $V_S$/2, G = 2; unless otherwise noted.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | **Frequency Domain Response** | | | | | |
| $BW_{ss}$ | -3dB Bandwidth | No Peaking, G = +2, $V_{OUT}$ = 0.2$V_{pp}$ | | 190 | | MHz |
| $BW_{Ls}$ | Full Power Bandwidth | No Peaking, G = +2, $V_{OUT}$ = 2$V_{pp}$ | | 190 | | MHz |
| $BW_{0.1dB}$ | 0.1dB Gain Flatness - Large Signal | G = +2, $V_{OUT}$ = 2$V_{pp}$ | | 35 | | MHz |
| | **Time Domain Response** | | | | | |
| $t_R$, $t_F$ | Rise and Fall Time | $V_{OUT}$ = 0.2V step | | 2.0 | | ns |
| $t_S$ | Settling Time to 0.1% | $V_{OUT}$ = 2V step | | 20 | | ns |
| OS | Overshoot | $V_{OUT}$ = 0.2V step | | 2.5 | | % |
| SR | Slew Rate | 2V step. G = -1 | | 800 | | V/µs |
| | **Distortion / Noise Response** | | | | | |
| HD2 | 2nd Harmonic Distortion | $V_{OUT}$ = 2$V_{pp}$, 5MHz | | -70 | | dBc |
| HD3 | 3rd Harmonic Distortion | $V_{OUT}$ = 2$V_{pp}$, 5MHz | | -80 | | dBc |
| THD | Total Harmonic Distortion | $V_{OUT}$ = 2$V_{pp}$, 5MHz | | -69 | | dB |
| DG | Differential Gain | NTSC (3.58MHz); AC coupled | | 0.08 | | % |
| DP | Differenital Phase | NTSC (3.58MHz); AC coupled | | 0.02 | | ˚ |
| $e_n$ | Input Voltage Noise | > 100kHz | | 8.5 | | nV/Hz |
| $i_n$ | Input Current Noise | > 100kHz | | 1 | | pA/Hz |
| $X_{TALK}$ | Crosstalk | at 5MHz | | -70 | | dB |
| | **DC Performance** | | | | | |
| $V_{IO}$ | Input Offset Voltage | | | 1 | | mV |
| $dV_{IO}$ | Average Drift | | | 10 | | µV/˚C |
| $I_{bn}$ | Input Bias Current | | | ±50 | | nA |
| $dI_{bn}$ | Average Drift | | | 0.33 | | nA/˚C |
| $I_{IO}$ | Input Offset Current | | | ±50 | | nA |
| PSRR | Power Supply Rejection Ratio | DC | | 75 | | dB |
| $A_{OL}$ | Open Loop Gain | DC | | 55 | | dB |
| $I_S$ | Supply Current per Amplifier | | | 3.0 | | mA |
| $I_{SD}$ | Disable Supply Current per Amp | Disable Mode | | 35 | | µA |
| | **Disable Characteristics** | | | | | |
| $OFF_{ISO}$ | Off Isolation | 5MHz | | -60 | | dB |
| $OFFC_{OUT}$ | Off Output Capacitance | | | 3 | | pF |
| $CH_{ISO}$ | Channel-to-Channel Isolation | 5MHz | | -85 | | dB |
| $T_{ON}$ | Turn on time | | | 300 | | ns |
| $T_{OFF}$ | Turn off time | | | 80 | | ns |
| $V_{OFF}$ | Power Down Input Voltage | $\overline{\text{DISABLE}}$ pins; disabled if pin is grounded or pulled below $V_{OFF}$ | | | $+V_s$ - 3.1 | V |
| $V_{ON}$ | Enable Input Voltage | $\overline{\text{DISABLE}}$ pins; enabled if pin is left open or pulled above $V_{ON}$ | $+V_s$ - 1.9 | | | V |

## Electrical Characteristics at +5V (Continued)

$T_c$ = 25˚C, $V_S$ = 5V, $R_f$ = 249Ω, $R_L$ = 150Ω to $V_S$/2, G = 2; unless otherwise noted.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | **Input Characteristics** | | | | | |
| $R_{IN}$ | Input Resistance | | | 70 | | MΩ |
| $C_{IN}$ | Input Capacitance | | | 1 | | pF |
| CMIR | Input Common Mode Voltage Range | | | 1.2 to 3.8 | | V |
| CMRR | Common Mode Rejection Ratio | DC, $V_{CM}$ = 1.5V to 3.5V | | 90 | | dB |
| | **Output Characteristics** | | | | | |
| $V_O$ | Output Voltage Swing | $R_L$ = 2kΩ to $V_S$/2 | | 1 to 4 | | V |
| | | $R_L$ = 150Ω to $V_S$/2 | | 1.1 to 3.9 | | V |
| $I_{OUT}$ | Linear Output Current | $V_O$ = +$V_S$/2 | | ±50 | | mA |
| $I_{SC}$ | Short Circuit Output Current | $V_O$ = shorted to +$V_S$ or GND | | ±75 | | mA |

## Electrical Characteristics at ±5V

$T_c$ = 25˚C, $V_S$ = ±5V, $R_f$ = 249Ω, $R_L$ = 150Ω to GND, G = 2; unless otherwise noted.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | **Frequency Domain Response** | | | | | |
| $BW_{ss}$ | -3dB Bandwidth | No Peaking, G = +2, $V_{OUT}$ = 0.2$V_{pp}$ | | 210 | | MHz |
| $BW_{Ls}$ | Full Power Bandwidth | No Peaking, G = +2, $V_{OUT}$ = 2$V_{pp}$ | | 210 | | MHz |
| $BW_{0.1dB}$ | 0.1dB Gain Flatness - Large Signal | G = +2, $V_{OUT}$ = 2$V_{pp}$ | | 30 | | MHz |
| $BW_{0.1dBss}$ | 0.1dB Gain Flatness - Small Signal | G = +2, $V_{OUT}$ = 0.2$V_{pp}$ | | 50 | | MHz |
| | **Time Domain Response** | | | | | |
| $t_R$, $t_F$ | Rise and Fall Time | $V_{OUT}$ = 0.2V step | | 2 | | ns |
| $t_S$ | Settling Time to 0.1% | $V_{OUT}$ = 2V step | | 20 | | ns |
| OS | Overshoot | $V_{OUT}$ = 0.2V step | | 1 | | % |
| SR | Slew Rate | 2V step. G = -1 | | 1100 | | V/µs |
| | **Distortion / Noise Response** | | | | | |
| HD2 | 2nd Harmonic Distortion | $V_{OUT}$ = 2$V_{pp}$, 5MHz | | -70 | | dBc |
| HD3 | 3rd Harmonic Distortion | $V_{OUT}$ = 2$V_{pp}$, 5MHz | | -74 | | dBc |
| THD | Total Harmonic Distortion | $V_{OUT}$ = 2$V_{pp}$, 5MHz | | -68 | | dB |
| DG | Differential Gain | NTSC (3.58MHz); AC coupled | | 0.07 | | % |
| DP | Differenital Phase | NTSC (3.58MHz); AC coupled | | 0.03 | | ° |
| $e_n$ | Input Voltage Noise | > 100kHz | | 9 | | nV/Hz |
| $i_n$ | Input Current Noise | > 100kHz | | 1 | | pA/Hz |
| $X_{TALK}$ | Crosstalk | at 5MHz | | -71 | | dB |
| | **DC Performance** | | | | | |
| $V_{IO}$ | Input Offset Voltage[1] | | -7 | 1 | 7 | mV |
| $dV_{IO}$ | Average Drift | | | 15 | | µV/˚C |
| $I_{bn}$ | Input Bias Current[1] | | -500 | ±100 | 500 | nA |
| $dI_{bn}$ | Average Drift | | | 0.3 | | nA/˚C |
| $I_{IO}$ | Input Offset Current[1] | | -500 | ±50 | 500 | nA |
| PSRR | Power Supply Rejection Ratio[1] | DC | 58 | 75 | | dB |
| $A_{OL}$ | Open Loop Gain[1] | DC | 52 | 58 | | dB |
| $I_S$ | Supply Current per Amplifier[1] | | | 3.6 | 5 | mA |
| $I_{SD}$ | Disable Supply Current per Amp[1] | Disable Mode | | 45 | 100 | µA |
| | **Disable Characteristics** | | | | | |
| $OFF_{ISO}$ | Off Isolation | 5MHz | | -65 | | dB |
| $OFFC_{OUT}$ | Off Output Capacitance | | | 3 | | pF |
| $CH_{ISO}$ | Channel-to-Channel Isolation | 5MHz | | -85 | | dB |
| $T_{ON}$ | Turn on time | | | 300 | | ns |
| $T_{OFF}$ | Turn off time | | | 80 | | ns |
| $V_{OFF}$ | Power Down Input Voltage | $\overline{\text{DISABLE}}$ pins; disabled if pin is grounded or pulled below $V_{OFF}$ | | | $+V_s$ - 3.1 | V |
| $V_{ON}$ | Enable Input Voltage | $\overline{\text{DISABLE}}$ pins; enabled if pin is left open or pulled above $V_{ON}$ | $+V_s$ - 1.9 | | | V |

**Notes:**

1. 100% tested at 25˚C

## Electrical Characteristics at ±5V (Continued)

$T_c$ = 25˚C, $V_s$ = ±5V, $R_f$ = 249Ω, $R_L$ = 150Ω to GND, G = 2; unless otherwise noted.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | **Input Characteristics** | | | | | |
| $R_{IN}$ | Input Resistance | | | 70 | | MΩ |
| $C_{IN}$ | Input Capacitance | | | 0.6 | | pF |
| CMIR | Input Common Mode Voltage Range | | | -3.8 to 3.8 | | V |
| CMRR | Common Mode Rejection Ratio[1] | DC, $V_{CM}$ = -3.5V to 3.5V | 58 | 98 | | dB |
| | **Output Characteristics** | | | | | |
| $V_O$ | Output Voltage Swing | $R_L$ = 2kΩ | | ±4 | | V |
| | | $R_L$ = 150Ω[1] | ±3.2 | ±3.7 | | V |
| $I_{OUT}$ | Linear Output Current | $V_o$ = 0V | | ±55 | | mA |
| $I_{SC}$ | Short Circuit Output Current | $V_O$ shorted to GND | | ±83 | | mA |

**Notes:**

1. 100% tested at 25˚C

## Typical Performance Characteristics

$T_c$ = 25˚C, $V_S$ = 5V, $R_f$ = 249Ω, $R_L$ = 150Ω to $V_S$/2, G = 2; unless otherwise noted.

**Figure 1. Non-Inverting Freq. Response (±5V)**

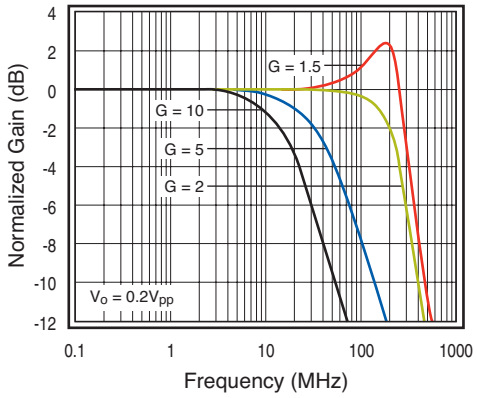



**Figure 2. Inverting Freq. Response (±5V)**

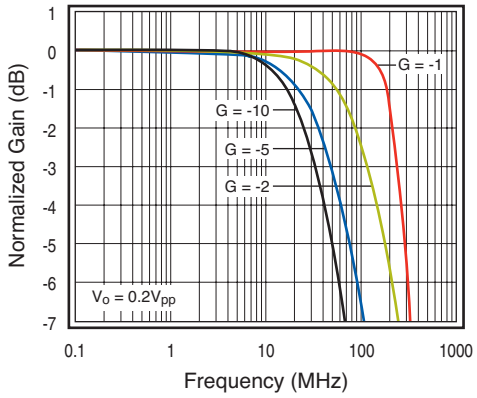



**Figure 3. Non-Inverting Freq. Response (+5V)**

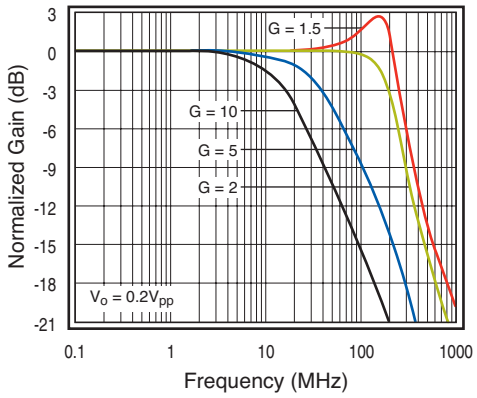



**Figure 4. Inverting Freq. Response (+5V)**

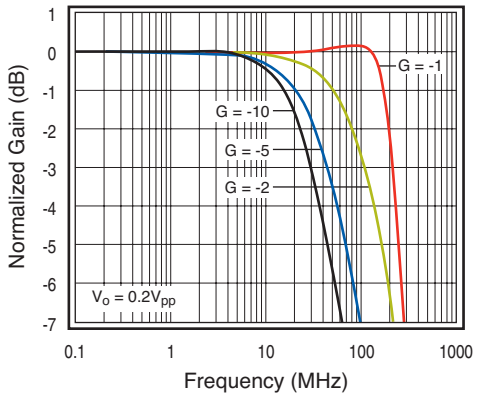



**Figure 5. Frequency Response vs. $C_L$ (+5V)**

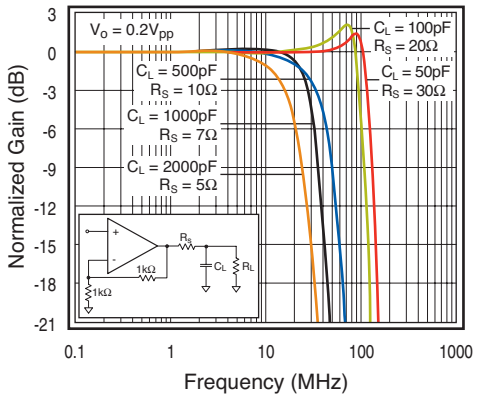
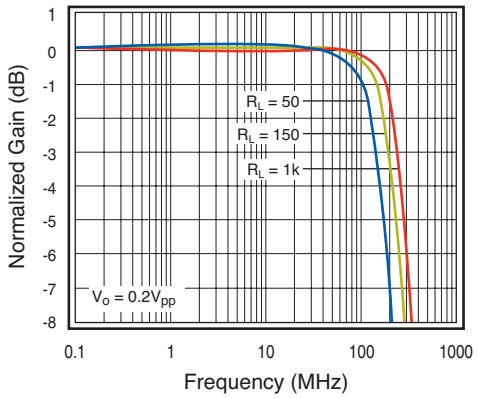



**Figure 6. Frequency Response vs. $R_L$ (+5V)**



## Typical Performance Characteristics

$T_C$ = 25°C, $V_S$ = 5V, $R_f$ = 249Ω, $R_L$ = 150Ω to $V_S$/2, G = 2; unless otherwise noted.

**Figure 7. Large Signal Freq. Response (±5V)**

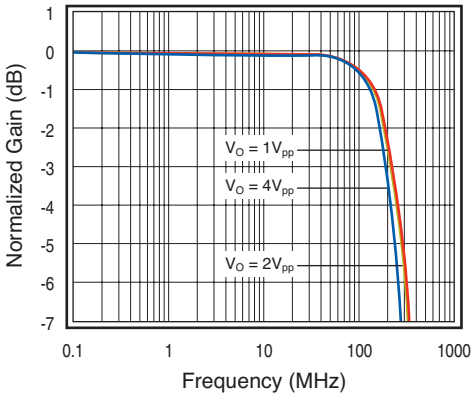



**Figure 8. Gain Flatness vs. Frequency**

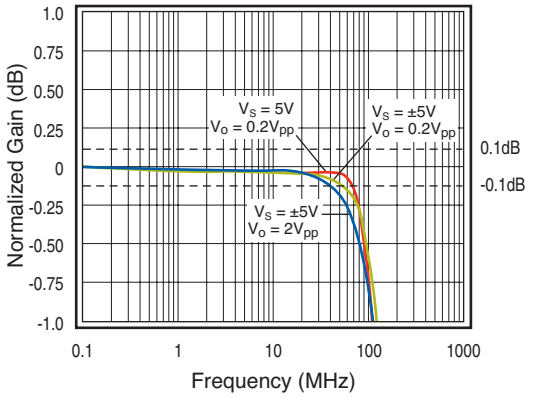



**Figure 9. HD2 vs. Frequency (±5V)**

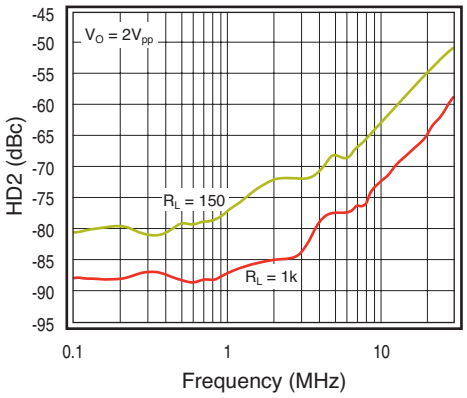



**Figure 10. HD3 vs. Frequency (±5V)**

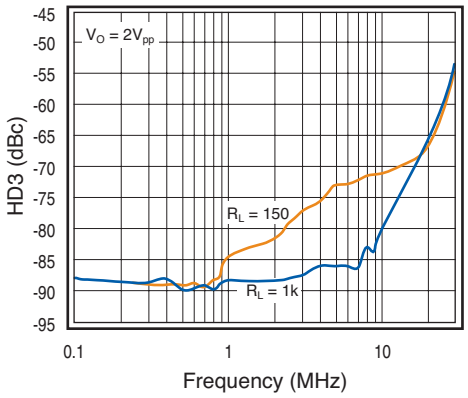



**Figure 11. HD2 vs. $V_o$ (±5V)**

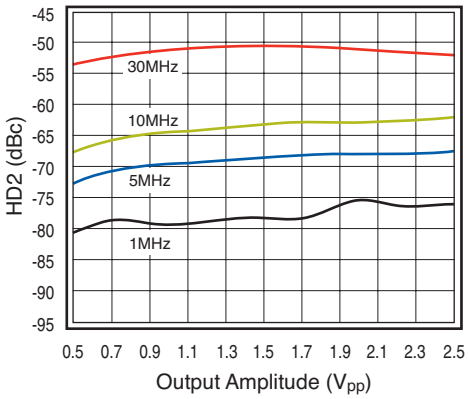
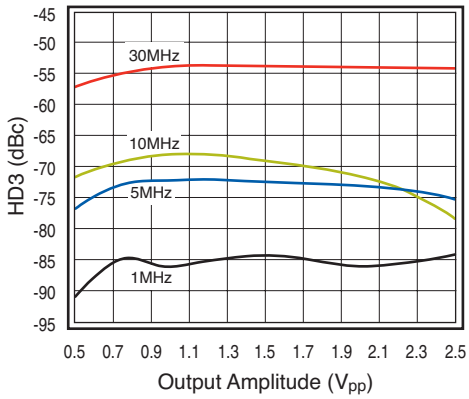



**Figure 12. HD3 vs. $V_o$ (±5V)**



## Typical Performance Characteristics

$T_c$ = 25°C, $V_S$ = 5V, $R_f$ = 249Ω, $R_L$ = 150Ω to $V_S$/2, G = 2; unless otherwise noted.

**Figure 13. CMRR vs. Frequency**

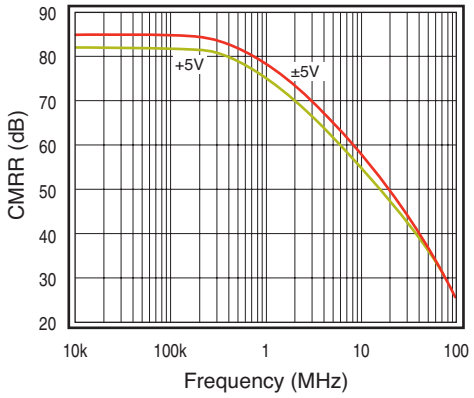



**Figure 14. PSRR vs. Frequency**

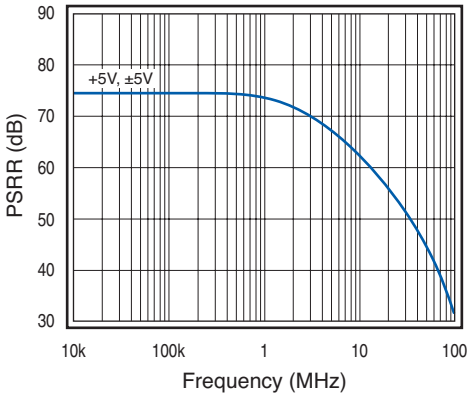



**Figure 15. Open Loop Gain & Phase vs. Freq.**

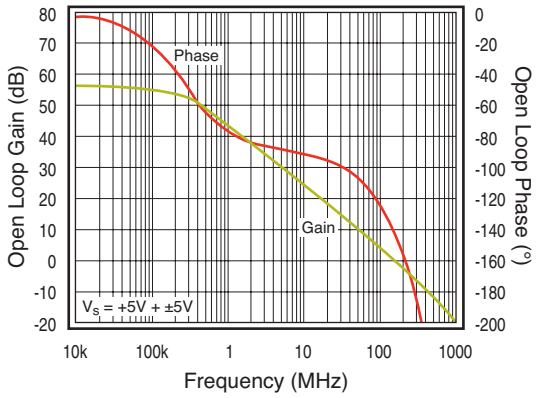



**Figure 16. Input Voltage Noise (+5V)**

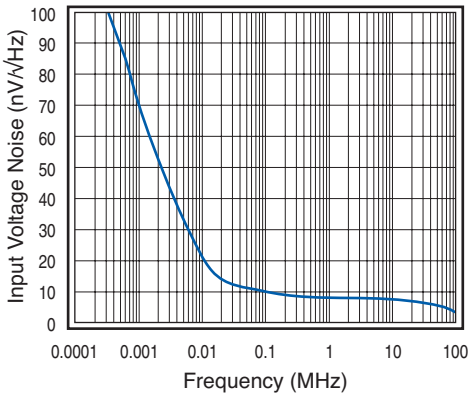



**Figure 17. Crosstalk vs. Frequency (+5V)**

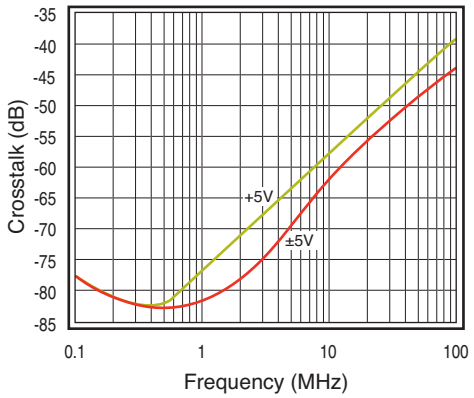
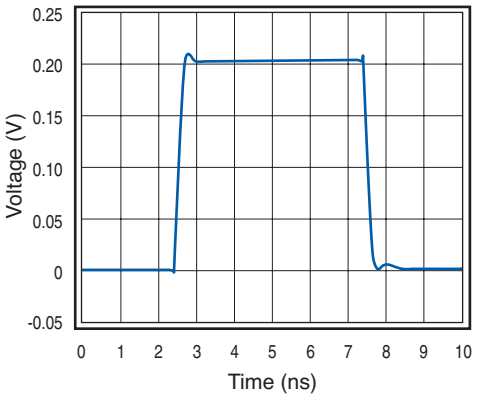



**Figure 18. Small Signal Pulse Response (+5V)**



## Typical Performance Characteristics

$T_c$ = 25°C, $V_S$ = 5V, $R_f$ = 249Ω, $R_L$ = 150Ω to $V_S$/2, G = 2; unless otherwise noted.

**Figure 19. Large Signal Pulse Response (+5V)**

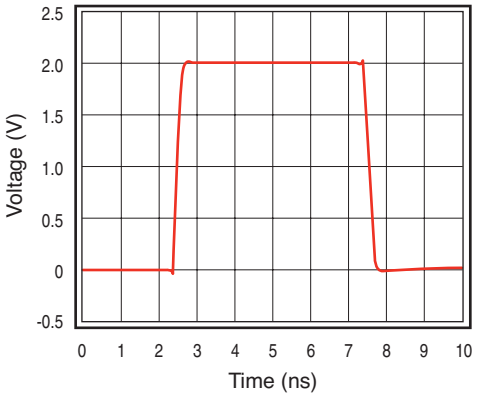



**Figure 20. Small Signal Pulse Response (±5V)**

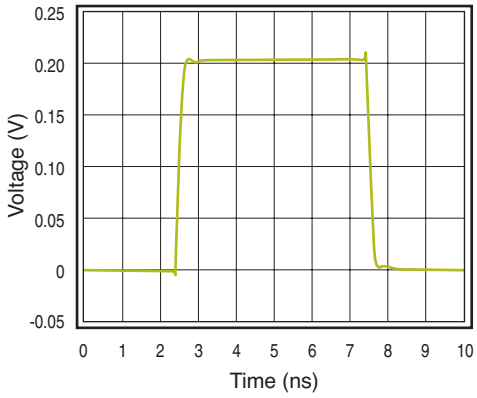



**Figure 21. Large Signal Pulse Response (±5V)**

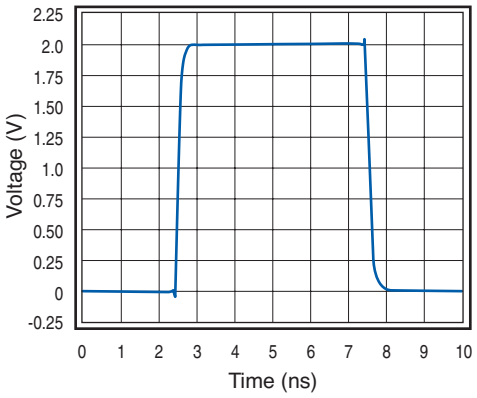



**Figure 22. Large Signal Pulse Response (±5V)**

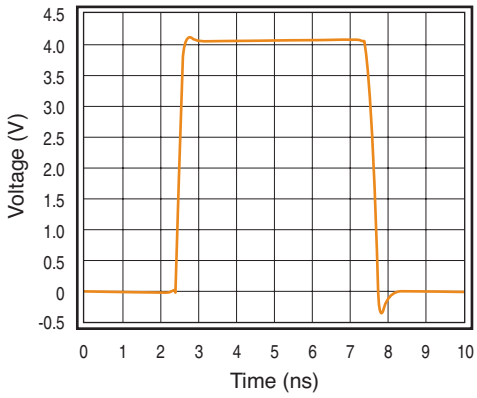



**Figure 23. Differential Gain and Phase (±2.5V)**

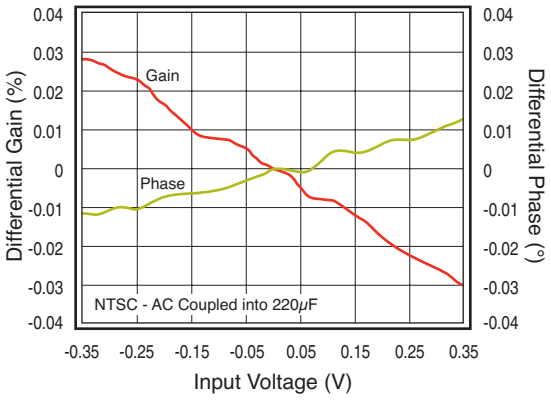
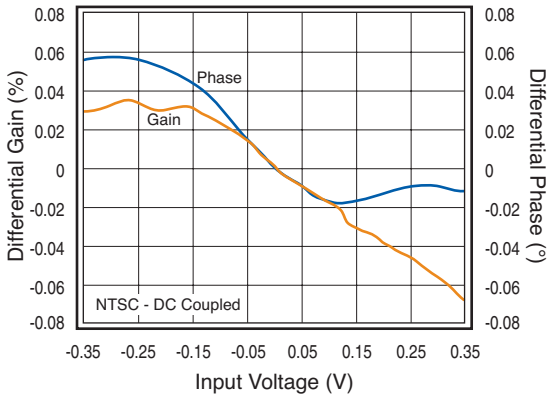



**Figure 24. Differential Gain and Phase (±2.5V)**



## Typical Performance Characteristics

$T_c$ = 25°C, $V_S$ = 5V, $R_f$ = 249Ω, $R_L$ = 150Ω to $V_S$/2, G = 2; unless otherwise noted.

**Figure 25. Differential Gain and Phase (±5V)**

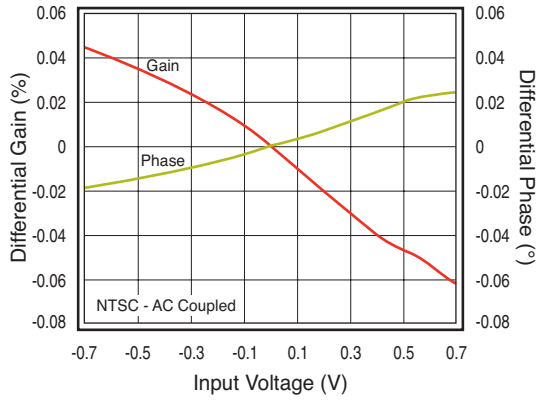



**Figure 26. Differential Gain and Phase (±5V)**

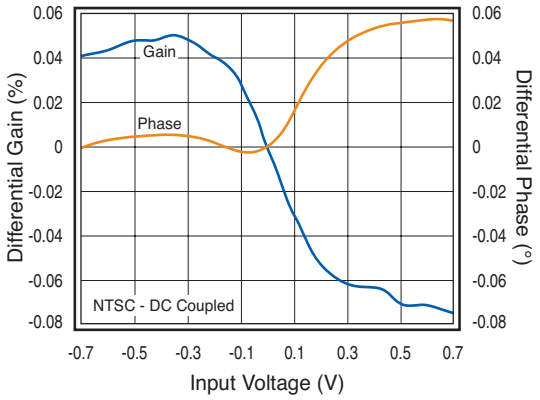



**Figure 27. Enable/Disable Response (±2.5V)**

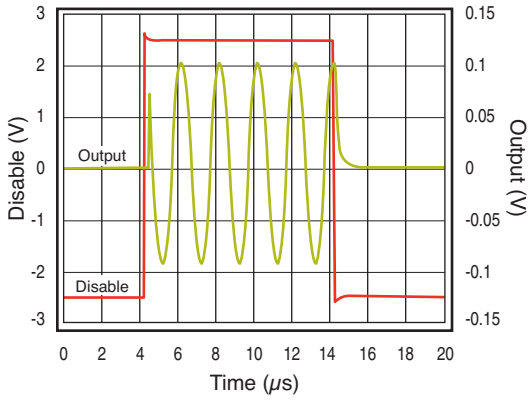



**Figure 28. Channel-to-Channel Isolation (+5V)**

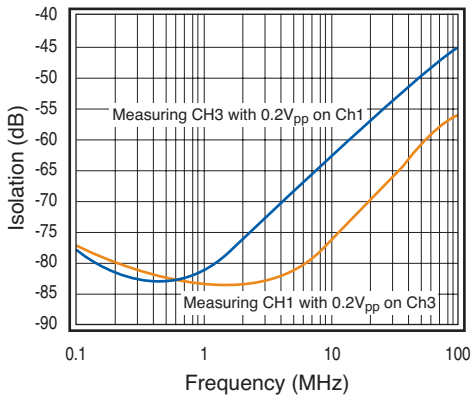



**Figure 29. Off Isolation (+5V)**

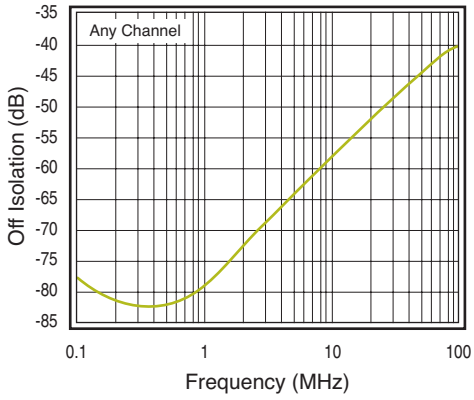
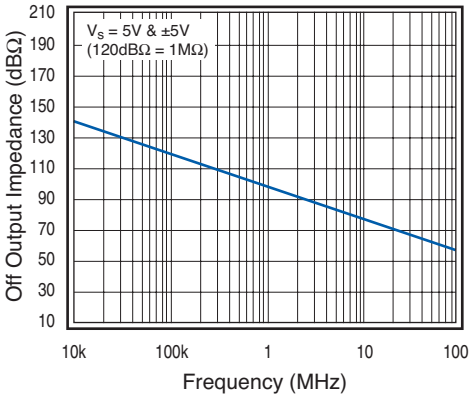



**Figure 30. Off Output Impedance (+5V)**



# Applications Information

## General Description

The FHP3350 and FHP3450 are low cost, high performance, voltage feedback amplifiers designed for video applications. These triple and quad amplifiers consume only 3.6mA of supply current per channel and are capable of driving dual (75Ω) video loads while providing 0.1dB of gain flatness to 30MHz. Consumer video applications will also benefit from their low 0.07% differential gain and 0.03˚ differential phase errors. The FHP3350 offers three outputs that can be put into a high impedance disable state to allow for video multiplexing or minimize power consumption.

These amplifiers are designed to operate from 5V (±2.5V) to 12V (±6V) supplies. The outputs swing to within 1.3V of either supply rail to accommodate video signals on a single 5V supply.

The FHP3350 and FHP3450 are designed on a complementary bipolar process. They provide 210MHz of full power bandwidth and 1,100V/µs of slew rate at a supply voltage of ±5V. The combination of high performance, low power, and excellent video performance make these amplifiers well suited for use in many digital consumer video appliances as well as many general purpose high speed applications.

## Driving Capacitive Loads

The Frequency Response vs. $C_L$ plot on page 8, illustrates the response of the FHP3350 Family. A small series resistance ($R_s$) at the output of the amplifier, illustrated in Figure 1, will improve stability and settling performance. $R_s$ values in the Frequency Response vs. $C_L$ plot were chosen to achieve maximum bandwidth with less than 1dB of peaking. For maximum flatness, use a larger $R_s$.

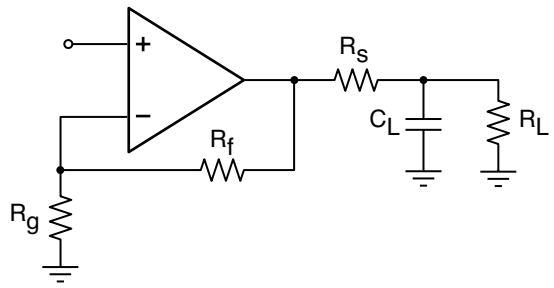



**Figure 31. Typical Topology for driving capacitive loads**

## Power Dissipation

The maximum internal power dissipation allowed is directly related to the maximum junction temperature. If the maximum junction temperature exceeds 150˚C for an extended time, device failure may occur. The FHP3350 and FHP3450 are short circuit protected. However, this may not guarantee that the maximum junction temperature (+150˚C) is not exceeded under all conditions. RMS Power Dissipation can be calculated using the following equation:

Power Dissipation = $I_S * (V_S+ - V_S-) + (V_S+ - V_{O(RMS)}) * I_{OUT(RMS)}$

Where $I_S$ is the supply current, $V_S+$ is the positive supply pin voltage, $V_S-$ is the negative supply pin voltage, $V_{O(RMS)}$ is the RMS output voltage and $I_{OUT(RMS)}$ is the RMS output current delivered to the load. Follow the maximum power derating curves shown in Figure 32 below to ensure proper operation.

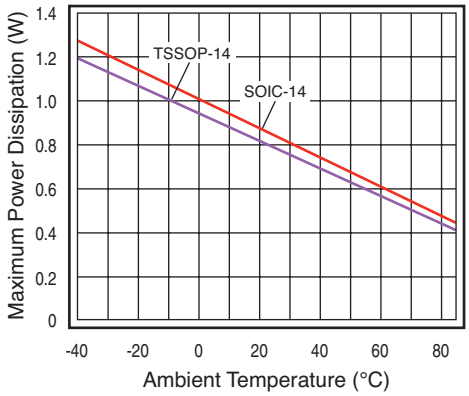



**Figure 32. Maximum Power Derating**

## Overdrive Recovery

For an amplifier, an overdrive condition occurs when the output and/or input ranges are exceeded. The recovery time varies based on whether the input or output is overdriven and by how much the ranges are exceeded. The FHP3350/3450 will typically recover in less than 50ns from an overdrive condition. Figure 33 shows the FHP3350 in an overdriven condition.

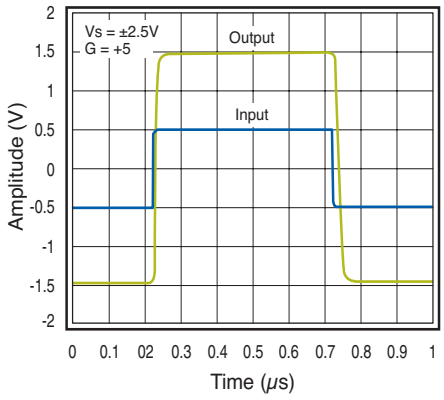



**Figure 33. Overdrive Recovery**

## Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. Fairchild has evaluation boards to use as a guide for high frequency layout and as aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8µF and 0.01µF ceramic capacitors
- Place the 6.8µF capacitor within 0.75 inches of the power pin
- Place the 0.01µF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts shown below for more information.

## Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of thes devices:

| Evaluation Board # | Products |
|---|---|
| KEB019 | FHP3350IM14X |
| KEB020 | FHP3350IMTC14X |
| KEB012 | FHP3450IMTC14X |
| KEB018 | FHP3450IM14X |

## Evalutaion Board Schematics

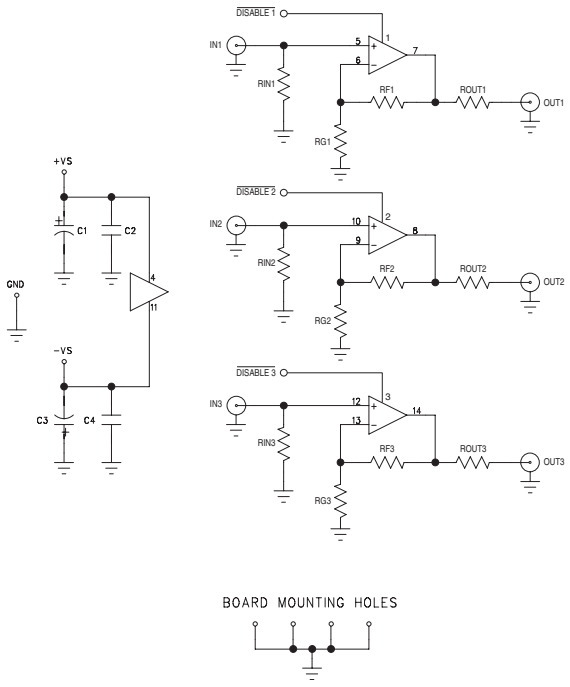



**Figure 34. FHP3350 KEB019/KEB020 schematic**

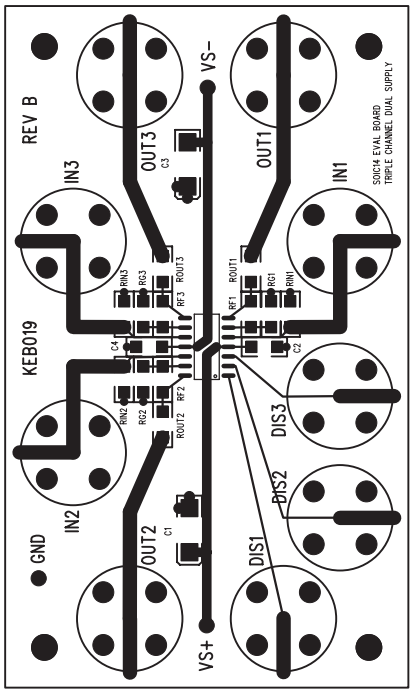



**Figure 35. FHP3350 KEB019 (top side)**

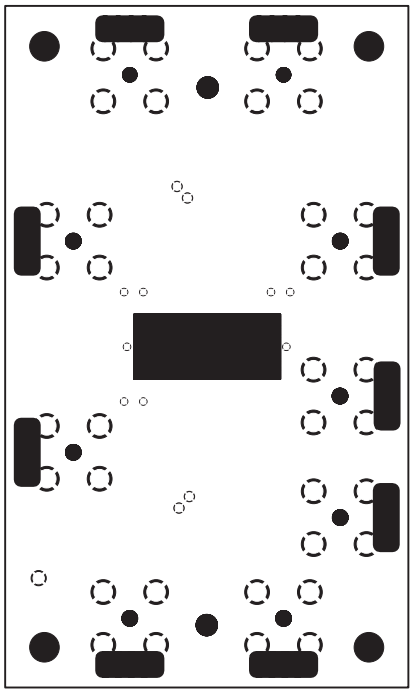


**Figure 36. FHP3350 KEB019 (bottom side)**

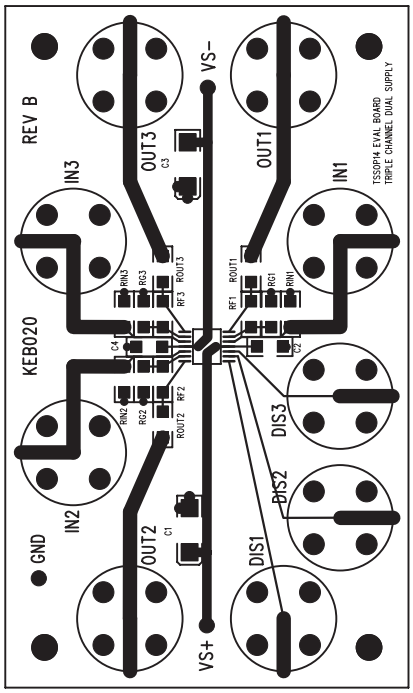



**Figure 37. FHP3350 KEB020 (top side)**

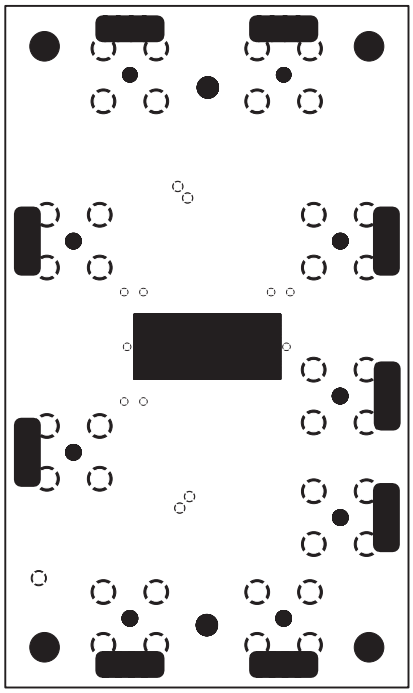


**Figure 38. FHP3350 KEB020 (bottom side)**

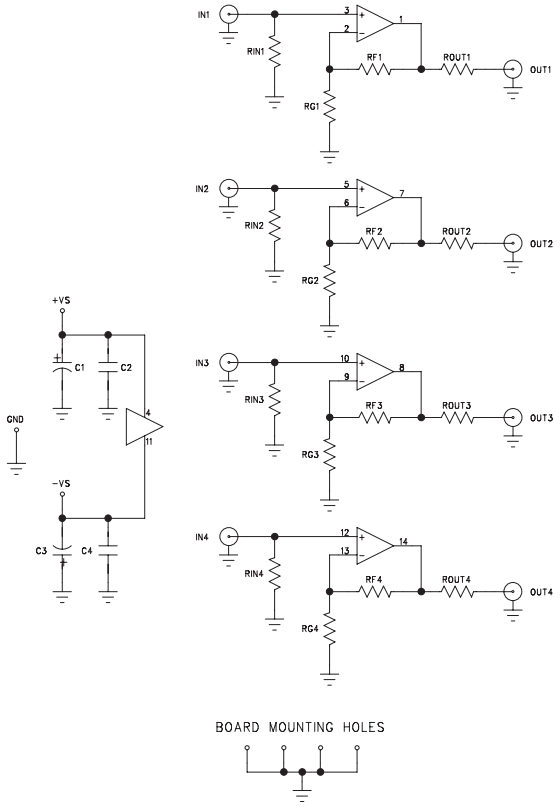



**Figure 39. FHP3450 KEB012/KEB018 schematic**

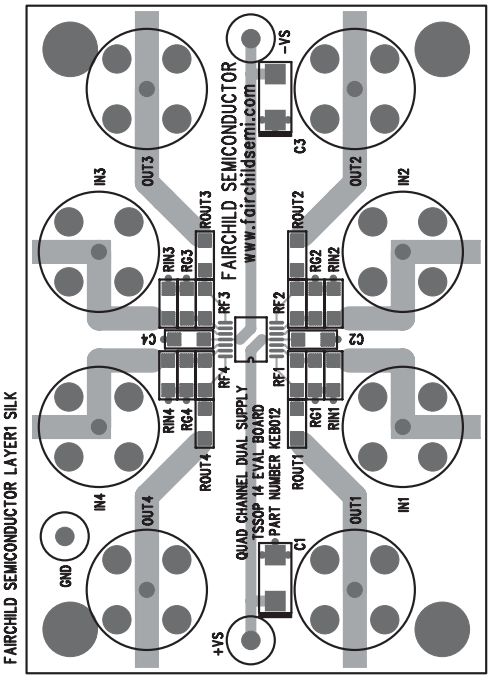



**Figure 40. FHP3450 KEB012 (top side)**

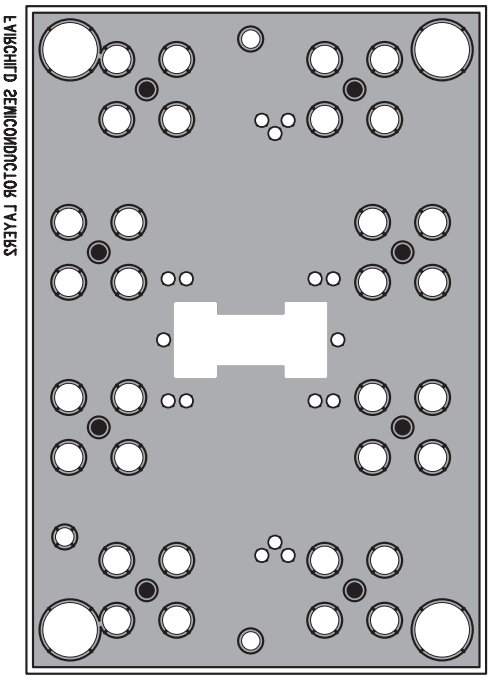



Figure 41. FHP3450 KEB012 (bottom side)

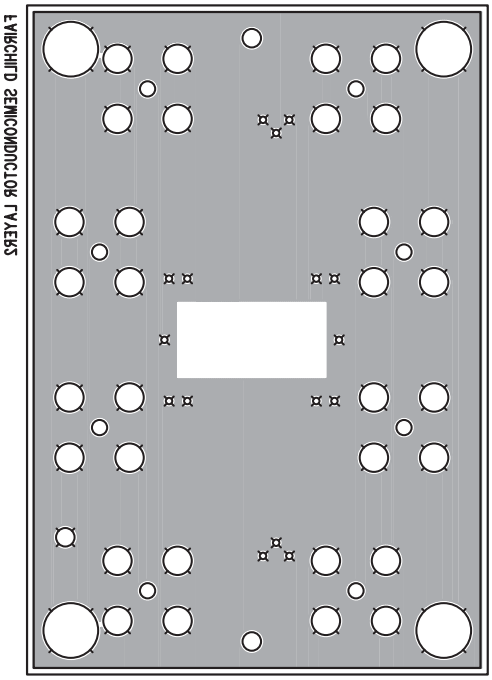



Figure 43. FHP3450 KEB018 (bottom side)

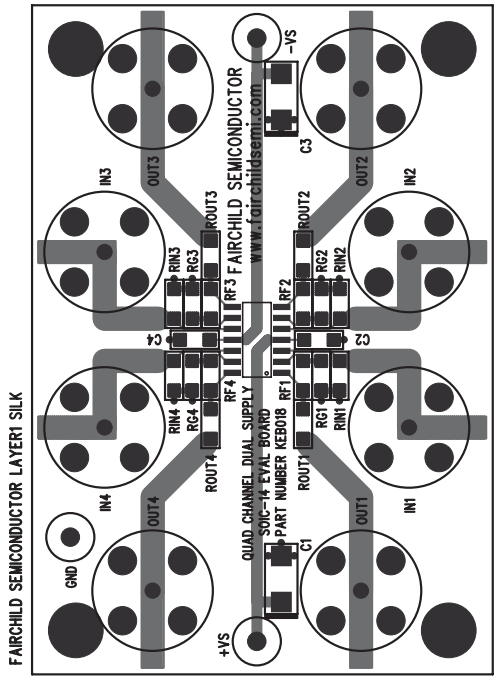
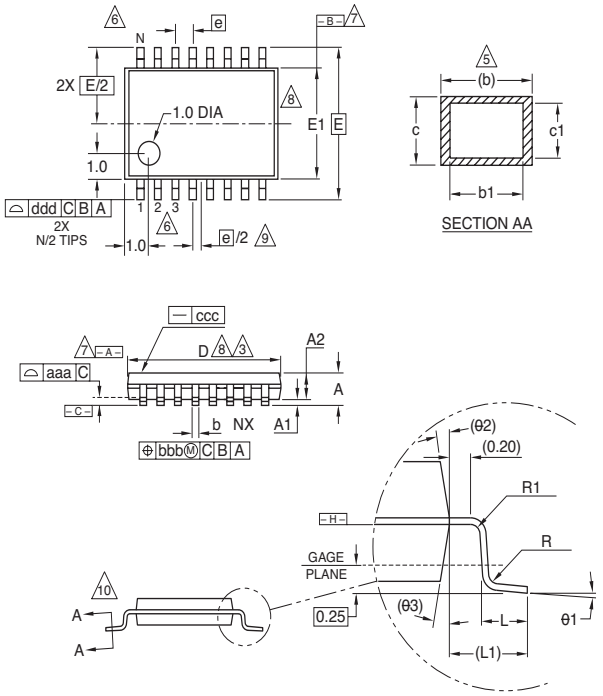



Figure 42. FHP3450 KEB018 (top side)

## Mechanical Dimensions

### 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package

### Number MTC14




| TSSOP-14 | | | |
|---|---|---|---|
| **SYMBOL** | **MIN** | **NOM** | **MAX** |
| A | – | – | 1.10 |
| A1 | 0.05 | – | 0.15 |
| A2 | 0.85 | 0.90 | 0.95 |
| L | 0.50 | 0.60 | 0.75 |
| R | 0.09 | – | – |
| R1 | 0.09 | – | – |
| b | 0.19 | – | 0.30 |
| b1 | 0.19 | 0.22 | 0.25 |
| c | 0.09 | – | 0.20 |
| c1 | 0.09 | – | 0.16 |
| θ1 | 0° | – | 8° |
| L1 | 1.0 REF | | |
| aaa | 0.10 | | |
| bbb | 0.10 | | |
| ccc | 0.05 | | |
| ddd | 0.20 | | |
| e | 0.65 BSC | | |
| θ2 | 12° REF | | |
| θ3 | 12° REF | | |
| D | 4.90 | 5.00 | 5.10 |
| E1 | 4.30 | 4.40 | 4.50 |
| E | 6.4 BSC | | |
| e | 0.65 BSC | | |
| N | 14 | | |

**NOTES:**

1 All dimensions are in millimeters (angle in degrees).

2 Dimensioning and tolerancing per ASME Y14.5–1994.

3 Dimensions "D" does not include mold flash, protusions or gate burrs. Mold flash protusions or gate burrs shall not exceed 0.15 per side .

4 Dimension "E1" does not include interlead flash or protusion. Interlead flash or protusion shall not exceed 0.25 per side.

5 Dimension "b" does not include dambar protusion. Allowable dambar protusion shall be 0.08mm total in excess of the "b" dimension at maximum material condition. Dambar connot be located on the lower radius of the foot. Minimum space between protusion and adjacent lead is 0.07mm for 0.5mm pitch packages.

6 Terminal numbers are shown for reference only.

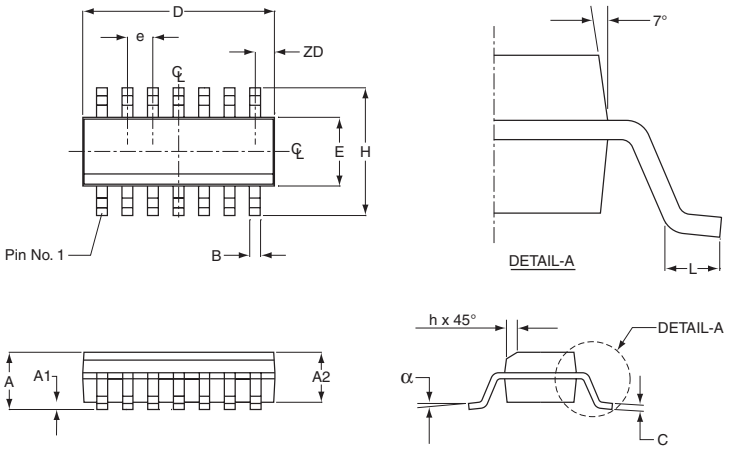
7 Datums – A – and – B – to be determined at datum plane – H –.

8 Dimensions "D" and "E1" to be determined at datum plane – H –.

9 This dimensions applies only to variations with an even number of leads per side. For variation with an odd number of leads per side, the "center" lead must be coincident with the package centerline, Datum A.

10 Cross sections A – A to be determined at 0.10 to 0.25mm from the leadtip.

## 14-Lead Small Outline Package (SOIC)




| SOIC-14 | | |
|---|---|---|
| **SYMBOL** | **MIN** | **MAX** |
| A1 | .0040 | .0098 |
| B | .014 | .018 |
| C | .0075 | .0098 |
| D | .337 | .344 |
| E | .150 | .157 |
| e | .050 BSC | |
| H | .2284 | .2440 |
| h | .0099 | .0196 |
| L | .016 | .050 |
| A | .060 | .068 |
| | 0° | 8° |
| ZD | 0.20 ref | |
| A2 | .054 | .062 |

**NOTE:**

1. All dimensions are in inches.
2. Lead coplanarity should be 0 to 0.10mm (.004") max.
3. Package surface finishing:
   (2.1) Top: matte (charmilles #18~30).
   (2.2) All sides: matte (charmilles #18~30).
   (2.3) Bottom: smooth or matte (charmilles #18~30).
4. All dimensions excluding mold flashes and end flash from the package body shall not exceed o.152mm (.006) per side (d).

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| ActiveArray™ | FASTr™ | LittleFET™ | PowerSaver™ | SuperSOT™-3 |
| Bottomless™ | FPS™ | MICROCOUPLER™ | PowerTrench® | SuperSOT™-6 |
| Build it Now™ | FRFET™ | MicroFET™ | QFET® | SuperSOT™-8 |
| CoolFET™ | GlobalOptoisolator™ | MicroPak™ | QS™ | SyncFET™ |
| *CROSSVOLT*™ | GTO™ | MICROWIRE™ | QT Optoelectronics™ | TCM™ |
| DOME™ | HiSeC™ | MSX™ | Quiet Series™ | TinyLogic® |
| EcoSPARK™ | $I^2C$™ | MSXPro™ | RapidConfigure™ | TINYOPTO™ |
| $E^2CMOS$™ | *i-Lo*™ | OCX™ | RapidConnect™ | TruTranslation™ |
| EnSigna™ | ImpliedDisconnect™ | OCXPro™ | µSerDes™ | UHC™ |
| FACT™ | IntelliMAX™ | OPTOLOGIC® | ScalarPump™ | UniFET™ |
| FACT Quiet Series™ | | OPTOPLANAR™ | SILENT SWITCHER® | UltraFET® |
| Across the board. Around the world.™ | | PACMAN™ | SMART START™ | VCX™ |
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