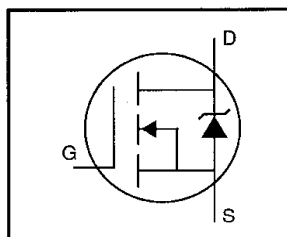


IRFI620GPbF

HEXFET® Power MOSFET

- Isolated Package
- High Voltage Isolation= 2.5KVRMS ⑤
- Sink to Lead Creepage Dist.= 4.8mm
- Dynamic dv/dt Rating
- Low Thermal Resistance
- Lead-Free



$$V_{DSS} = 200V$$

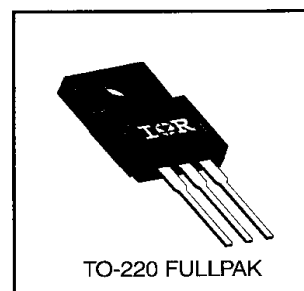
$$R_{DS(on)} = 0.80\Omega$$

$$I_D = 4.1A$$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	4.1	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	2.6	
I_{DM}	Pulsed Drain Current ①	16	
$P_D @ T_C = 25^\circ C$	Power Dissipation	30	W
	Linear Derating Factor	0.24	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	100	mJ
I_{AR}	Avalanche Current ①	4.1	A
E_{AR}	Repetitive Avalanche Energy ①	3.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	4.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	—	65	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	200	—	—	V	V _{GS} =0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.29	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.80	Ω	V _{GS} =10V, I _D =2.5A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	1.5	—	—	S	V _{DS} =50V, I _D =2.5A ④
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} =200V, V _{GS} =0V
		—	—	250		V _{DS} =160V, V _{GS} =0V, T _J =125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} =20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} =-20V
Q _g	Total Gate Charge	—	—	14	nC	I _D =4.8A
Q _{gs}	Gate-to-Source Charge	—	—	3.0		V _{DS} =160V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	7.9		V _{GS} =10V See Fig. 6 and 13 ④
t _{d(on)}	Turn-On Delay Time	—	7.2	—	ns	V _{DD} =100V
t _r	Rise Time	—	22	—		I _D =4.8A
t _{d(off)}	Turn-Off Delay Time	—	19	—		R _G =18Ω
t _f	Fall Time	—	13	—		R _D =20Ω See Figure 10 ④
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	260	—	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	100	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	30	—		f=1.0MHz See Figure 5
C	Drain to Sink Capacitance	—	12	—	pF	f=1.0MHz

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	4.1	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	16		
V _{SD}	Diode Forward Voltage	—	—	1.8	V	T _J =25°C, I _S =4.1A, V _{GS} =0V ④
t _{rr}	Reverse Recovery Time	—	150	300	ns	T _J =25°C, I _F =4.8A
Q _{rr}	Reverse Recovery Charge	—	0.91	1.8	μC	di/dt=100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

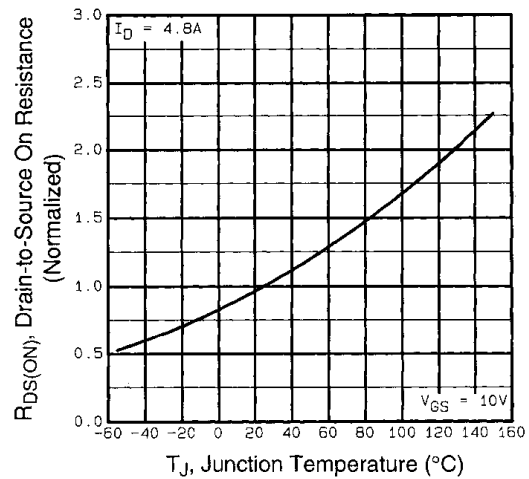
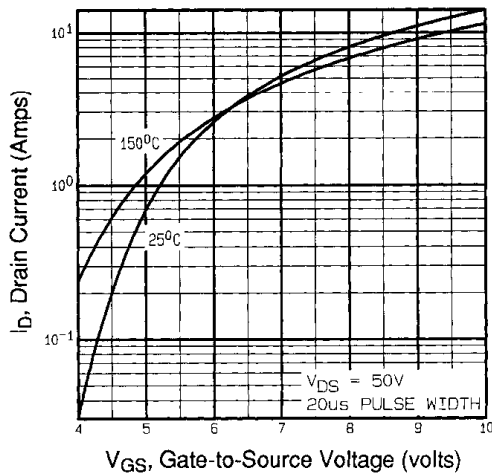
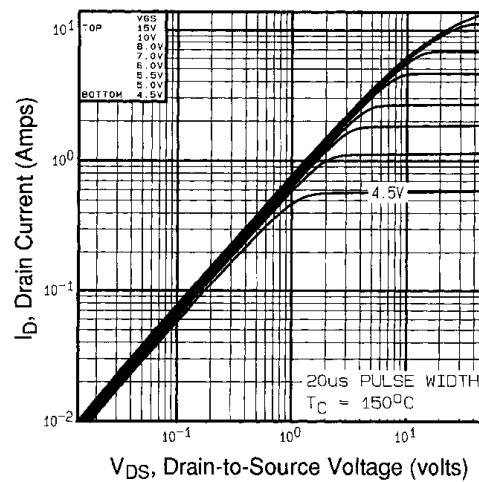
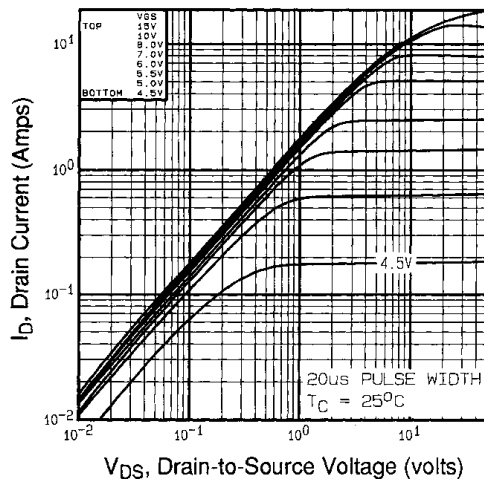
① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

③ I_{SD}≤5.2A, di/dt≤95A/μs, V_{DD}≤V_{(BR)DSS}, T_J≤150°C

⑤ t=60s, f=60Hz

② V_{DD}=50V, starting T_J=25°C, L=8.9mH
R_G=25Ω, I_{AS}=4.1A (See Figure 12)

④ Pulse width ≤ 300 μs; duty cycle ≤2%.



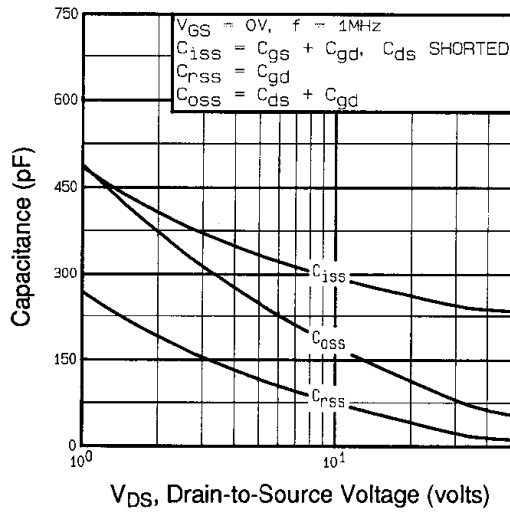


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

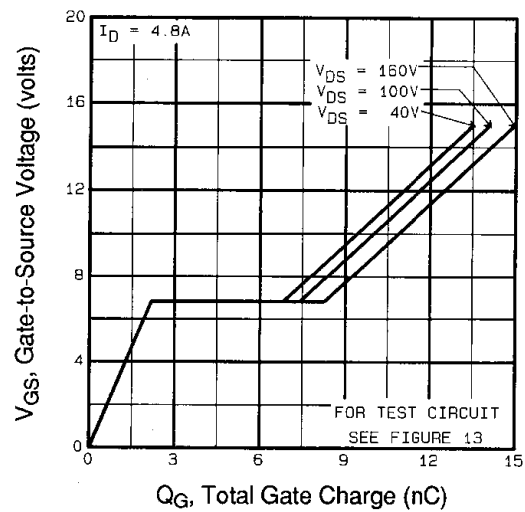


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

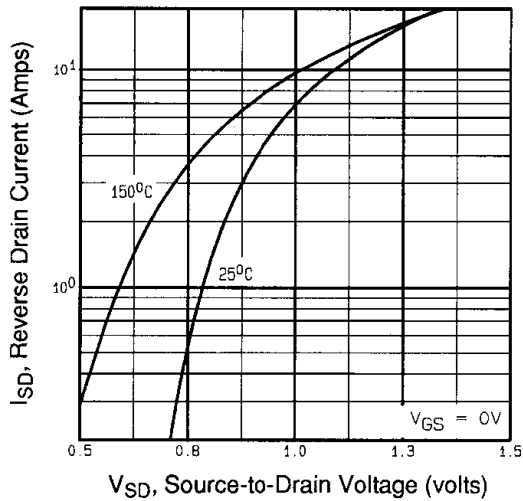


Fig 7. Typical Source-Drain Diode Forward Voltage

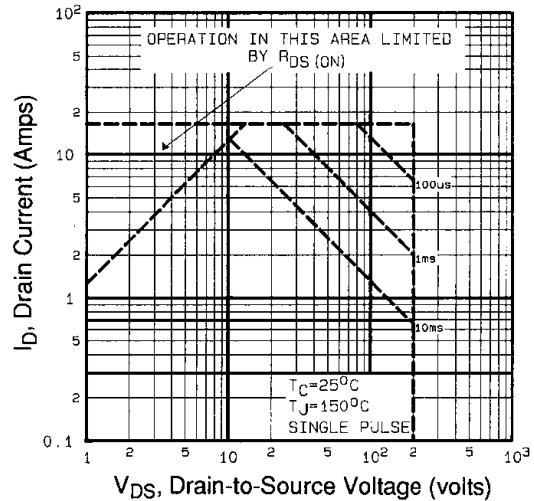


Fig 8. Maximum Safe Operating Area

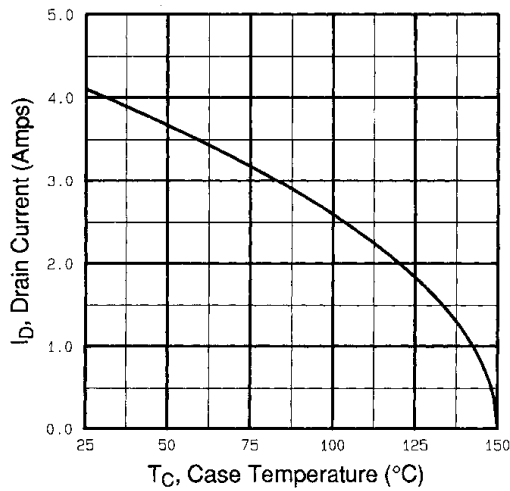


Fig 9. Maximum Drain Current Vs. Case Temperature

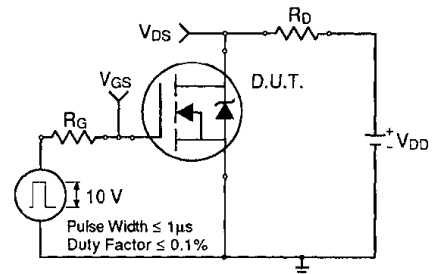


Fig 10a. Switching Time Test Circuit

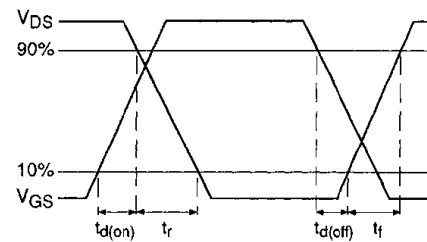


Fig 10b. Switching Time Waveforms

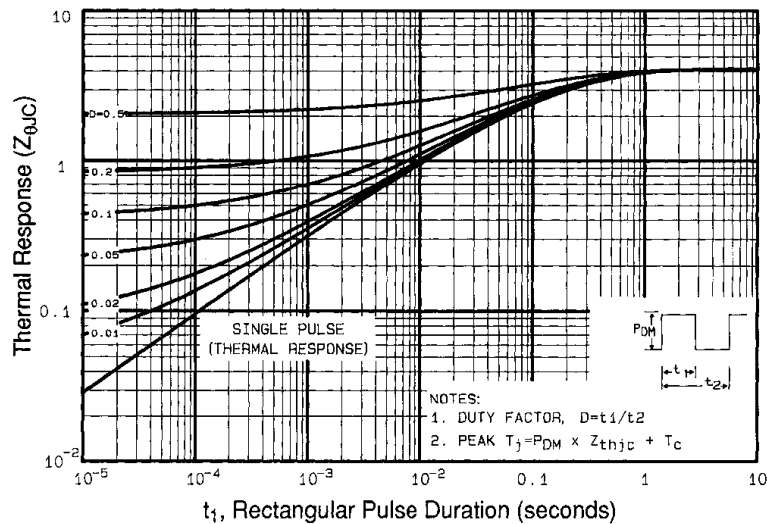


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

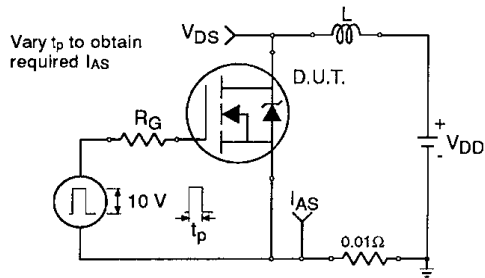


Fig 12a. Unclamped Inductive Test Circuit

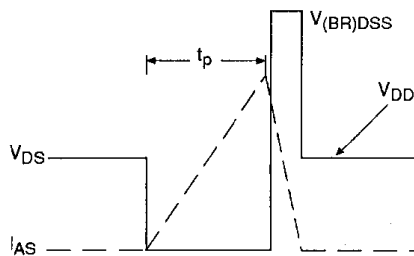


Fig 12b. Unclamped Inductive Waveforms

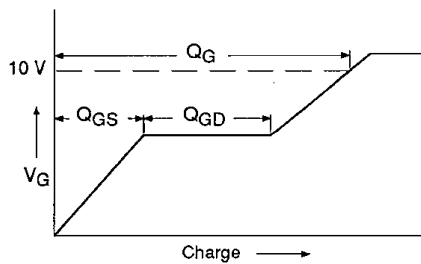


Fig 13a. Basic Gate Charge Waveform

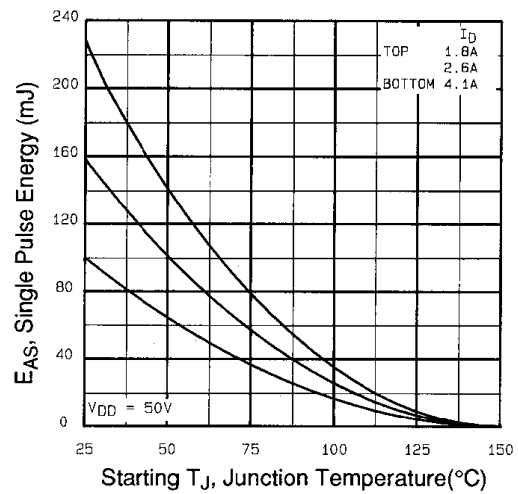


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

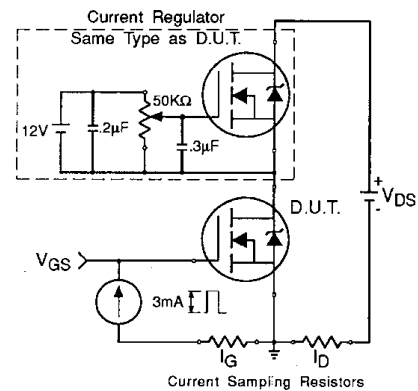
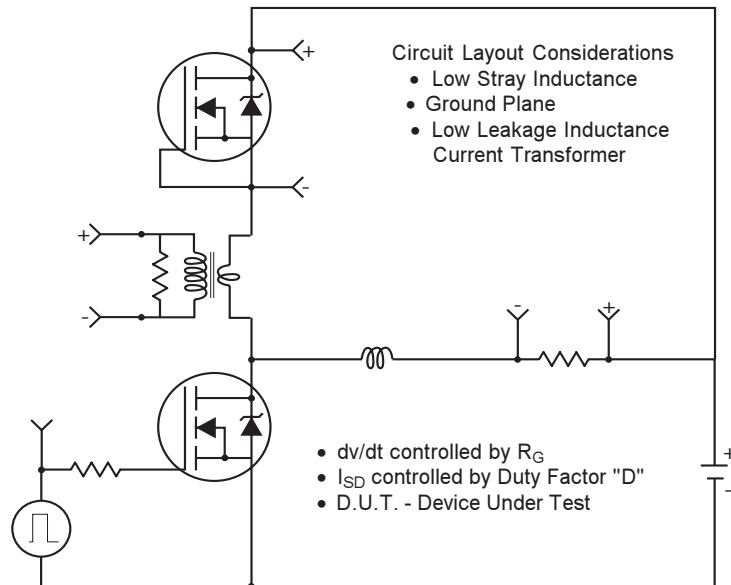


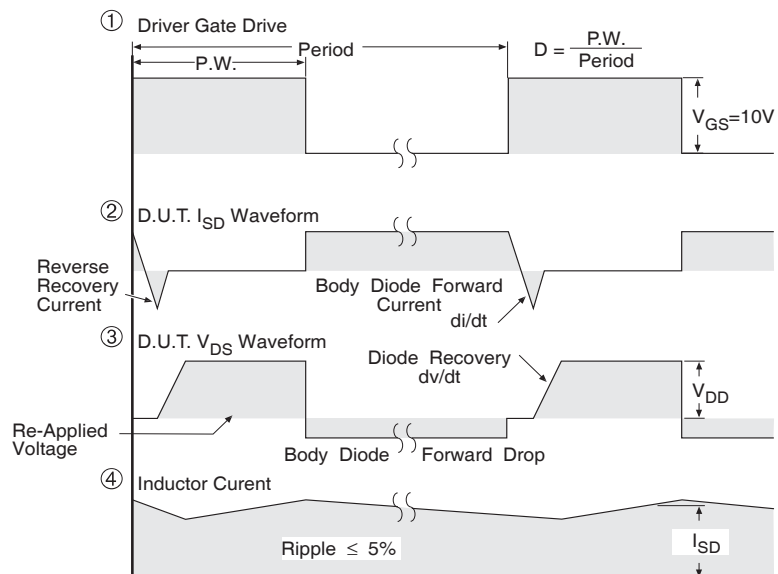
Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

** Use P-Channel Driver for P-Channel Measurements



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

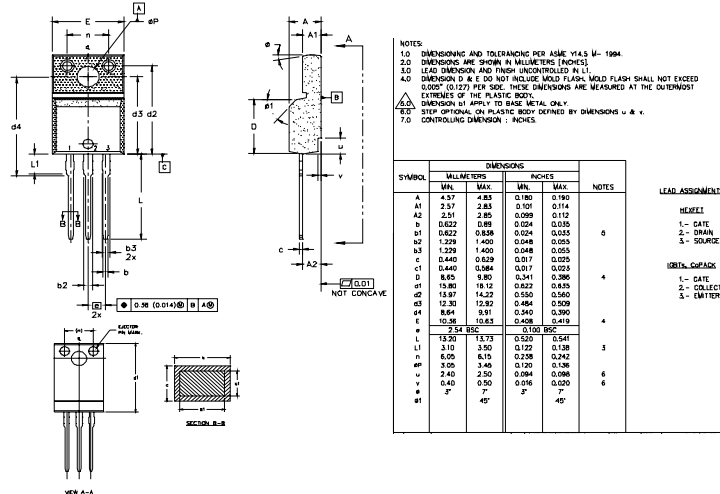
Fig. 14 For N and P Channel HEXFETS

IRFI620GPbF

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TO-220 Full-Pak Package Outline

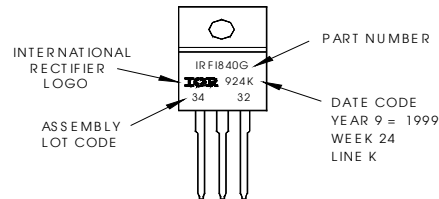
Dimensions are shown in millimeters (inches)



TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRFI840G
WITH ASSEMBLY
LOT CODE 3432
ASSEMBLED ON WW 24 1999
IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.

International
IOR Rectifier

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TAC Fax: (310) 252-7903

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