

IRFR210PbF IRFU210PbF

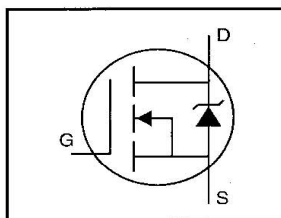
HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Surface Mount (IRFR210)
- Straight Lead (IRFU210)
- Available in Tape & Reel
- Fast Switching
- Ease of Paralleling
- Lead-Free

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

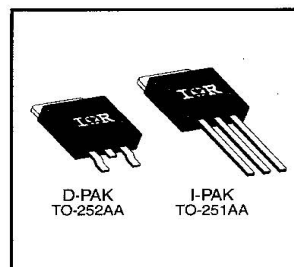
The D-Pak is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



$$V_{DSS} = 200V$$

$$R_{DS(on)} = 1.5\Omega$$

$$I_D = 2.6A$$



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10 V	2.6	A
I_D @ $T_C = 100^\circ C$	Continuous Drain Current, V_{GS} @ 10 V	1.7	
I_{DM}	Pulsed Drain Current ①	10	
P_D @ $T_C = 25^\circ C$	Power Dissipation	25	W
P_D @ $T_A = 25^\circ C$	Power Dissipation (PCB Mount)**	2.5	
	Linear Derating Factor	0.20	W/°C
	Linear Derating Factor (PCB Mount)**	0.020	
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	130	mJ
I_{AR}	Avalanche Current ①	2.7	A
E_{AR}	Repetitive Avalanche Energy ①	2.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	260 (1.6mm from case)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	5.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)**	—	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	—	110	

** When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS}=0V$, $I_D=250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.30	—	$V/^\circ\text{C}$	Reference to 25°C , $I_D=1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	1.5	Ω	$V_{GS}=10V$, $I_D=1.6A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
g_{fs}	Forward Transconductance	0.80	—	—	S	$V_{DS}=50V$, $I_D=1.6A$ ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS}=200V$, $V_{GS}=0V$
		—	—	250		$V_{DS}=160V$, $V_{GS}=0V$, $T_J=125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS}=20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS}=-20V$
Q_g	Total Gate Charge	—	—	8.2	nC	$I_D=3.3A$
Q_{gs}	Gate-to-Source Charge	—	—	1.8		$V_{DS}=160V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	4.5		$V_{GS}=10V$ See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	8.2	—	ns	$V_{DD}=100V$
t_r	Rise Time	—	17	—		$I_D=3.3A$
$t_{d(off)}$	Turn-Off Delay Time	—	14	—		$R_G=24\Omega$
t_f	Fall Time	—	8.9	—		$R_D=30\Omega$ See Figure 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	140	—	pF	$V_{GS}=0V$
C_{oss}	Output Capacitance	—	53	—		$V_{DS}=25V$
C_{rss}	Reverse Transfer Capacitance	—	15	—		$f=1.0\text{MHz}$ See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	2.6	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	10		
V_{SD}	Diode Forward Voltage	—	—	2.0	V	$T_J=25^\circ\text{C}$, $I_S=2.6A$, $V_{GS}=0V$ ④
t_{rr}	Reverse Recovery Time	—	150	310	ns	$T_J=25^\circ\text{C}$, $I_F=3.3A$
Q_{rr}	Reverse Recovery Charge	—	0.60	1.4	μC	$di/dt=100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

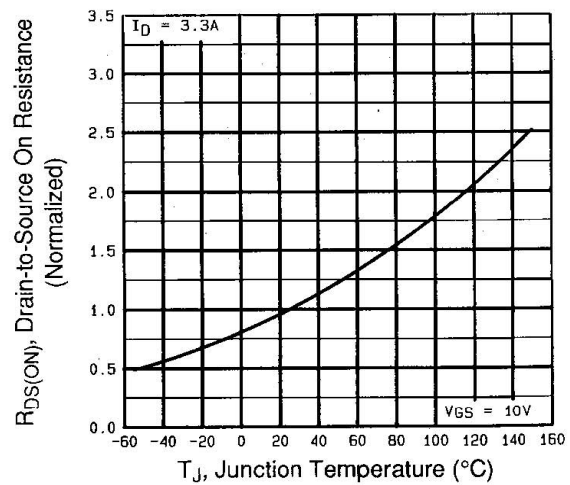
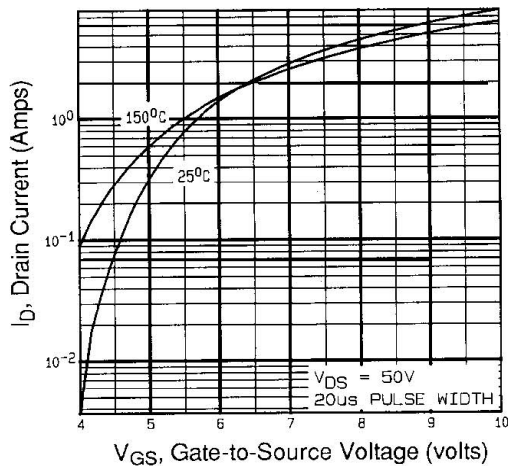
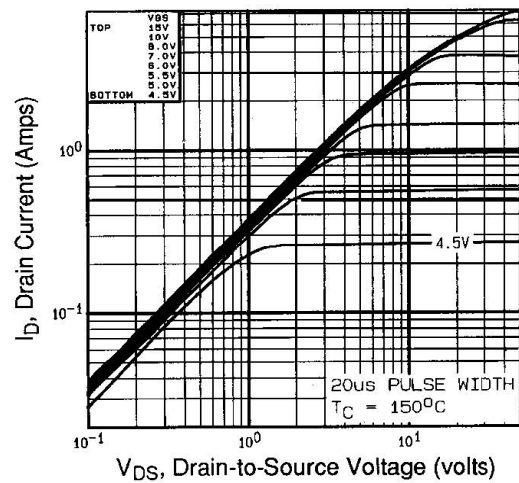
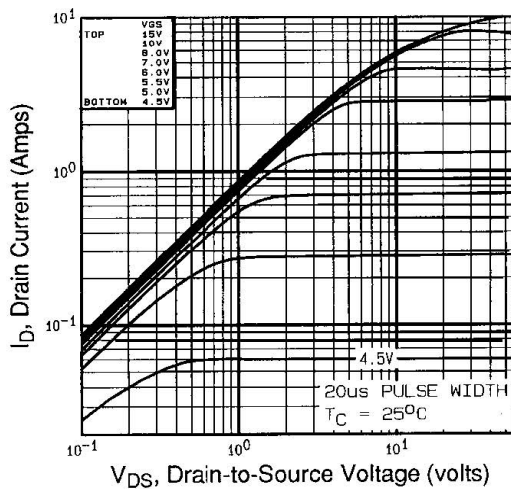
Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② $V_{DD}=50V$, starting $T_J=25^\circ\text{C}$, $L=28\text{mH}$
 $R_G=25\Omega$, $I_{AS}=2.6A$ (See Figure 12)

③ $I_{SD}\leq 2.6A$, $di/dt\leq 70A/\mu s$, $V_{DD}\leq V_{(BR)DSS}$,
 $T_J\leq 150^\circ\text{C}$

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.



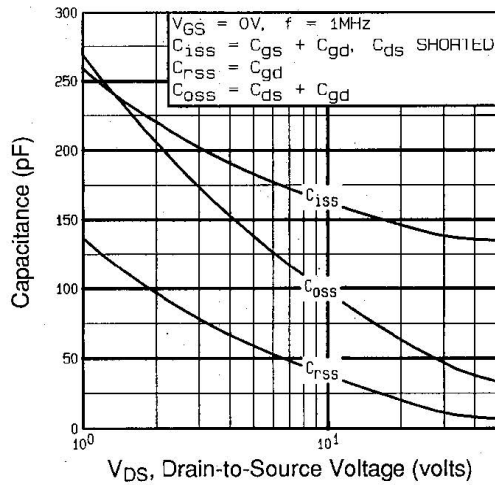


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

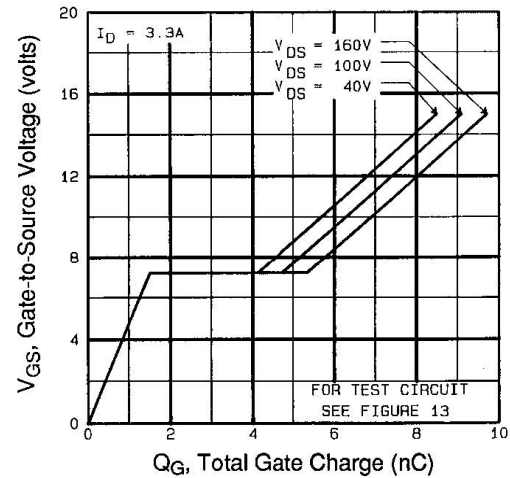


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

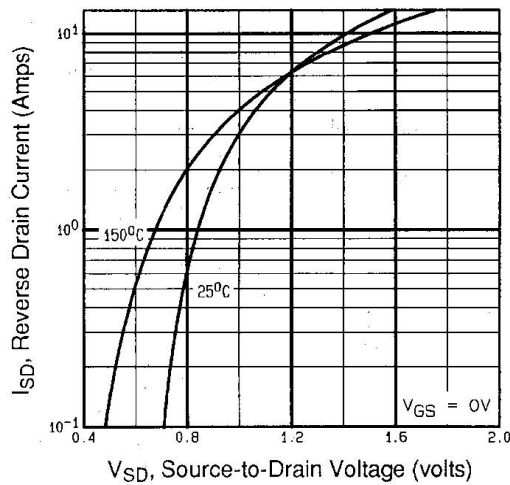


Fig 7. Typical Source-Drain Diode Forward Voltage

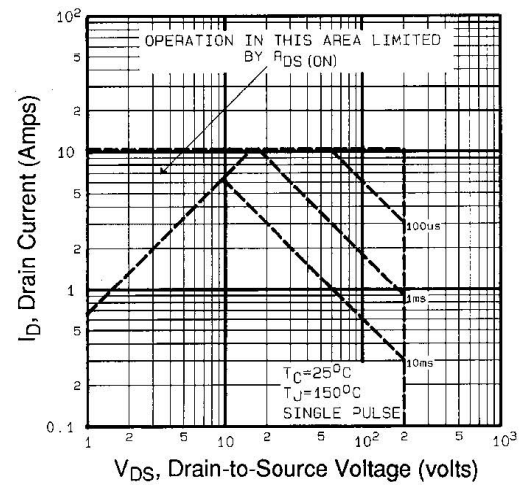


Fig 8. Maximum Safe Operating Area

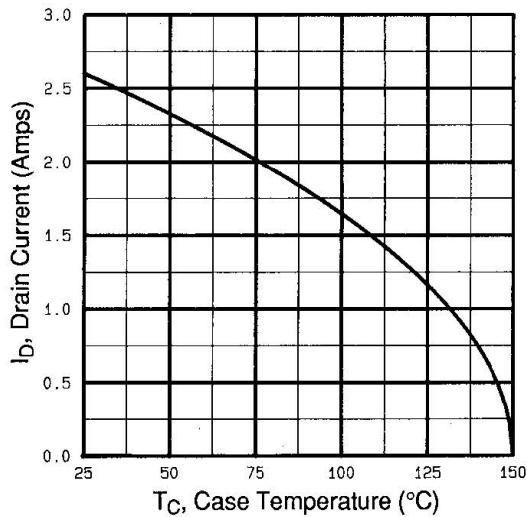


Fig 9. Maximum Drain Current Vs. Case Temperature

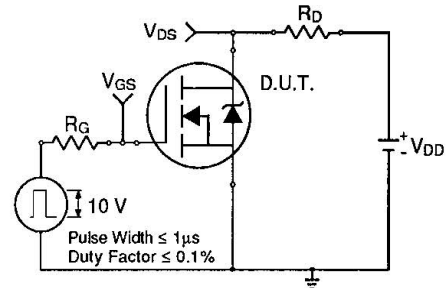


Fig 10a. Switching Time Test Circuit

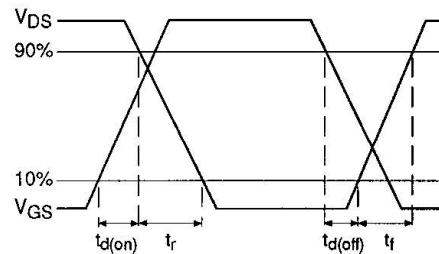


Fig 10b. Switching Time Waveforms

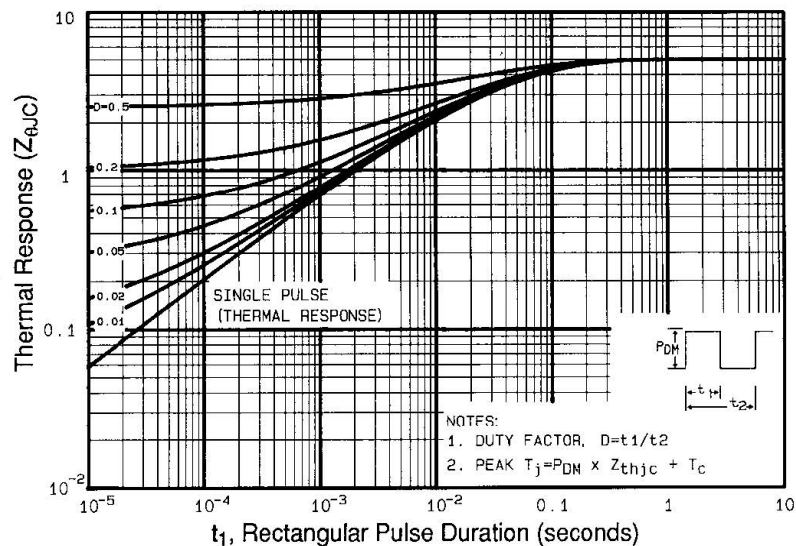


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

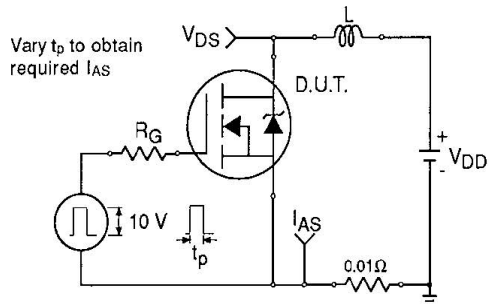


Fig 12a. Unclamped Inductive Test Circuit

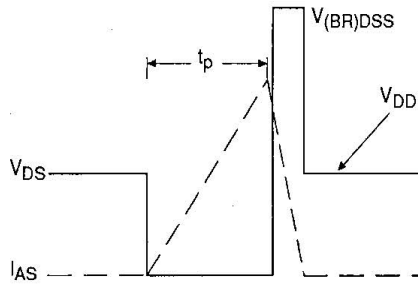


Fig 12b. Unclamped Inductive Waveforms

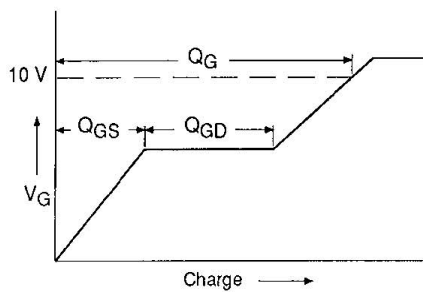


Fig 13a. Basic Gate Charge Waveform

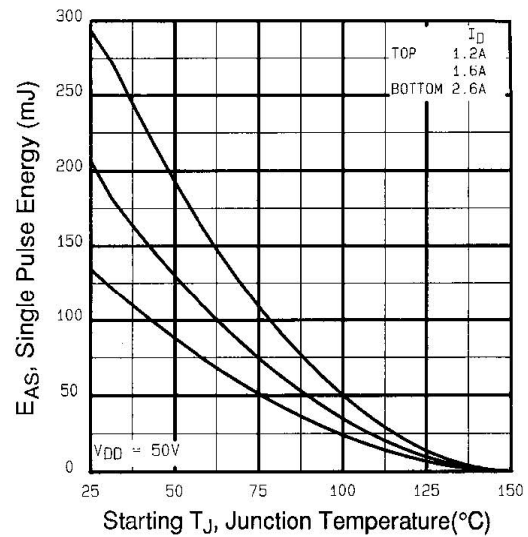


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

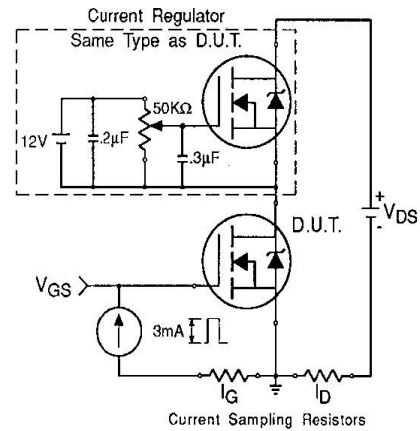


Fig 13b. Gate Charge Test Circuit

The diagram shows a Class-AB push-pull amplifier circuit. It consists of two NPN bipolar junction transistors in a push-pull configuration. The bases of both transistors are driven by a common-emitter BJT driver stage. The driver stage's base is connected to a square-wave voltage source through a resistor. The driver stage's emitter is connected to ground, and its collector is connected to the bases of the output transistors. The load is connected between the collectors of the two output transistors and is represented by a transformer. A current transformer is placed in the secondary winding of the load transformer to sense the load current. The primary winding of the current transformer is connected in series with the load. The secondary winding is connected to a load resistor and ground. The output voltage is taken across the load resistor. The circuit is powered by a positive supply voltage and ground.

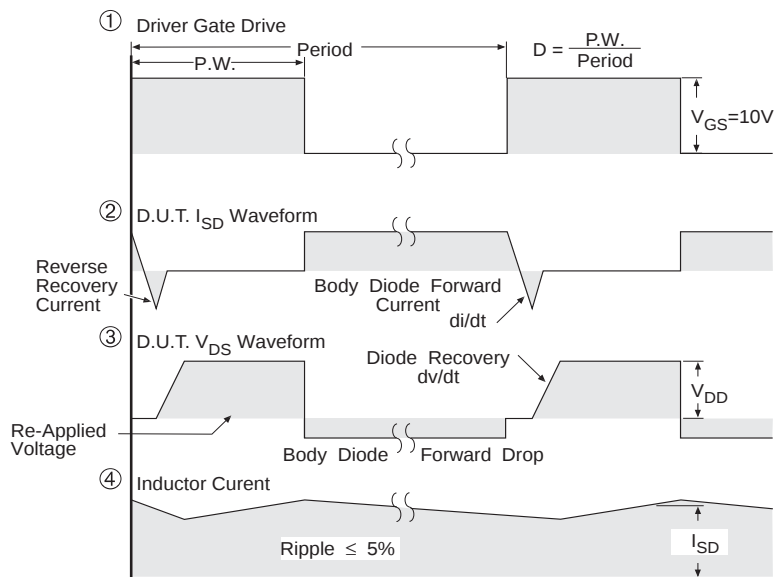
Circuit Layout Considerations

- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance

Current Transformer

- dv/dt controlled by R_G
- I_{SD} controlled by Duty Factor "D"
- D.U.T. - Device Under Test

**** Use P-Channel Driver for P-Channel Measurements**

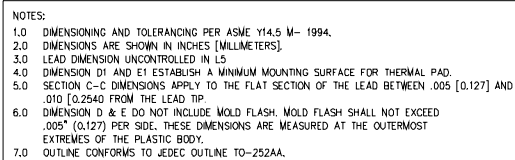


*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14 For N Channel HEXFETS

International
IOR Rectifier

Dimensions are shown in millimeters (inches)



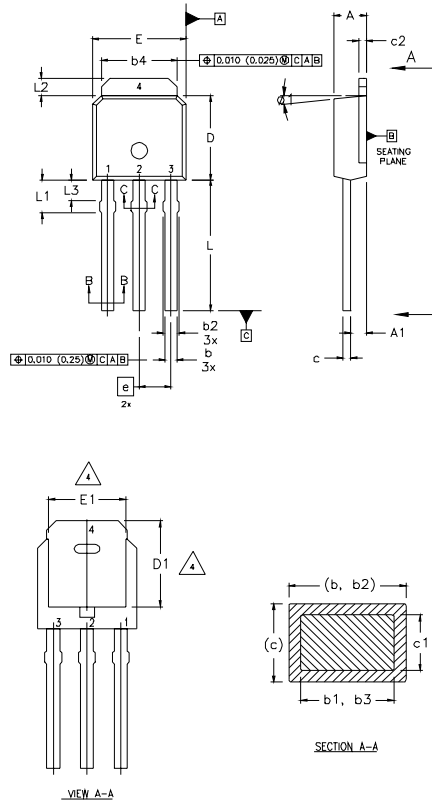
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1		0.13		.005	
b	0.64	0.89	.025	.035	5
b1	0.64	0.79	.025	0.031	5
b2	0.76	1.14	.030	.045	
b3	.945	1.46	.198	.214	
c	0.46	0.61	.018	.024	5
c1	0.41	0.56	.016	.022	5
c2	.046	0.39	.018	.035	5
D	5.97	6.22	.235	.245	
D1	5.21		.209		4
E	6.35	6.75	.250	.265	6
E1	4.32		.170		4
e	2.29		.090 BSC		
H	9.40	10.17	.370	.410	
L1	2.74 REF.		.108 REF.		
L2	.051 BSC		.020 BSC		
L3	0.89	1.02	.035	.060	
L4		1.52		.040	
L5	1.14	1.52	.045	.060	3
a	0°	10°	0°	10°	
a1	0°	15°	0°	15°	

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

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I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
- 5 LEAD DIMENSION UNCONTROLLED IN L3.
- 6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
- 7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
- 8 CONTROLLING DIMENSION : INCHES.

LEAD ASSIGNMENTS

HEXFET

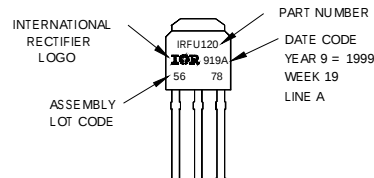
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
b1	0.64	0.79	0.025	0.031	4
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	
b4	5.00	5.46	0.195	0.215	4
c	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	.046	0.86	0.018	0.035	
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	—	0.205	—	4
E	6.35	6.73	0.250	0.265	3, 4
E1	4.32	—	0.170	—	4
e	2.29		0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	4
L3	1.14	1.52	0.045	0.060	5
ø1	0"	15"	0"	15"	

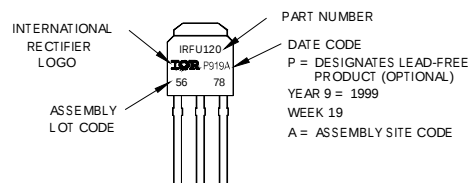
I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW19, 1999
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line
position indicates "Lead-Free"



OR

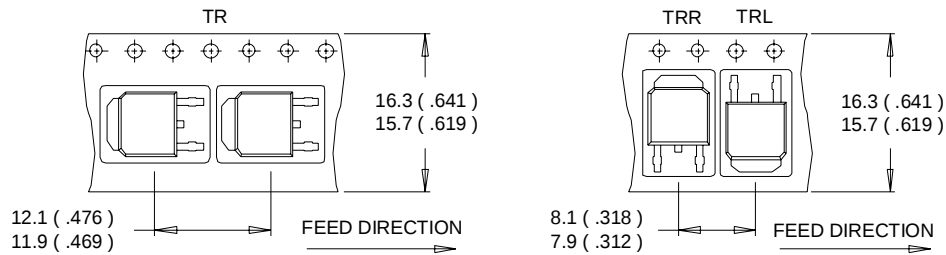


IRFR/U210PbF

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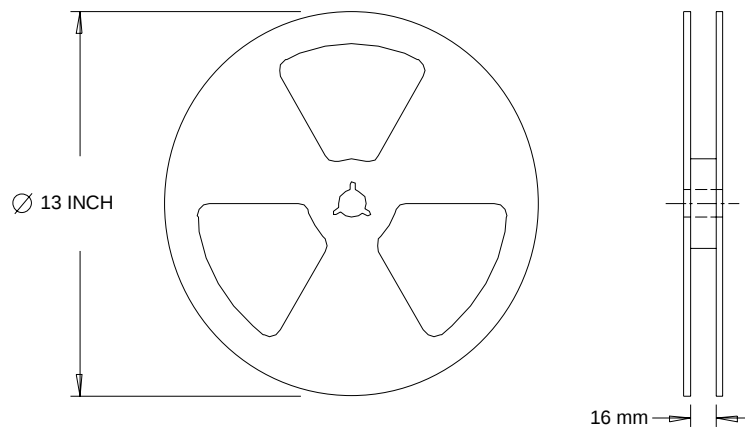
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Data and specifications subject to change without notice.

International
IOR Rectifier

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