Data Sheet | September 22, 2006 | FN6312.0

Dual Micropower Single Supply Rail-to-Rail Input and Output (RRIO) Precision Op-Amp

The ISL28286 and ISL28486 are Dual and Quad channel micropower precision operational amplifiers optimized for single supply operation at 5V down to 2.4V. For equivalent performance in a single channel op-amp reference EL8186.

The ISL28286 and ISL28486 feature an Input Range Enhancement Circuit (IREC) which enables both parts to maintain CMRR performance for input voltages equal to the positive and negative supply rails. The input signal is capable of swinging 10% above the positive supply rail and to ground with only a slight degradation of the CMRR performance. The output operation is rail to rail.

Both parts draw minimal supply current while meeting excellent DC-accuracy, AC-performance, noise and output drive specifications.

The ISL28286 and ISL28486 can be operated from a single lithium cell or two Ni-Cd batteries. The input range includes both positive and negative rail.

Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
ISL28286FUZ (See Note)	8286Z	50/Tube	10 Ld MSOP (Pb-free)	MDPOO43
ISL28286FUZ-T7 (See Note)	8286Z	7” (1500 pcs)	10 Ld MSOP (Pb-free)	MDP0043
Coming Soon ISL28486FAZ (Note)	28486FAZ	97/Tube	16 Ld QSOP (Pb-free)	MDP0040
Coming Soon ISL28486FAZ-T7 (Note)	28486FAZ	7” (1000 pcs)	16 Ld QSOP (Pb-free)	MDP0040

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

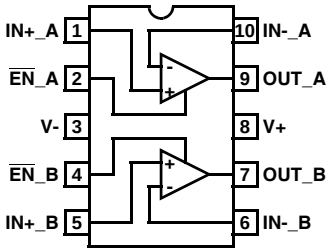
- 120µA typ supply current for both channels
- 600µV max offset voltage
- 500pA typ input bias current
- 400kHz gain-bandwidth product
- 115dB PSRR and CMRR
- Single supply operation down to 2.4V
- Input is capable of swinging above V+ and to V- (ground sensing)
- Rail-to-rail input and output (RRIO)
- Pb-free plus anneal available (RoHS compliant)

Applications

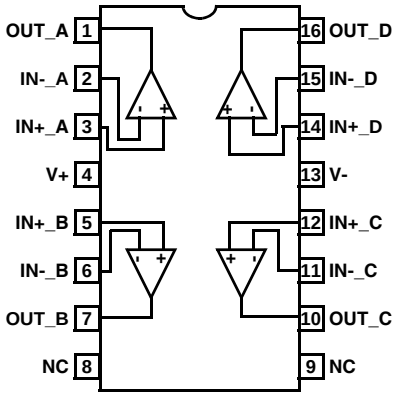
- Battery- or solar-powered systems
- 4mA to 25mA current loops
- Handheld consumer products
- Medical devices
- Thermocouple amplifiers
- Photodiode pre-amps
- pH probe amplifiers

Pinouts

ISL28286
(10 LD MSOP)
TOP VIEW



ISL28486
(16 LD QSOP)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage 5.5V
Supply Turn On Voltage Slew Rate 1V/µs
Differential Input Current 5mA
Differential Input Voltage 0.5V
Input Voltage . . . . . V- - 0.5V to V+ + 0.5V
ESD tolerance, Human Body Model 3kV
ESD tolerance, Machine Model 300V

Output Short-Circuit Duration . . . . . .Indefinite
Ambient Operating Temperature Range . . . . . .-40°C to +125°C
Storage Temperature Range . . . . . .-65°C to +150°C
Operating Junction Temperature . . . . . .+125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, T_A = +25°C unless otherwise specified.
Boldface limits apply over the operating temperature range, -40°C to +125°C, temperature data guaranteed by characterization

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage		-600 **-650**	±20	600 **650**	µV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability			1.2		µV/Mo
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Drift vs Temperature			0.3		µV/°C
I_{OS}	Input Offset Current		-1.5 **-1.5**	±0.25	2.5 **2.5**	nA
I_B	Input Bias Current		-2 **-2.5**	±0.5	2 **2.5**	nA
e_N	Input Noise Voltage Peak-to-Peak	f = 0.1Hz to 10Hz		4.5		μV_{PP}
	Input Noise Voltage Density	f_O = 1kHz		48		nV/√Hz
i_N	Input Noise Current Density	f_O = 1kHz		0.18		pA/√Hz
CMIR	Input Voltage Range	Guaranteed by CMRR test	**0**		**5**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 5V	90 **80**	115		dB
PSRR	Power Supply Rejection Ratio	V_+ = 2.4V to 5V	90 **80**	115		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 4.5V, R_L = 100kΩ	275 **275**	500		V/mV
		V_O = 0.5V to 4.5V, R_L = 1kΩ		25		V/mV
V_{OUT}	Maximum Output Voltage Swing	Output low, R_L = 100kΩ		3	6 **30**	mV
		Output low, R_L = 1kΩ		130	175 **225**	mV
		Output high, R_L = 100kΩ	4.990 **4.97**	4.996		V
		Output high, R_L = 1kΩ	4.800 **4.750**	4.880		V
SR+	Positive Slew Rate		0.13 **0.10**	0.17	0.20 **0.25**	V/µs
SR-	Negative Slew Rate		0.10 **0.09**	0.13	0.17 **0.19**	V/µs

Electrical Specifications V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, T_A = +25°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C, temperature data guaranteed by characterization (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
GBW	Gain Bandwidth Product			400		kHz
$I_{S,ON}$	Supply Current, Enabled	All channels enabled.		120	156 **175**	µA
$I_{S,OFF}$	Supply Current, Disabled	All channels disabled.		4	7 **9**	µA
I_{SC}^+	Short Circuit Sourcing Capability	R_L = 10Ω	29 **23**	31		mA
I_{SC}^-	Short Circuit Sinking Capability	R_L = 10Ω	24 **19**	26		mA
V_S	Minimum Supply Voltage		**2.4**			V
V_{INH}	Enable Pin High Level		**2**			V
V_{INL}	Enable Pin Low Level				**0.8**	V
I_{ENH}	Enable Pin Input Current	V_{EN} = 5V		0.7	1.3 **1.5**	µA
I_{ENL}	Enable Pin Input Current	V_{EN} = 0V	**-0.1**	0	**+0.1**	µA

Typical Performance Curves

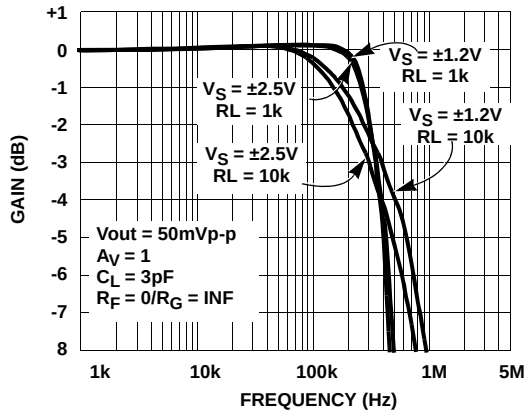


FIGURE 1. FREQUENCY RESPONSE vs SUPPLY VOLTAGE

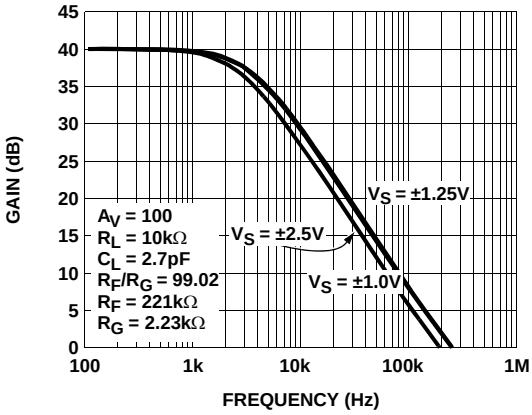


FIGURE 2. FREQUENCY RESPONSE vs SUPPLY VOLTAGE

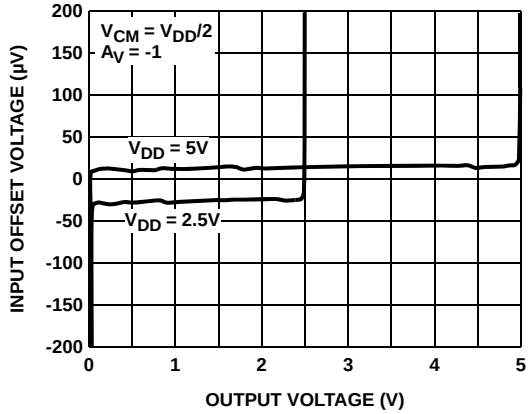


FIGURE 3. INPUT OFFSET VOLTAGE vs OUTPUT VOLTAGE

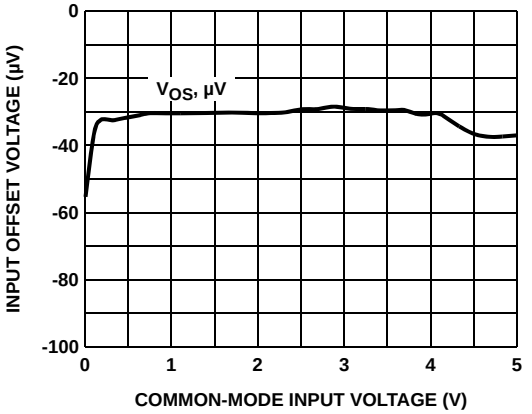


FIGURE 4. INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

Typical Performance Curves (Continued)

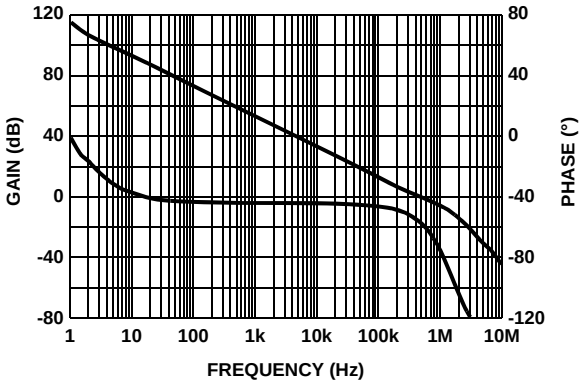


FIGURE 5. A_{VOL} vs FREQUENCY @ 100kΩ LOAD

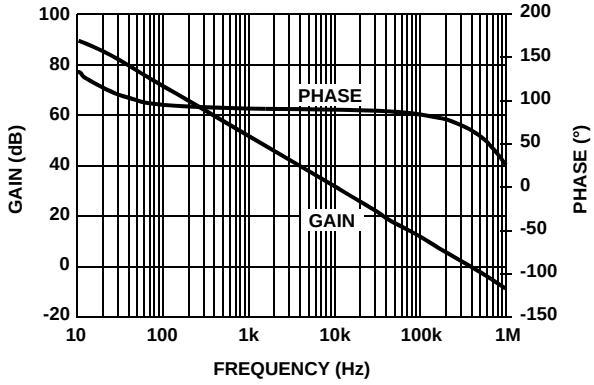


FIGURE 6. A_{VOL} vs FREQUENCY @ 1kΩ LOAD

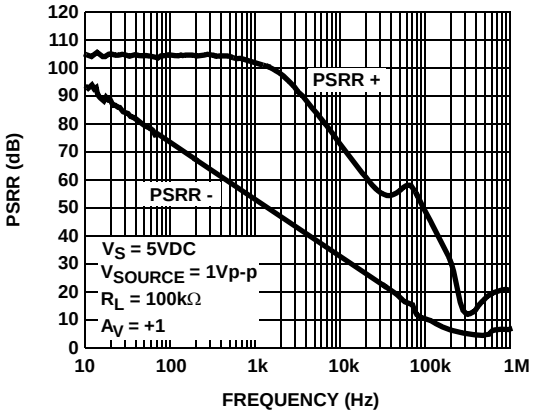


FIGURE 7. PSRR vs FREQUENCY

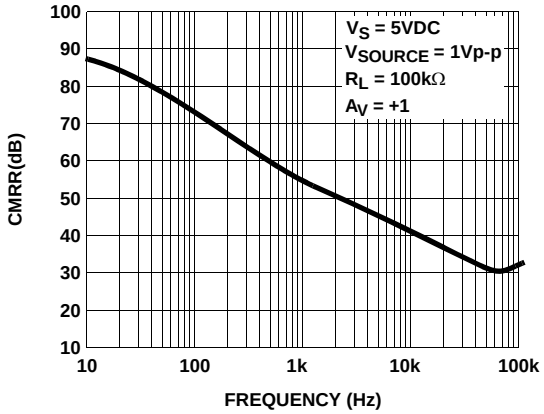


FIGURE 8. CMRR vs FREQUENCY

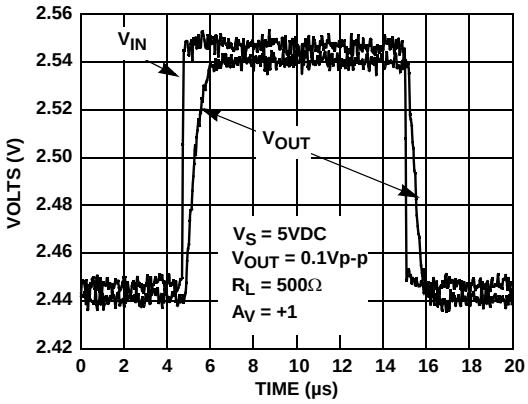


FIGURE 9. SMALL SIGNAL TRANSIENT RESPONSE

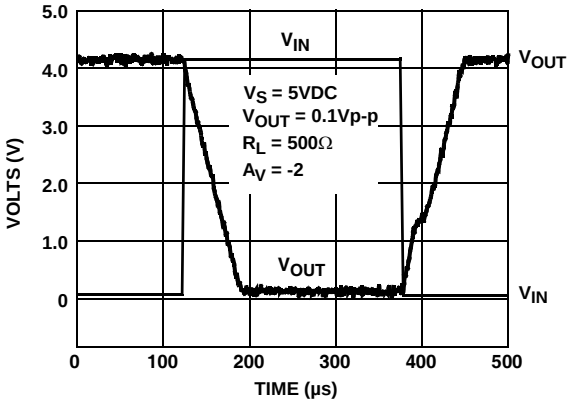


FIGURE 10. LARGE SIGNAL TRANSIENT RESPONSE

Typical Performance Curves (Continued)

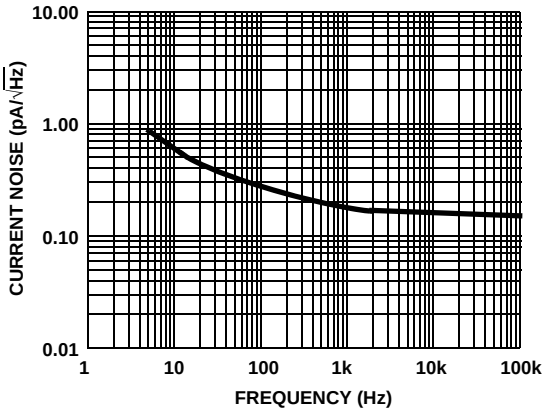


FIGURE 11. CURRENT NOISE vs FREQUENCY

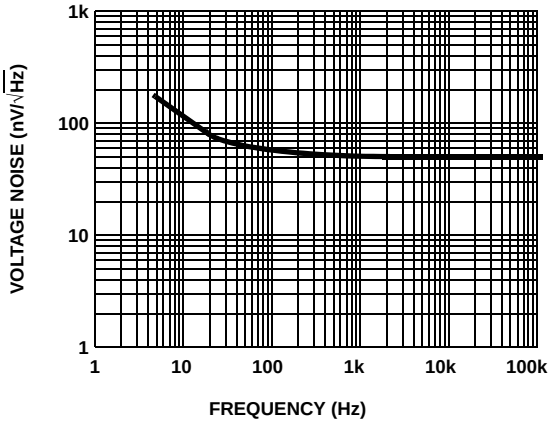


FIGURE 12. VOLTAGE NOISE vs FREQUENCY

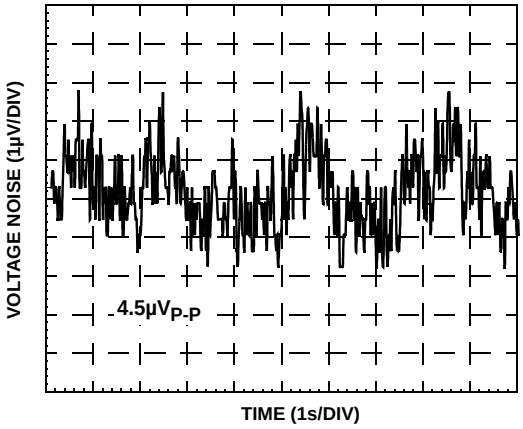


FIGURE 13. 0.1Hz TO 10Hz INPUT VOLTAGE NOISE

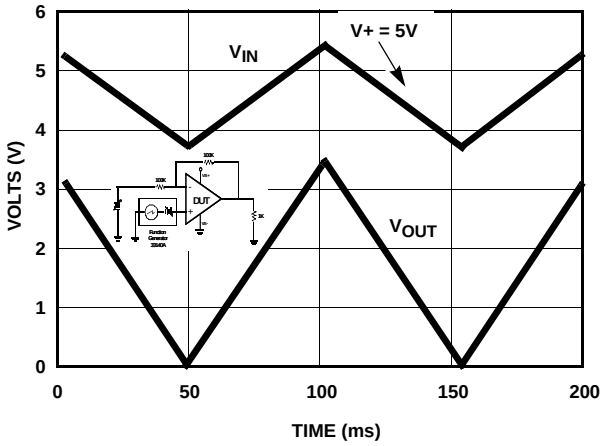


FIGURE 14. INPUT VOLTAGE SWING ABOVE THE V+ SUPPLY

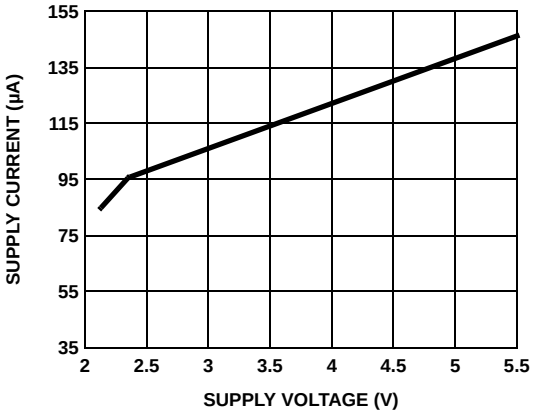


FIGURE 15. SUPPLY CURRENT vs SUPPLY VOLTAGE

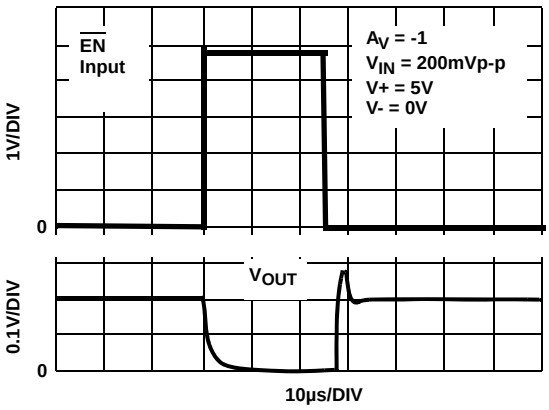


FIGURE 16. ENABLE TO OUTPUT DELAY TIME

Typical Performance Curves (Continued)

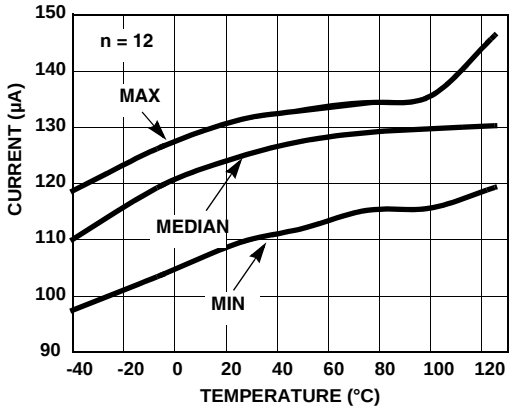


FIGURE 17. SUPPLY CURRENT vs TEMPERATURE V_S = ±2.5V ENABLED. R_L = INF

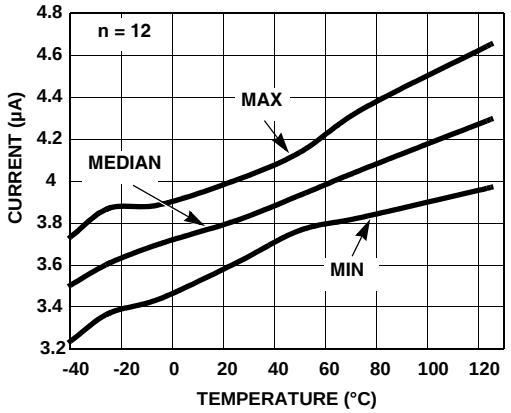


FIGURE 18. SUPPLY CURRENT vs TEMPERATURE V_S = ±2.5V DISABLED. R_L = INF

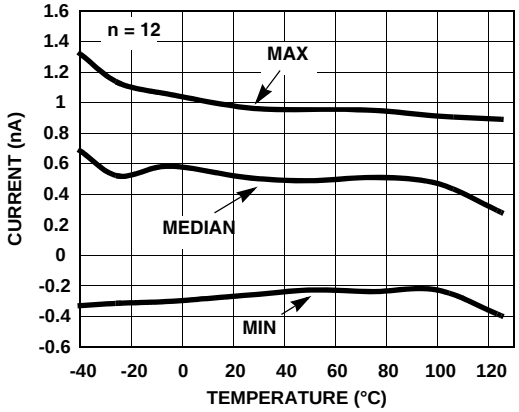


FIGURE 19. I BIAS(+) vs TEMPERATURE V_S = ±2.5V

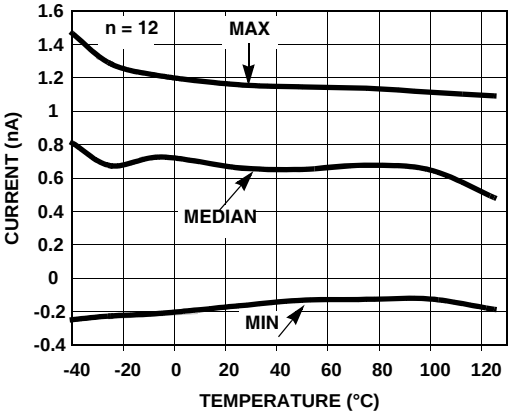


FIGURE 20. I BIAS(+) vs TEMPERATURE V_S = ±1.2V

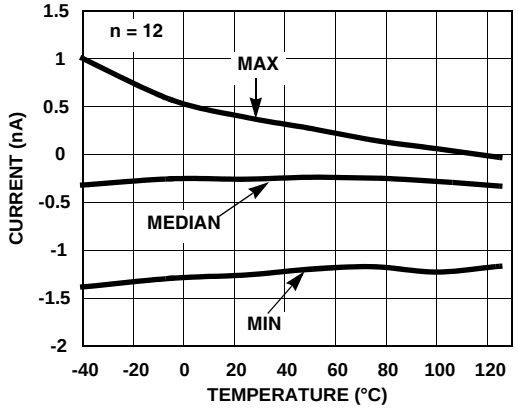


FIGURE 21. I BIAS(-) vs TEMPERATURE V_S = ±2.5V

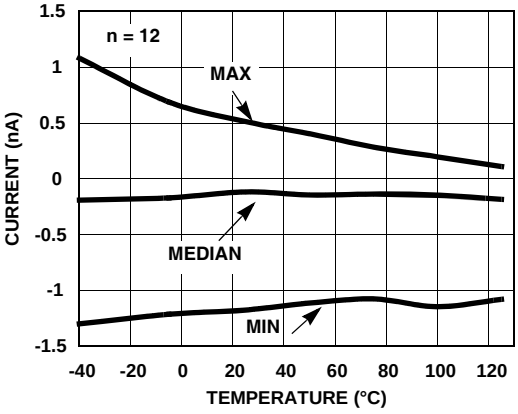


FIGURE 22. I BIAS(-) vs TEMPERATURE V_S = ±1.2V

Typical Performance Curves (Continued)

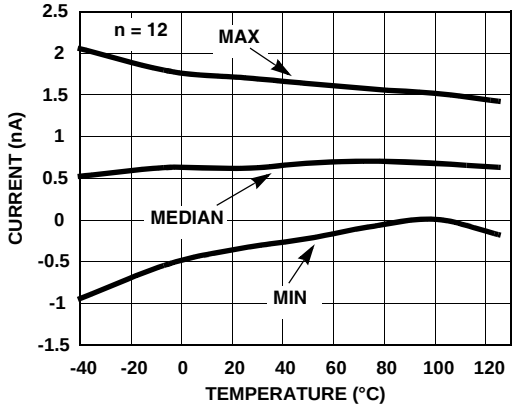


FIGURE 23. INPUT OFFSET CURRENT vs TEMPERATURE V_S = ±2.5V

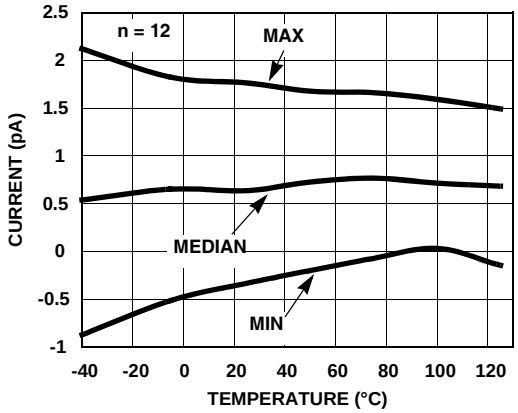


FIGURE 24. INPUT OFFSET CURRENT vs TEMPERATURE V_S = ±1.2V

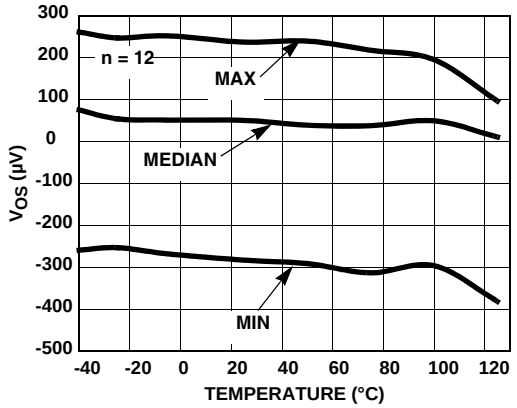


FIGURE 25. INPUT OFFSET VOLTAGE vs TEMPERATURE V_S = ±2.5V

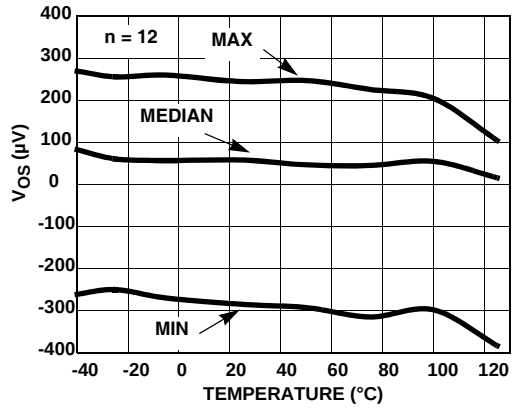


FIGURE 26. INPUT OFFSET VOLTAGE vs TEMPERATURE\ V_S = ±1.2V

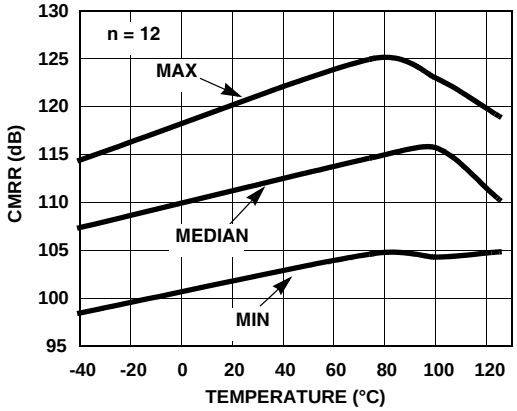


FIGURE 27. CMRR vs TEMPERATURE V_{CM} = +2.5V TO -2.5V

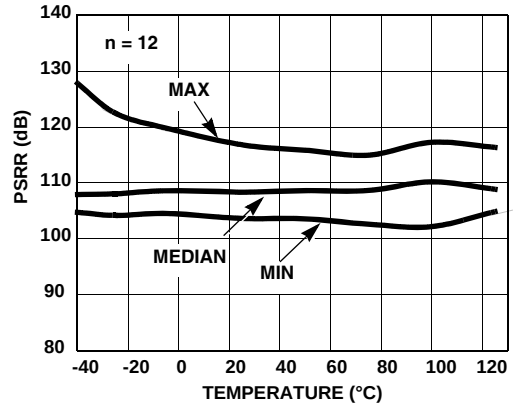


FIGURE 28. PSRR vs TEMPERATURE V_S = ±2.5V

Typical Performance Curves (Continued)

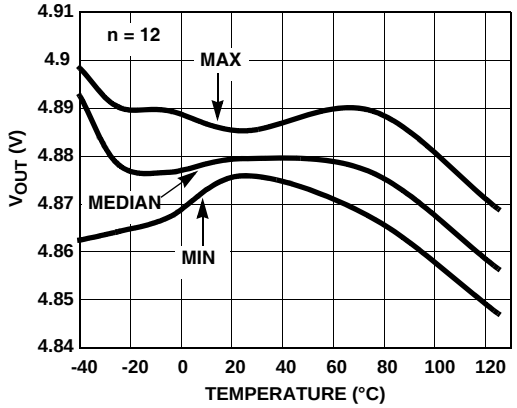


FIGURE 29. POSITIVE V_{OUT} vs TEMPERATURE R_L = 1k V_S = ±2.5V

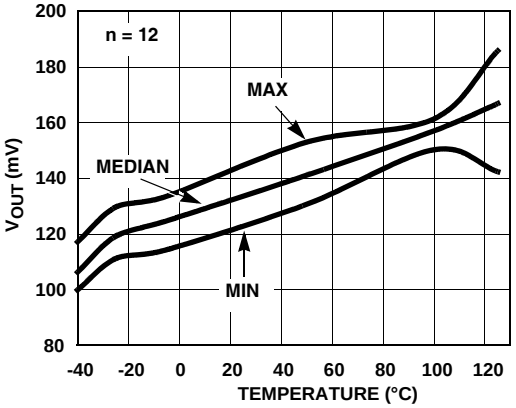


FIGURE 30. NEGATIVE V_{OUT} vs TEMPERATURE R_L = 1k V_S = ±2.5V

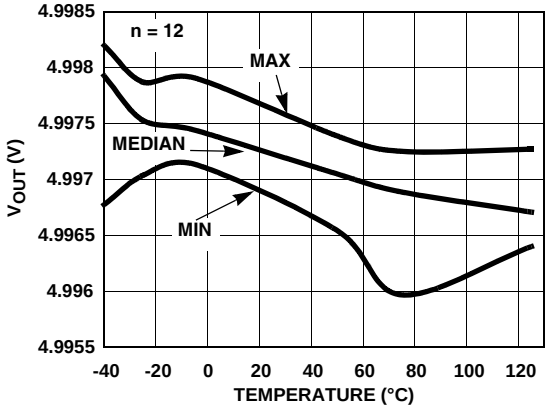


FIGURE 31. POSITIVE V_{OUT} vs TEMPERATURE R_L = 100k V_S = ±2.5V

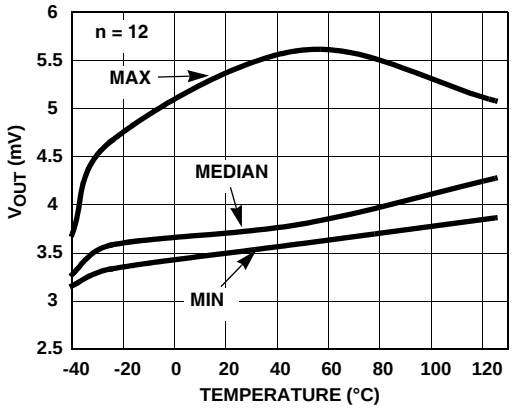


FIGURE 32. NEGATIVE V_{OUT} vs TEMPERATURE R_L = 100k V_S = ±2.5V

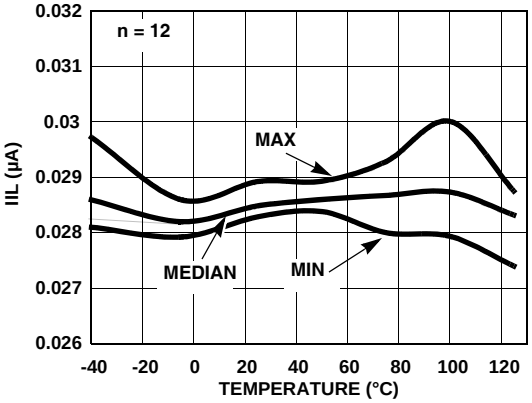


FIGURE 33. I_{IL} (EN) vs TEMPERATURE V_S = ±2.5V

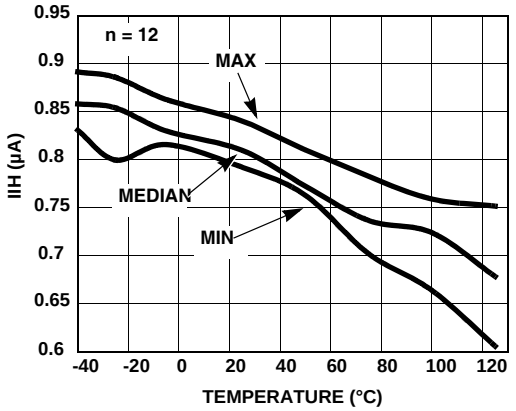


FIGURE 34. I_{IH} (EN) vs TEMPERATURE V_S = ±2.5V

Typical Performance Curves (Continued)

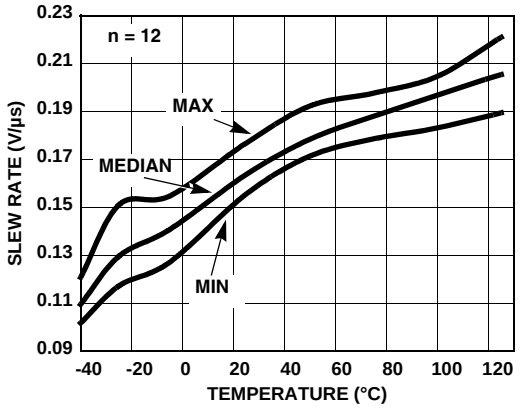


FIGURE 35. + SLEW RATE vs TEMPERATURE V_S = ±2.5V INPUT = ±0.75V A_V = 2

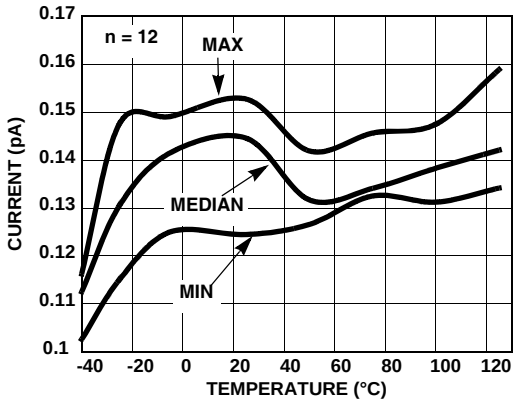


FIGURE 36. - SLEW RATE vs TEMPERATURE V_S = ±2.5V INPUT = ±0.75V A_V = 2

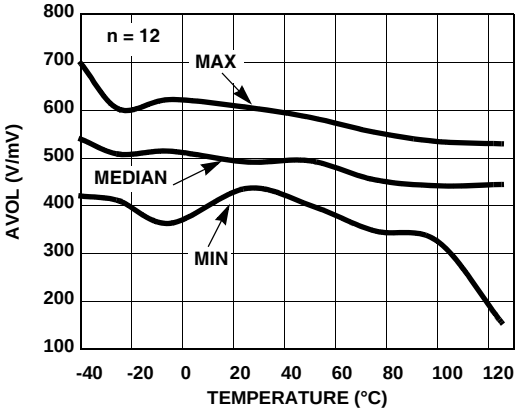


FIGURE 37. AVOL CH A vs TEMPERATURE RL = 100K VO = ±2V V_S = ±2.5V

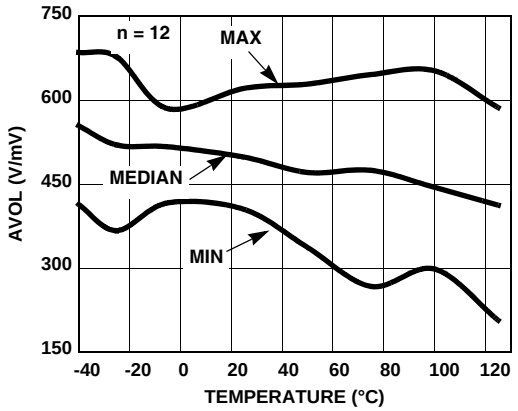


FIGURE 38. AVOL CH B vs TEMPERATURE RL = 100K VO = ±2V V_S = ±2.5V

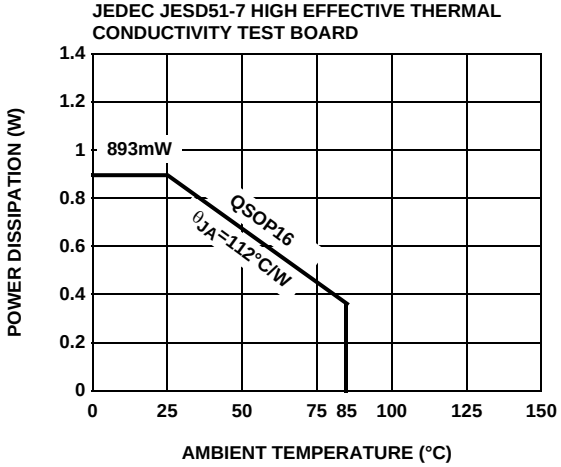


FIGURE 39. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

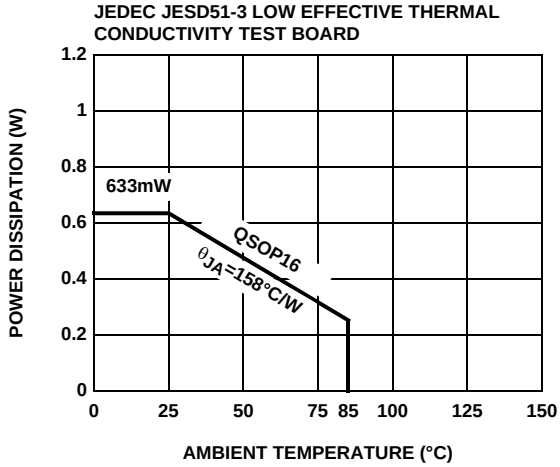


FIGURE 40. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Typical Performance Curves (Continued)

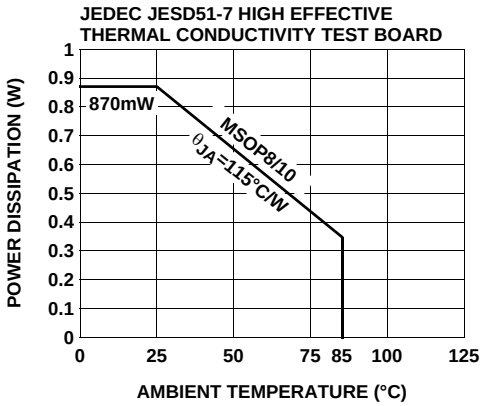


FIGURE 41. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

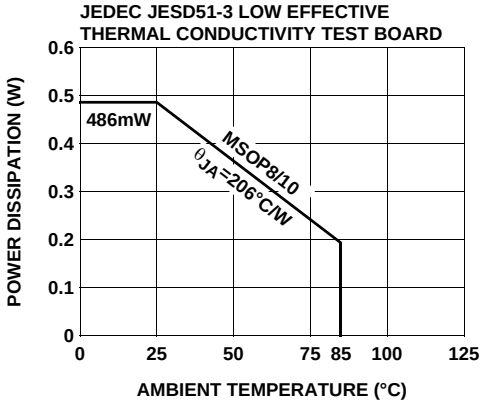
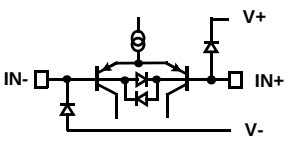


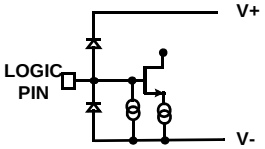
FIGURE 42. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Pin Descriptions

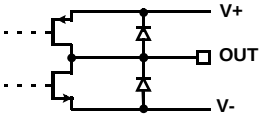
ISL28286 (10 LD MSOP)	ISL28486 (16 LD QSOP)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1	3	IN+_A	Circuit 1	Amplifier A non-inverting input
2		$\overline{EN}$_A	Circuit 2	Amplifier A enable pin internal pull-down; Logic “1” selects the disabled state; Logic “0” selects the enabled state.
3	13	V-	Circuit 4	Negative power supply
4		$\overline{EN}$_B	Circuit 2	Amplifier B enable pin with internal pull-down; Logic “1” selects the disabled state; Logic “0” selects the enabled state.
5	5	IN+_B	Circuit 1	Amplifier B non-inverting input
6	6	IN-_B	Circuit 1	Amplifier B inverting input
7	7	OUT_B	Circuit 3	Amplifier B output
8	4	V+	Circuit 4	Positive power supply
9	1	OUT_A	Circuit 3	Amplifier A output
10	2	IN-_A	Circuit 1	Amplifier A inverting input
	10	OUT_C	Circuit 3	Amplifier C output
	11	IN-_C	Circuit 1	Amplifier C inverting input
	12	IN+_C	Circuit 1	Amplifier C non-inverting input
	14	IN+_D	Circuit 1	Amplifier D non-inverting input
	15	IN-_D	Circuit 1	Amplifier D inverting input
	16	OUT_D	Circuit 3	Amplifier D output
	8, 9	NC	-	No internal connection



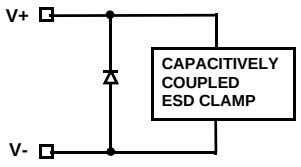
CIRCUIT 1



CIRCUIT 2



CIRCUIT 3



CIRCUIT 4

Applications Information

Introduction

The ISL28286 and ISL28486 are enhanced rail-to-rail input micropower precision operational amplifiers with an enable feature. The part is designed to operate from single supply (2.4V to 5.0V) or dual supply (±1.2V to ±2.5V). The device is capable of swinging 10% above the positive supply rail and to ground. The parts maintains CMRR performance for input voltages equal to the positive supply. The output operation can swing within about 4mV of the supply rails with a 100kΩ load (reference Figures 29 through 32).

Rail-to-Rail Input

The input common-mode voltage range of both parts goes from 10mV above the negative supply to the positive supply without introducing additional offset errors or degrading performance associated with a conventional rail-to-rail input operational amplifier. Many rail-to-rail input stages use two differential input pairs, a long-tail PNP (or PFET) and an NPN (or NFET). Severe penalties have to be paid for this circuit topology. As the input signal moves from one supply rail to another, the operational amplifier switches from one input pair to the other causing drastic changes in input offset voltage and an undesired change in magnitude and polarity of input offset current.

The ISL28286 and ISL28486 achieves input rail-to-rail without sacrificing important precision specifications and degrading distortion performance. The devices' input offset voltage exhibits a smooth behavior throughout the entire common-mode input range. The input bias current versus the common-mode voltage range gives us an undistorted behavior from the negative rail and 10% higher than the V+ rail (0.5V higher than V+ when V+ equals 5V).

Input Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. Both parts have additional back-to-back diodes across the input terminals. If overdriving the inputs is necessary, the external input current must never exceed 5mA. External series resistors may be used as an external protection to limit excessive external voltage and current from damaging the inputs.

Input Bias Current Compensation

The input bias currents are decimated down to a typical of 500pA while maintaining an excellent bandwidth for a micro-power operational amplifier. Inside the ISL28286 and ISL28478 is an input bias canceling circuit. The input stage transistors are still biased with an adequate current for speed but the canceling circuit sinks most of the base current, leaving a small fraction as input bias current.

Rail-to-Rail Output

A pair of complementary MOSFET devices are used to achieve the rail-to-rail output swing. The NMOS sinks current to swing the output in the negative direction. The PMOS sources current to swing the output in the positive direction. Both parts with a 100kΩ load will swing to within 4mV of the supply rails.

Enable/Disable Feature

The ISL28286 and ISL28486 offer an $\overline{EN}$ pin that disables the device when pulled up to at least 2.0V. In the disabled state (output in a high impedance state), the part consumes typically 4µA. By disabling the part, multiple parts can be connected together as a MUX. The outputs are tied together in parallel and a channel can be selected by the $\overline{EN}$ pin. The $\overline{EN}$ pin also has an internal pull down. If left open, the $\overline{EN}$ pin will pull to the negative rail and the device will be enabled by default.

Using Only One Channel

The ISL28286 and ISL28486 are Dual and Quad channel op-amps. If the application only requires one channel when using the ISL28286 or less than 4 channels when using the ISL28486, the user must configure the unused channel (s) to prevent them from oscillating. The unused channel (s) will oscillate if the input and output pins are floating. This will result in higher than expected supply currents and possible noise injection into the channel being used. The proper way to prevent this oscillation is to short the output to the negative input and ground the positive input (as shown in Figure 43).

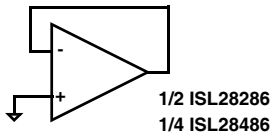


FIGURE 43. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

Proper Layout Maximizes Performance

To achieve the maximum performance of the high input impedance and low offset voltage of the ISL28286 and ISL28486, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board. When input leakage current is a concern, the use of guard rings around the amplifier inputs will further reduce leakage currents. Figure 44 shows a guard ring example for a unity gain amplifier that uses the low impedance amplifier output at the same voltage as the high impedance input to eliminate surface leakage. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. For further reduction of leakage currents, components can be mounted

to the PC board using Teflon standoff insulators.

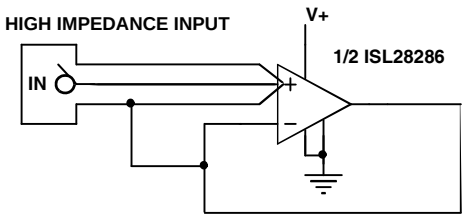


FIGURE 44. GUARD RING EXAMPLE FOR UNITY GAIN AMPLIFIER

Example Application

Thermocouples are the most popular temperature-sensing device because of their low cost, interchangeability, and ability to measure a wide range of temperatures. The ISL28286 (Figure 45) is used to convert the differential thermocouple voltage into single-ended signal with 10X gain. The ISL28286's rail-to-rail input characteristic allows the thermocouple to be biased at ground and the converter to run from a single 5V supply.

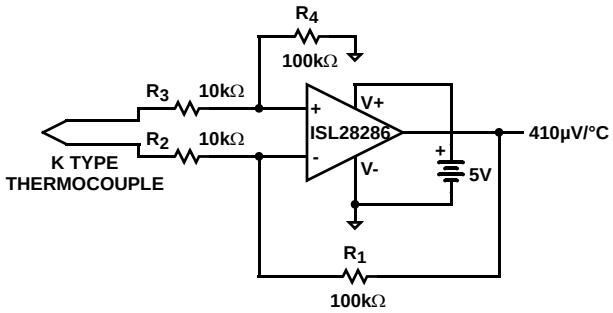


FIGURE 45. THERMOCOUPLE AMPLIFIER

Current Limiting

The ISL28286 and ISL28486 have no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the Absolute Maximum Rating for output current or power dissipation, potentially resulting in the destruction of the device.

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related as follows:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} x PD_{MAXTOTAL}) \quad \text{(EQ. 1)}$$

where:

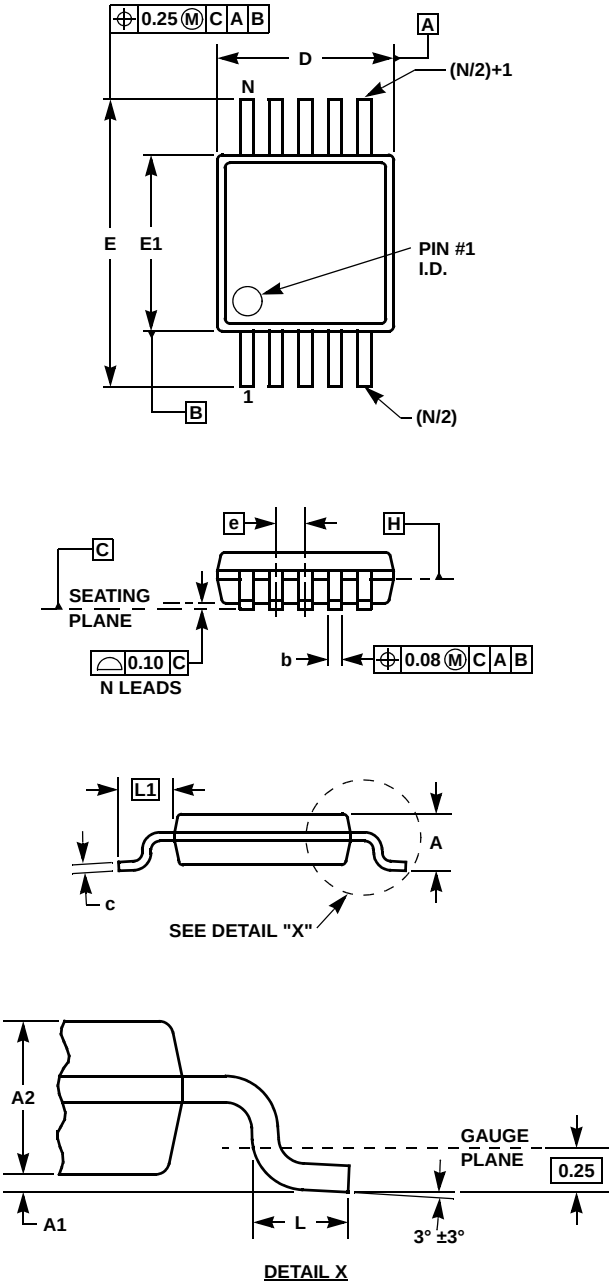
- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated as follows:

$$PD_{MAX} = 2*V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Supply voltage
- I_{MAX} = Maximum supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

Mini SO Package Family (MSOP)



MDP0043

MINI SO PACKAGE FAMILY

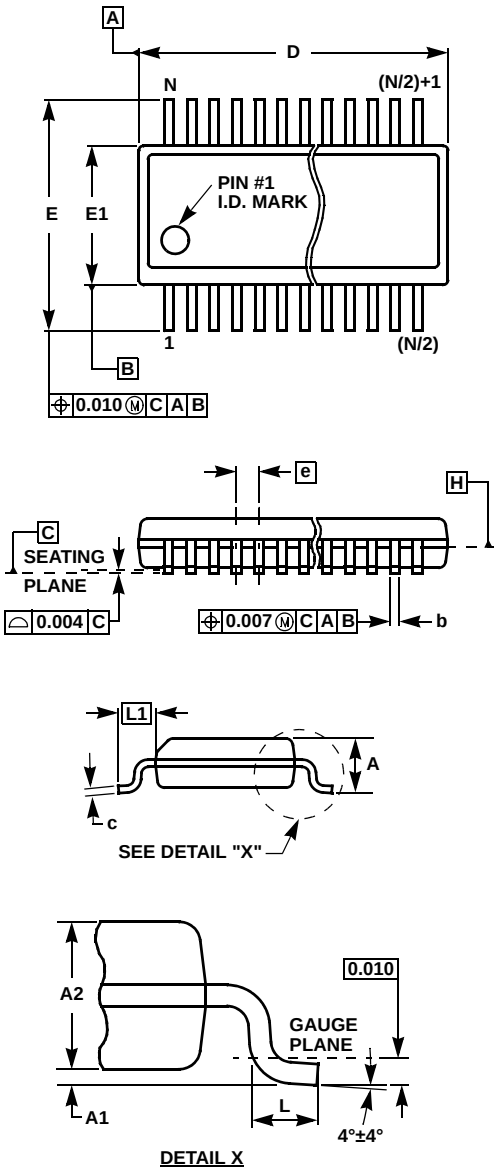
SYMBOL	MSOP8	MSOP10	TOLERANCE	NOTES
A	1.10	1.10	Max.	-
A1	0.10	0.10	±0.05	-
A2	0.86	0.86	±0.09	-
b	0.33	0.23	+0.07/-0.08	-
c	0.18	0.18	±0.05	-
D	3.00	3.00	±0.10	1, 3
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

Rev. C 6/99

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

Quarter Size Outline Plastic Packages Family (QSOP)



MDP0040

QUARTER SIZE OUTLINE PLASTIC PACKAGES FAMILY

SYMBOL	QSOP16	QSOP24	QSOP28	TOLERANCE	NOTES
A	0.068	0.068	0.068	Max.	-
A1	0.006	0.006	0.006	±0.002	-
A2	0.056	0.056	0.056	±0.004	-
b	0.010	0.010	0.010	±0.002	-
c	0.008	0.008	0.008	±0.001	-
D	0.193	0.341	0.390	±0.004	1, 3
E	0.236	0.236	0.236	±0.008	-
E1	0.154	0.154	0.154	±0.004	2, 3
e	0.025	0.025	0.025	Basic	-
L	0.025	0.025	0.025	±0.009	-
L1	0.041	0.041	0.041	Basic	-
N	16	24	28	Reference	-

Rev. E 3/01

NOTES:

1. Plastic or metal protrusions of 0.006” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.