

3A DDR Bus Termination Regulator

Features

- V_{CNTL} Supply Voltage: 3.3V to 5.5V
- Termination Supply Voltage: 1.8V to 3.6V
- Support Both DDR I (1.25V_{TT}) and DDR II (0.9V_{TT}) Requirements
- Requires Only 20μF Ceramic Output Capacitor
- Low Output Offset
- 3A Source and Sink Current
- Low External Component Count
- No Inductor Required
- Thermal Shutdown Protection
- Over Current Protection
- Suspend to RAM (STR) Function with High-impedance output
- SOP-8 (FD) Package

Applications

- DDR-SDRAM Termination Voltage
- DDR I / DDR II Termination Voltage
- SSTL-18
- SSTL-2
- SSTL-3

General Description

The G2992 is a linear regulator designed to meet the JEDEC SSTL-18, SSTL-2 and SSTL-3 (Series Stub Termination Logic) specifications for termination of DDR I / II -SDRAM. It contains a high-speed operational amplifier that provides excellent response to the load transients. This device can deliver 3A continuous current in the application such as required for DDR I / II SDRAM termination. The G2992 can easily provide the accurate V_{TT} voltage with two external resistors generating reference voltage. The quiescent current is as low as 750μA @ $V_{CNTL} = 3.3V$. So the power consumption can meet the low power consumption applications. The G2992 also has a shutdown function by setting V_{REF} smaller than 0.2V, that provides Suspend to RAM (STR) functionality. When in the shutdown mode, the V_{TT} output (on V_{OUT} pin) will be tri-state providing a high impedance. A power saving advantage can be obtained in this mode through lowering the quiescent current to 50μA @ $V_{CNTL} = 3.3V$.

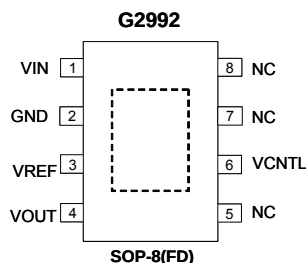
Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Pb free)
G2992F1U	G2992	-40°C to +85°C	SOP-8 (FD)

Note: U: Tape & Reel

(FD): Thermal Pad

Pin Configuration



Typical Application Circuit

