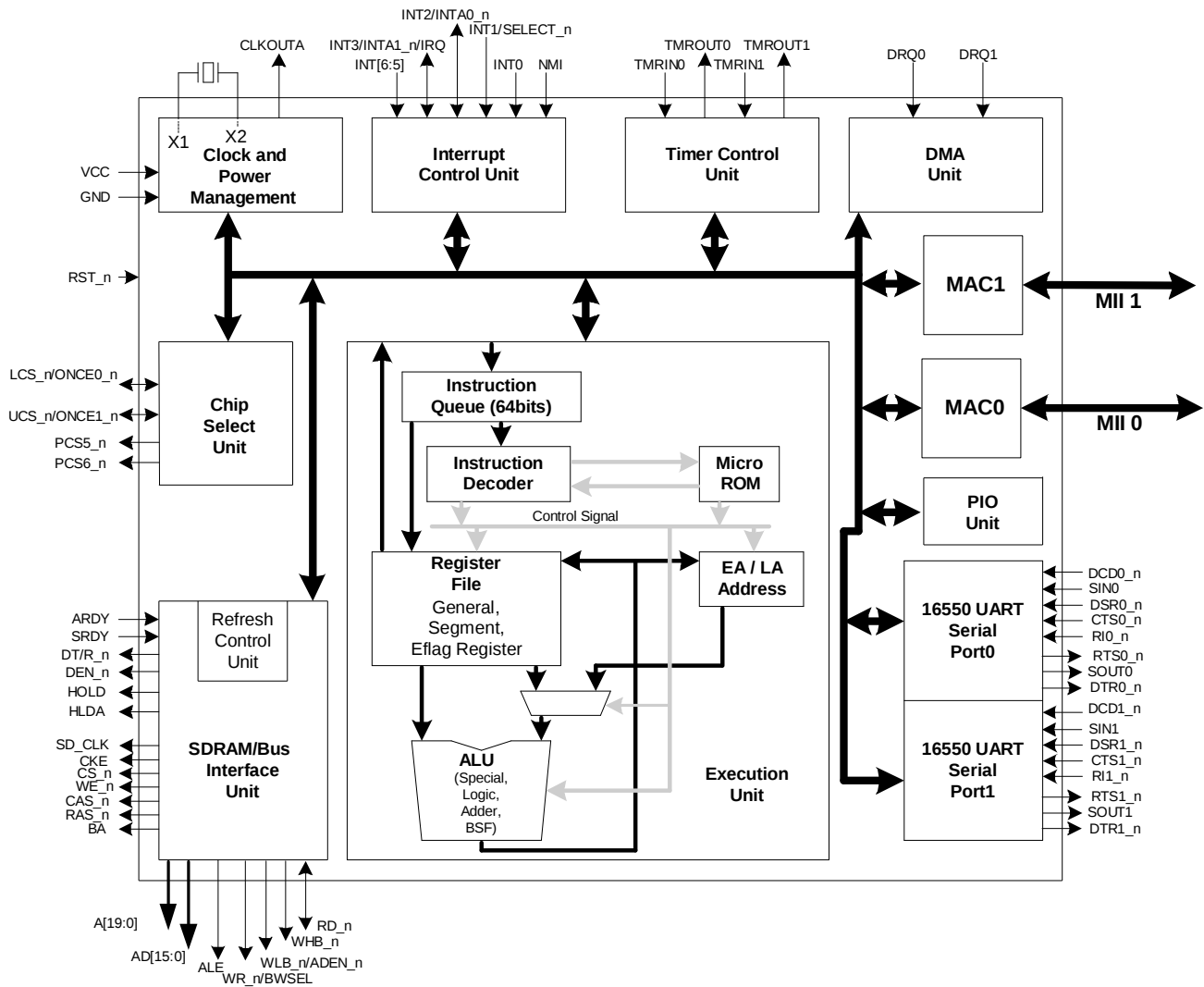


R1620
Brief Sheet
FAST ETHERNET RISC PROCESSOR

1. Features

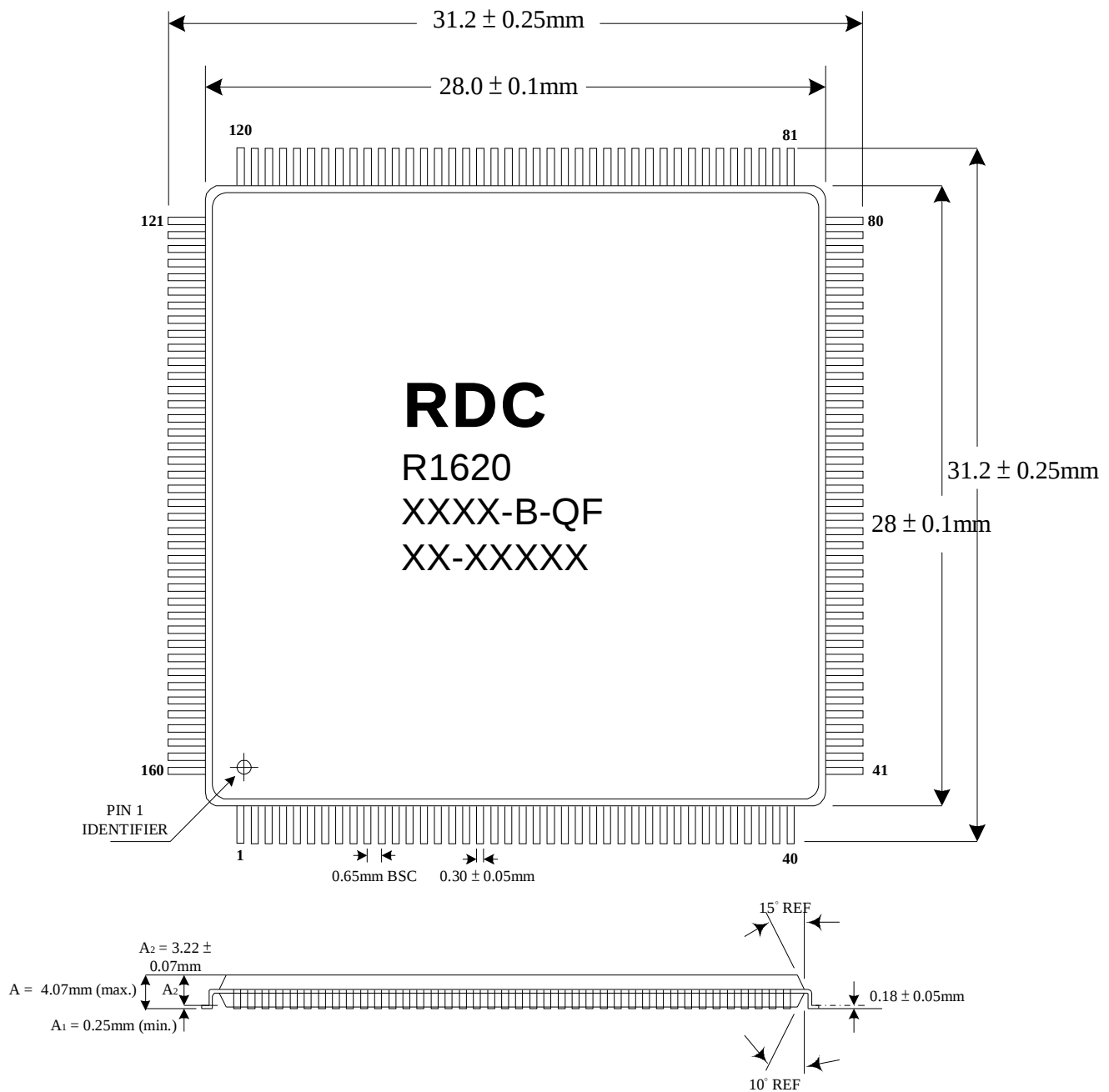
- | Five-stage pipeline
- | RISC architecture
- | Bus interface
 - Multiplexed address and Data bus
 - Supports non-multiplexed address bus A[19:0]
 - 8-bit or 16-bit external bus dynamic access
 - 1M-byte memory address space
 - 64K-byte I/O space
 - Supports an independent bus for slower I/O device
- | Software is compatible with the 80C186 microprocessor
- | Supports two 16550 UART serial channel with 16 bytes FIFO.
- | Supports CPU ID
- | Supports 32 PIO pins
- | SDRAM control Interface
- | Three independent 16-bit timers and one independent programmable watchdog timer
- | The Interrupt controller with six maskable external interrupts and two non-maskable external interrupt
- | Two independent DMA channels
- | Programmable chip-select logic for Memory or I/O bus cycle decoder
- | Programmable wait-state generator
- | With 8-bit or 16-bit Boot ROM bus size
- | 2-Port Fast Ethernet MAC with MII interface
- | With 25MHz input frequency and up to 4x25MHz maximum internal frequency.
- | Compatible with 3.3V I/O.
- | Package Types include 160-pin PQFP and 160-pin LQFP.

2. Block Diagram



3. Package Information

PQFP 160 pins



LQFP 160 pins

