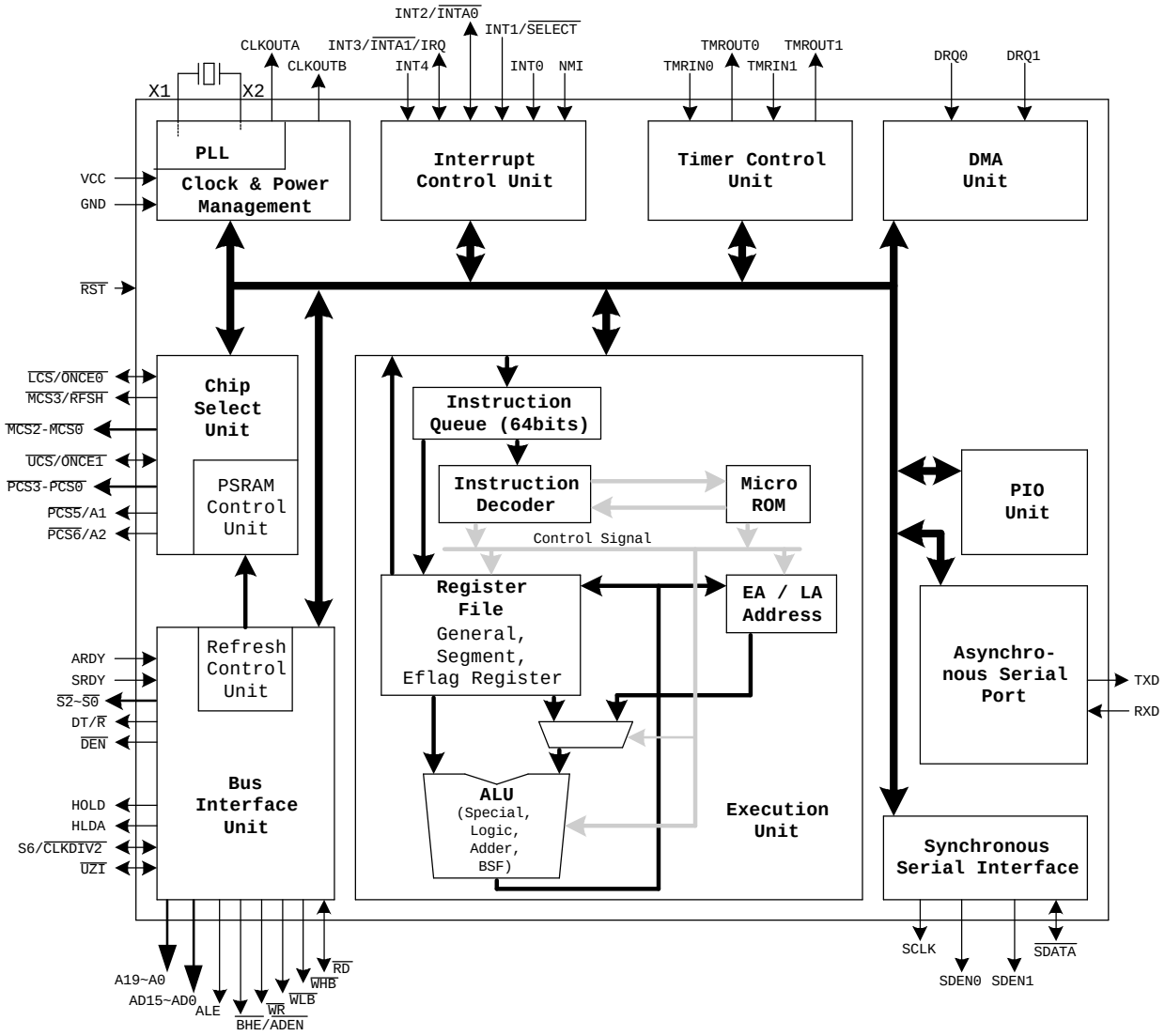
R1100
Brief Sheet
16 BIT RISC MICRO PROCESSOR

1 Features

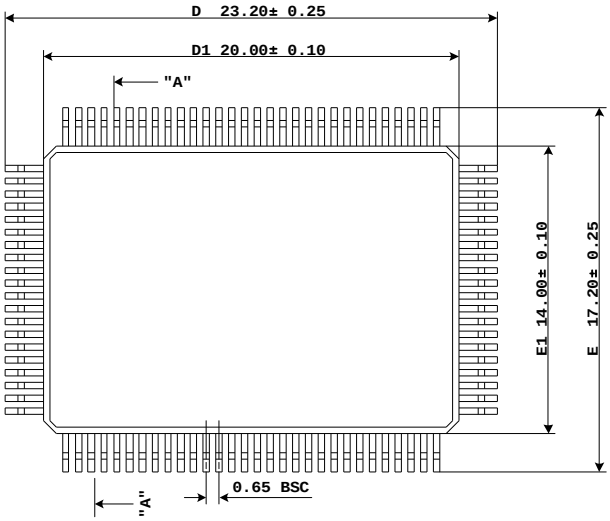
- CPU Core
  - RDC's proprietary RISC architecture
  - Five-stages pipeline
  - Operation frequency: 80MHz
  - Support CPU ID
  - Supports 32 PIO pins
  - External bus, Internal bus and core in the same clock base
- Bus interface
  - Multiplexed address and Data bus
  - With 8-bit or 16-bit boot ROM bus size
  - Supports direct address bus [A19 : A0]
  - 8-bit or 16-bit external bus dynamic access
- ROM/RAM/DRAM Controller and Addressing Space
  - 1M byte memory address space
  - 64K byte I/O space
- Software
  - Software compatible with generic 80C186 microprocessor
- Asynchronous Serial Channels
  - Support two Asynchronous serial channels with hardware handshaking signals.
- Interrupt Controller
  - The interrupt controller with seven maskable external interrupts and one non-maskable external interrupt (NMI)
- Two Independent DMA Channels
- Integrate PLL(*1~*8)
- Programmable Chip-select Logic
  - Programmable chip-select logic for Memory or I/O bus cycle decoder
- Programmable Wait-state Generator
- Counter/Timers
  - Three independent 16-bit timers and one independent programmable watchdog timer
- Operating Voltage Range
  - Operation voltage: 3.3V
  - I/O pin input voltage: 3.3V ~ 5V
  - I/O pin output voltage: 3.3V
- Package Type
  - 100 Pin PQFP & LQFP
- A Green Product

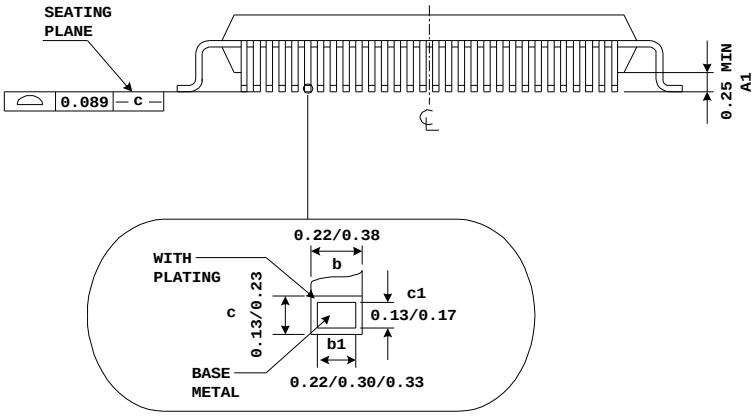
2. Block Diagram

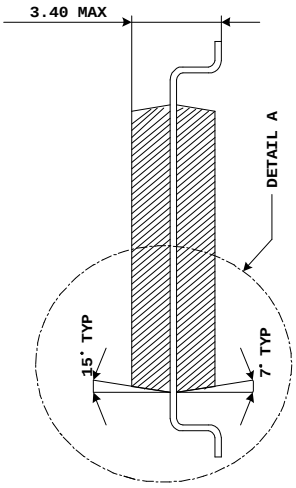


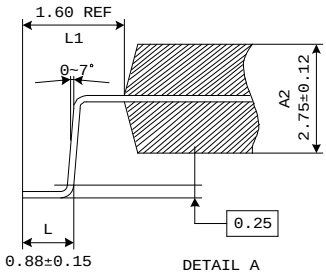
3. Package Information

100 Pin PQFP

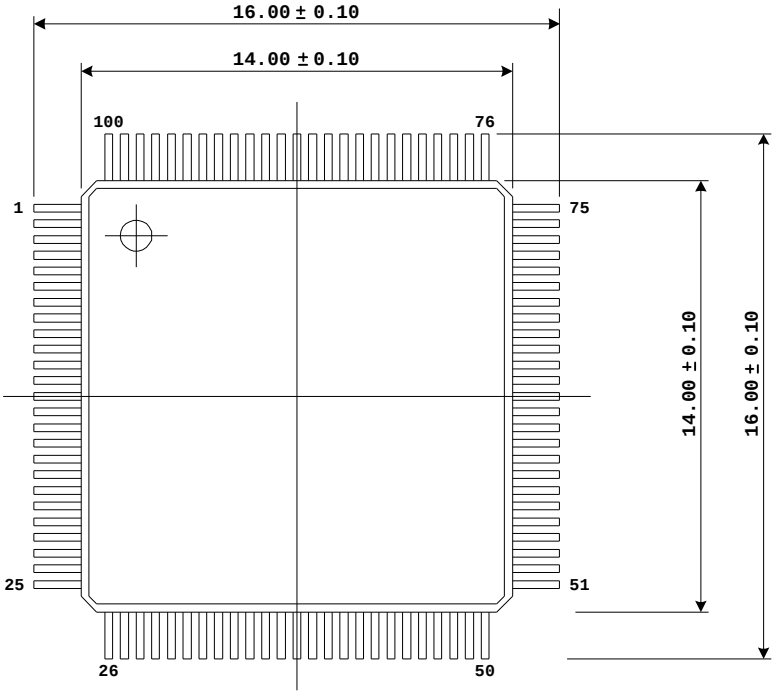


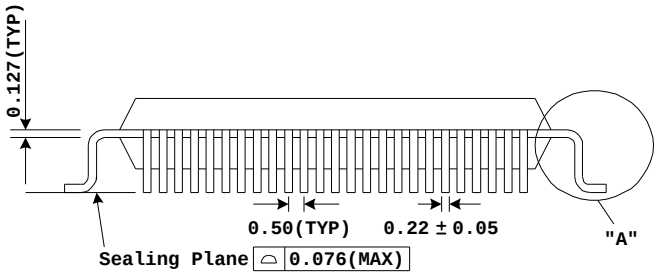


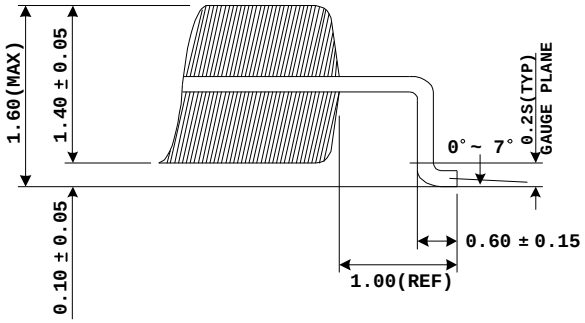




100 Pin LQFP







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