



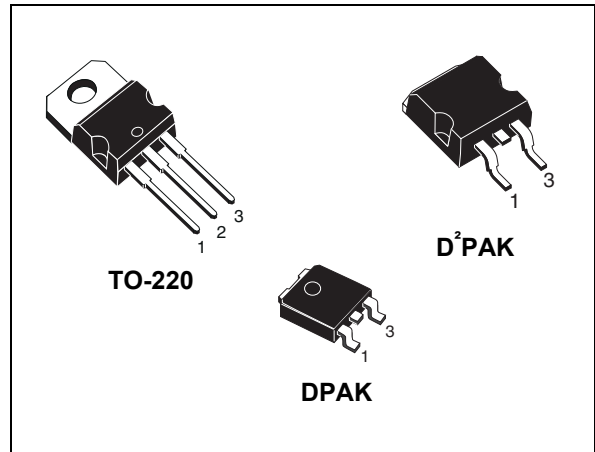
STGB10NC60K - STGD10NC60K STGP10NC60K

N-channel 600V - 10A - D²PAK / TO-220 / DPAK
Short circuit rated PowerMESH™ IGBT

General features

Type	V _{CES}	V _{CE(sat)} Max @25°C	I _C @100°C
STGB10NC60K	600V	<2.5V	10A
STGP10NC60K	600V	<2.5V	10A
STGD10NC60K	600V	<2.5V	10A

- Lower on voltage drop (V_{cesat})
- Lower C_{RES} / C_{IES} ratio (no cross-conduction susceptibility)
- Very soft ultra fast recovery antiparallel diode
- Short circuit withstand time 10μs



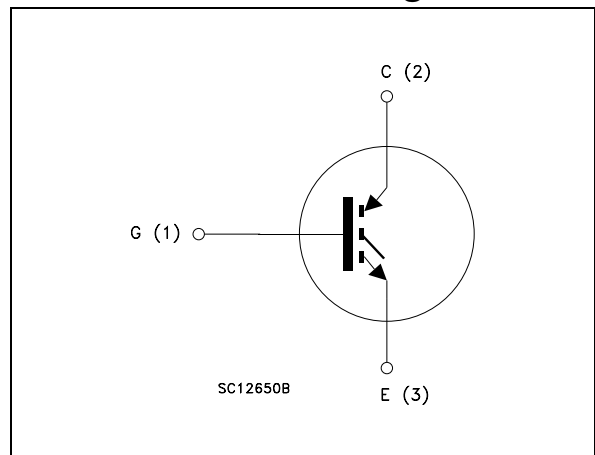
Description

Using the latest high voltage technology based on a patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, the PowerMESH™ IGBTs, with outstanding performances. The suffix "K" identifies a family optimized for high frequency motor control applications with short circuit withstand capability.

Applications

- High frequency motor controls
- SMPS and PFC in both hard switch and resonant topologies
- Motor drivers

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STGB10NC60KT4	GB10NC60K	D ² PAK	Tape & reel
STGP10NC60K	GP10NC60K	TO-220	Tube
STGD10NC60KT4	GD10NC60K	DPAK	Tape & reel

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage ($V_{GS} = 0$)	600	V
$I_C^{(1)}$	Collector current (continuous) at $T_C = 25^\circ\text{C}$	20	A
$I_C^{(1)}$	Collector current (continuous) at $T_C = 100^\circ\text{C}$	10	A
$I_{CM}^{(2)}$	Collector current (pulsed)	30	A
V_{GE}	Gate-emitter voltage	± 20	V
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	60	W
T_{stg}	Storage temperature	– 55 to 150	$^\circ\text{C}$
T_j	Operating junction temperature		
T_{scw}	Short circuit withstand time	10	μs
T_l	Maximum lead temperature for soldering purpose (for 10sec. 1.6 mm from case)	300	$^\circ\text{C}$

1. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{JMAX} - T_C}{R_{THJ-C} \times V_{CESAT(MAX)}(T_C, I_C)}$$

2. Pulse width limited by max junction temperature

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case Max	2.08	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient Max	62.5	$^\circ\text{C/W}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	$I_C = 1\text{mA}$, $V_{GE} = 0$	600			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE} = 15\text{V}$, $I_C = 5\text{A}$ $V_{GE} = 15\text{V}$, $I_C = 5\text{A}$, $T_C = 125^{\circ}\text{C}$		2.2 1.8	2.5	V V
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}$, $I_C = 250\text{ }\mu\text{A}$	4.5		6.5	V
I_{CES}	Collector cut-off current ($V_{GE} = 0$)	$V_{CE} = \text{Max Rating}$, $T_C = 25^{\circ}\text{C}$ $V_{CE} = \text{Max Rating}$, $T_C = 125^{\circ}\text{C}$			150 1	μA mA
I_{GES}	Gate-emitter leakage current ($V_{CE} = 0$)	$V_{GE} = \pm 20\text{V}$, $V_{CE} = 0$			± 100	nA
g_{fs}	Forward transconductance	$V_{CE} = 15\text{V}$, $I_C = 5\text{A}$		15		S

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies}	Input capacitance	$V_{CE} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GE} = 0$		380		pF
C_{oes}	Output capacitance			46		pF
C_{res}	Reverse transfer capacitance			8.5		pF
Q_g	Total gate charge	$V_{CE} = 390\text{V}$, $I_C = 5\text{A}$,		19		nC
Q_{ge}	Gate-emitter charge	$V_{GE} = 15\text{V}$,		5		nC
Q_{gc}	Gate-collector charge	(see Figure 16)		9		nC

Table 5. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 390V, I_C = 5A$		17		ns
t_r	Current rise time	$R_G = 10\Omega, V_{GE} = 15V, T_J = 25^\circ C$		6		ns
$(di/dt)_{on}$	Turn-on current slope	(see Figure 17)		655		A/ μs
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 390V, I_C = 5A$		16.5		ns
t_r	Current rise time	$R_G = 10\Omega, V_{GE} = 15V, T_J = 125^\circ C$		6.5		ns
$(di/dt)_{on}$	Turn-on current slope	(see Figure 17)		575		A/ μs
$t_r(V_{off})$	Off voltage rise time	$V_{CC} = 390V, I_C = 5A,$		33		ns
$t_{d(off)}$	Turn-off delay time	$R_{GE} = 10\Omega, V_{GE} = 15V, T_J = 25^\circ C$		72		ns
t_f	Current fall time	(see Figure 17)		82		ns
$t_r(V_{off})$	Off voltage rise time	$V_{CC} = 390V, I_C = 5A,$		60		ns
$t_{d(off)}$	Turn-off delay time	$R_{GE} = 10\Omega, V_{GE} = 15V, T_J = 125^\circ C$		106		ns
t_f	Current fall time	(see Figure 17)		136		ns

Table 6. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$E_{on}^{(1)}$	Turn-on switching losses	$V_{CC} = 390V, I_C = 5A$		55		μJ
$E_{off}^{(2)}$	Turn-off switching losses	$R_G = 10\Omega, V_{GE} = 15V, T_J = 25^\circ C$		85		μJ
E_{ts}	Total switching losses	(see Figure 17)		140		μJ
$E_{on}^{(1)}$	Turn-on switching losses	$V_{CC} = 390V, I_C = 5A$		87		μJ
$E_{off}^{(2)}$	Turn-off switching losses	$R_G = 10\Omega, V_{GE} = 15V,$		162		μJ
E_{ts}	Total switching losses	$T_J = 125^\circ C$ (see Figure 17)		249		μJ

1. E_{on} is the turn-on losses when a typical diode is used in the test circuit in figure 2. If the IGBT is offered in a package with a co-pak diode, the co-pak diode is used as external diode. IGBTs & Diode are at the same temperature (25°C and 125°C)
2. Turn-off losses include also the tail of the collector current

2.1 Electrical characteristics (curves)

Figure 1. Output characteristics

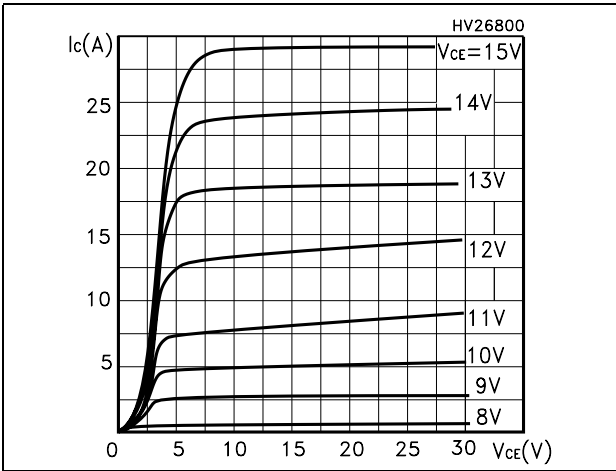


Figure 2. Transfer characteristics

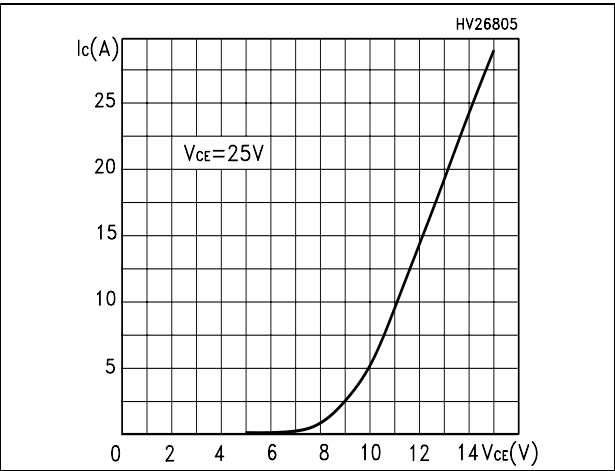


Figure 3. Transconductance

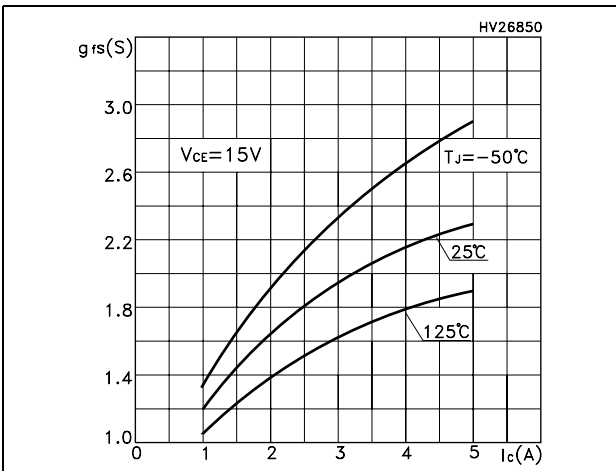


Figure 4. Collector-emitter on voltage vs temperature

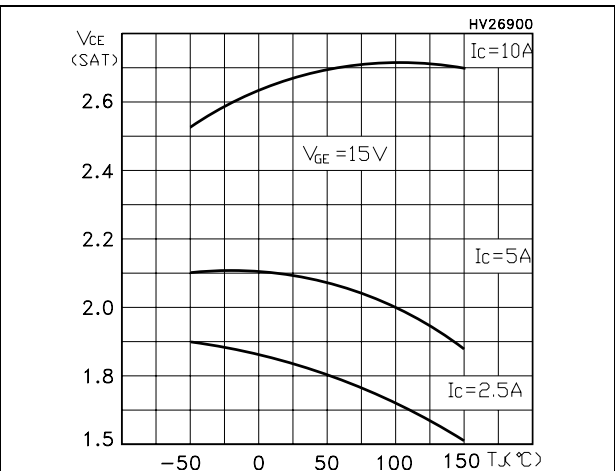


Figure 5. Gate charge vs gate-source voltage

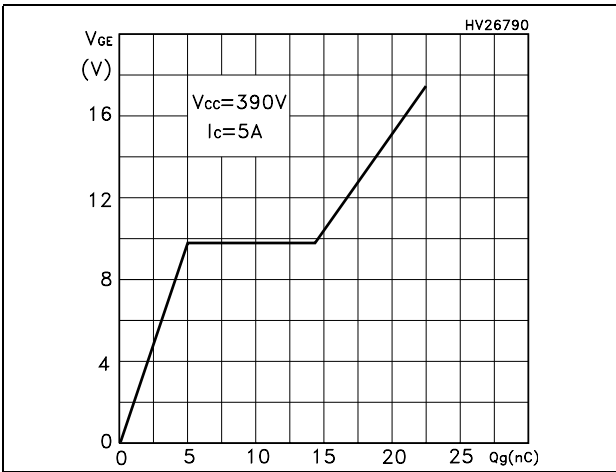


Figure 6. Capacitance variations

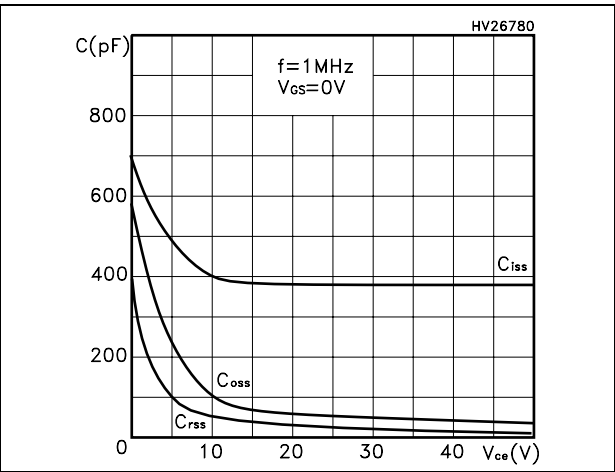


Figure 7. Normalized gate threshold voltage vs temperature

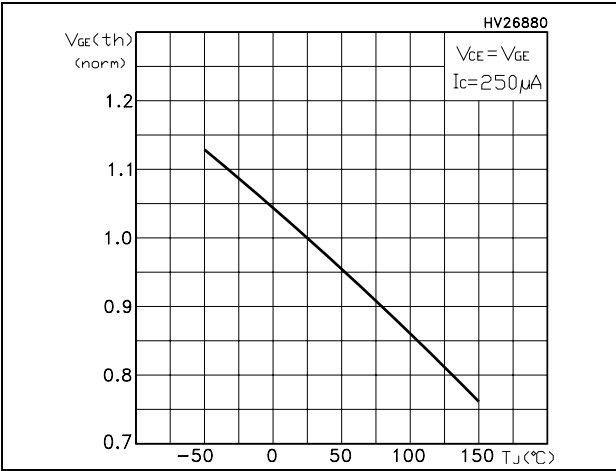


Figure 8. Collector-emitter on voltage vs collector current

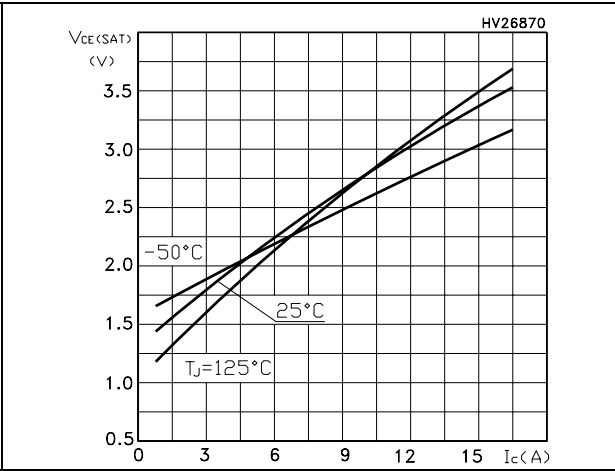


Figure 9. Normalized breakdown voltage vs temperature

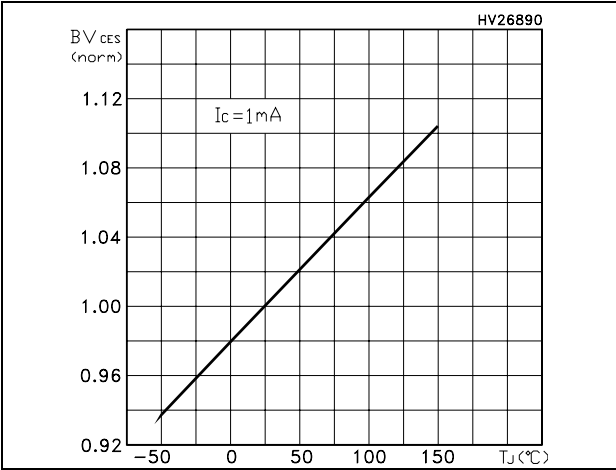


Figure 10. Switching losses vs temperature

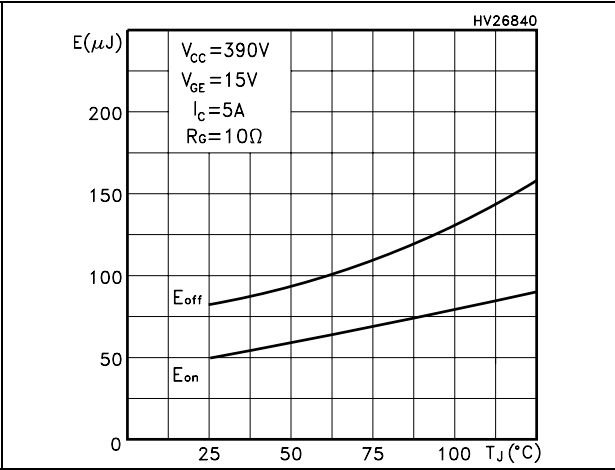


Figure 11. Switching losses vs gate resistance

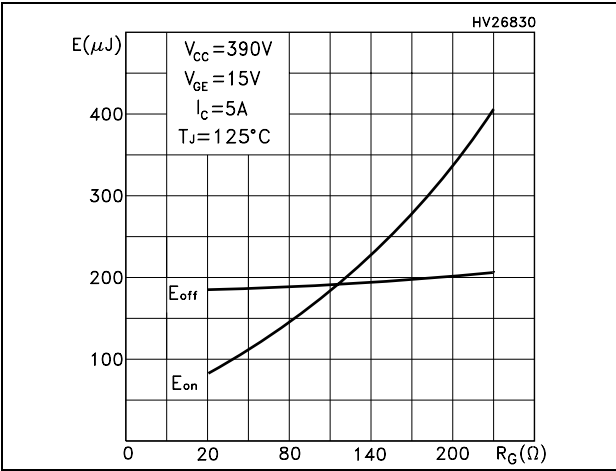


Figure 12. Switching losses vs collector current

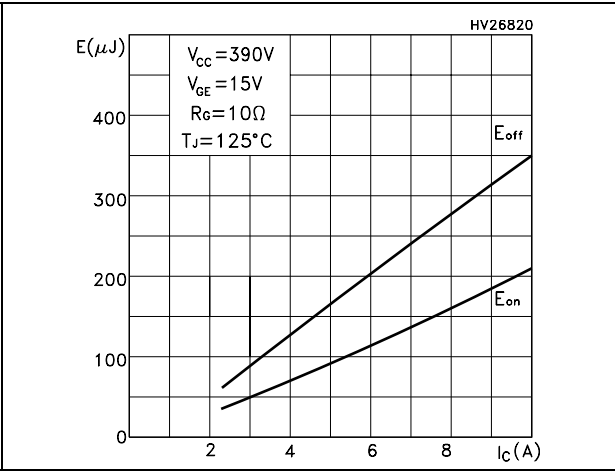


Figure 13. Thermal impedance

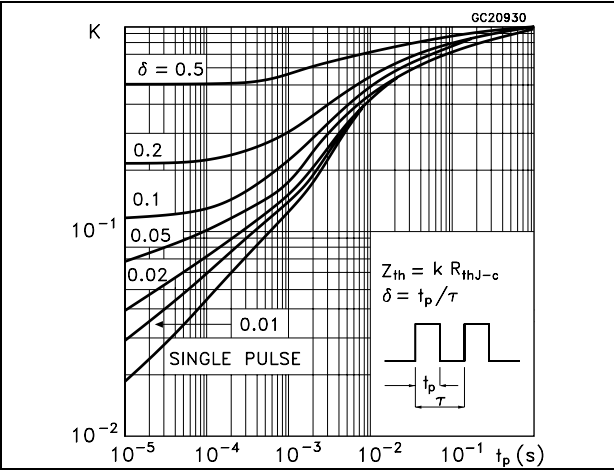
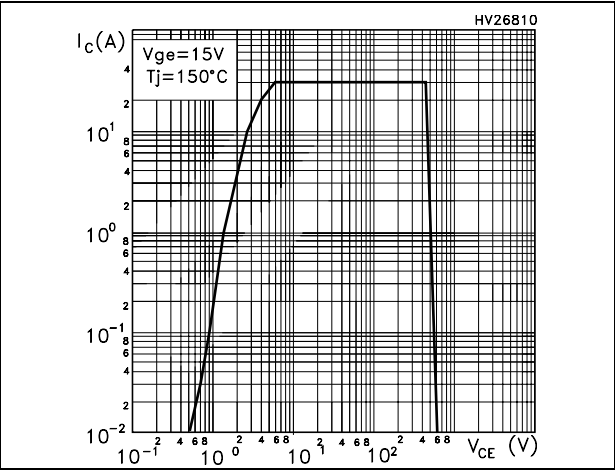


Figure 14. Turn-off SOA



3 Test circuit

Figure 15. Test circuit for inductive load switching

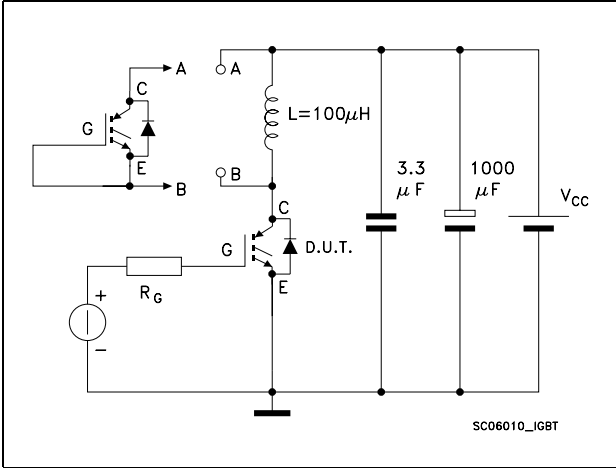


Figure 16. Gate charge test circuit

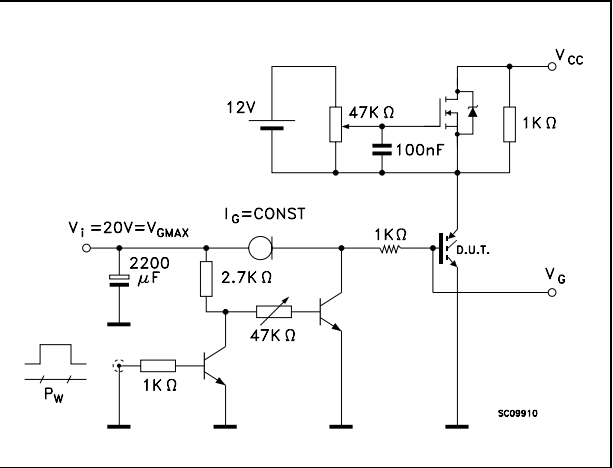


Figure 17. Switching waveform

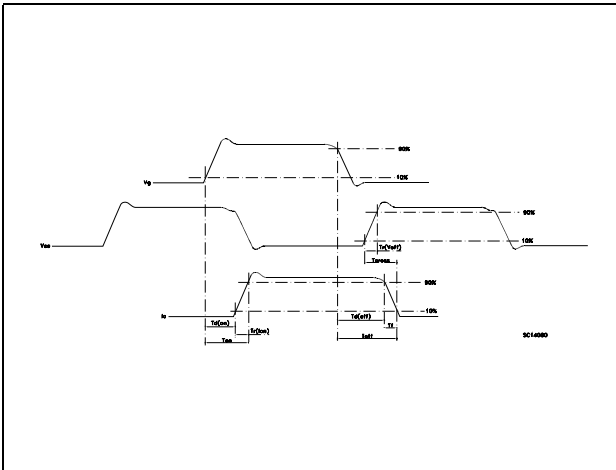
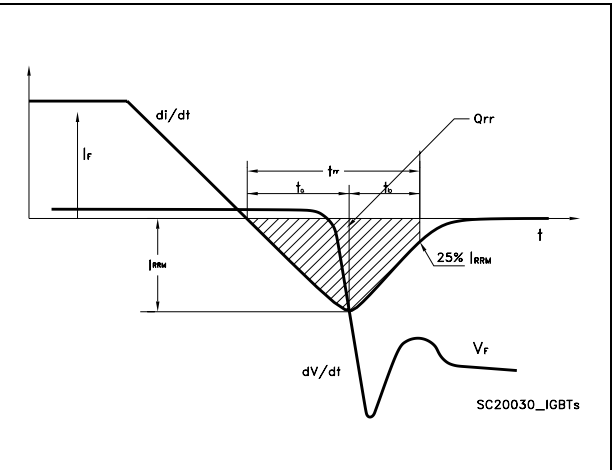


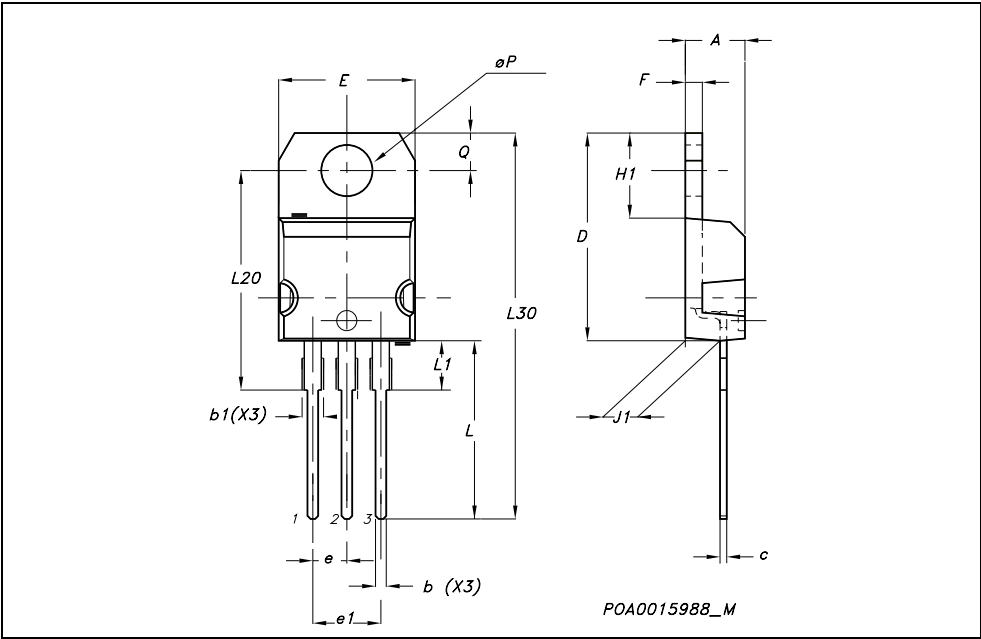
Figure 18. Diode recovery time waveform



4 Package mechanical data

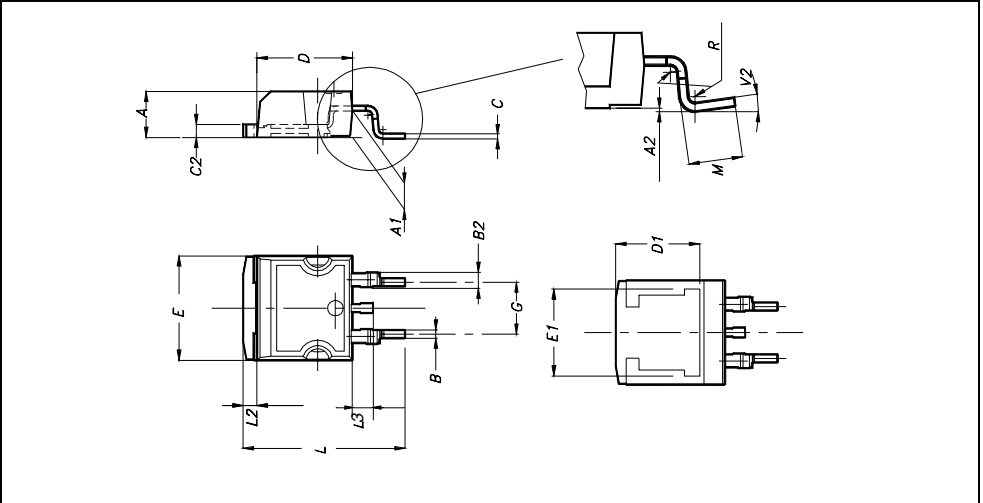
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-220 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



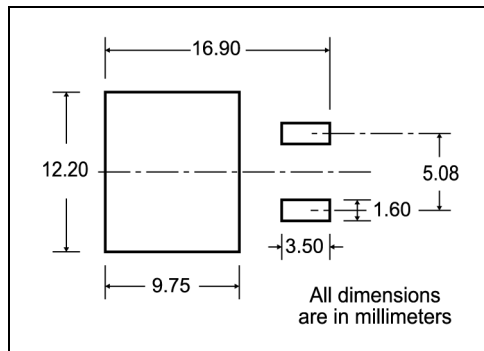
DPAK MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°

The mechanical drawing illustrates the DPAK package geometry. The top view shows dimensions E (total width), b4 (lead width), and e (pitch). The side view shows dimensions A (height), A1 (lead height), A2 (lead thickness), B (lead thickness), C (lead thickness), C2 (lead thickness), D (total height), D1 (lead height), E1 (lead height), and H (total height). The detail view shows dimensions L (lead length), L1 (lead length), L2 (lead length), L4 (lead length), and V2 (lead angle). The thermal pad is shown with dimensions E1 and D1. The seating plane and gauge plane are indicated.

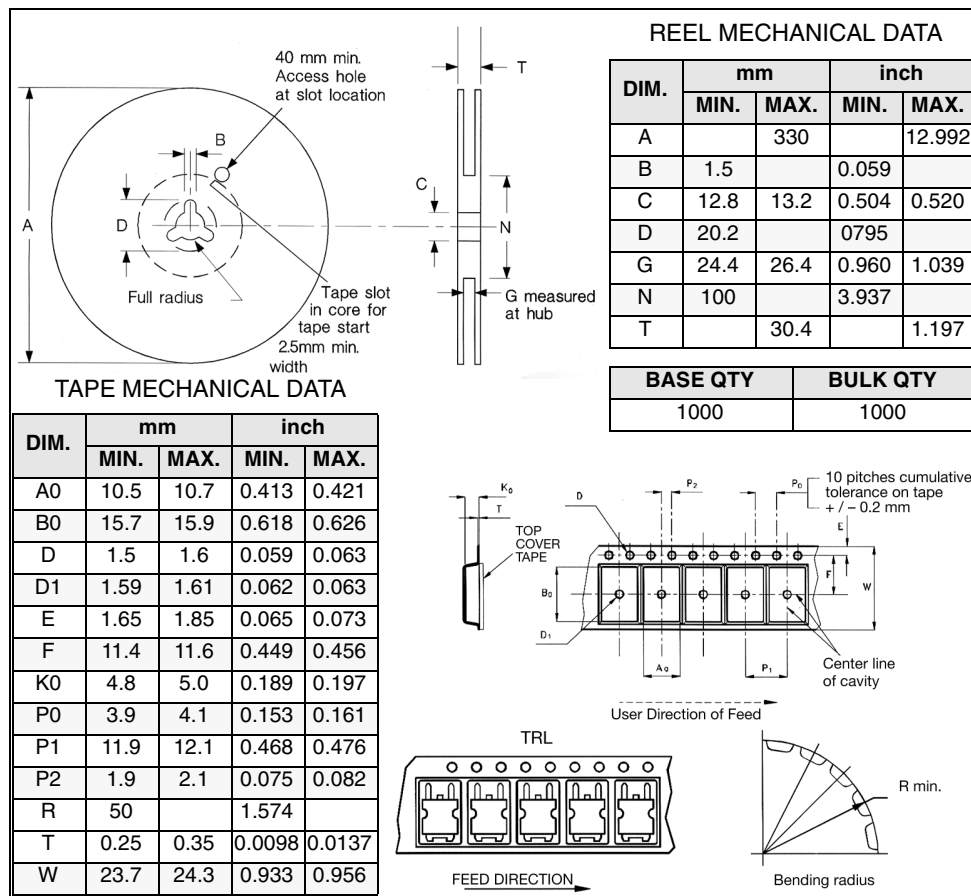
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5 Packaging mechanical data

D²PAK FOOTPRINT

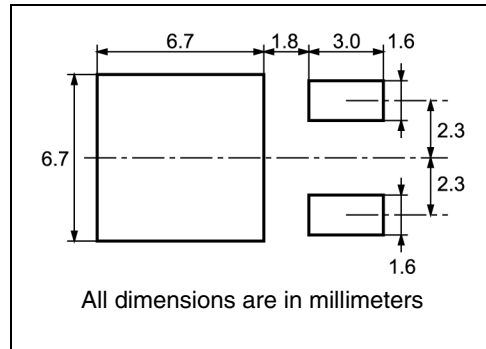


TAPE AND REEL SHIPMENT

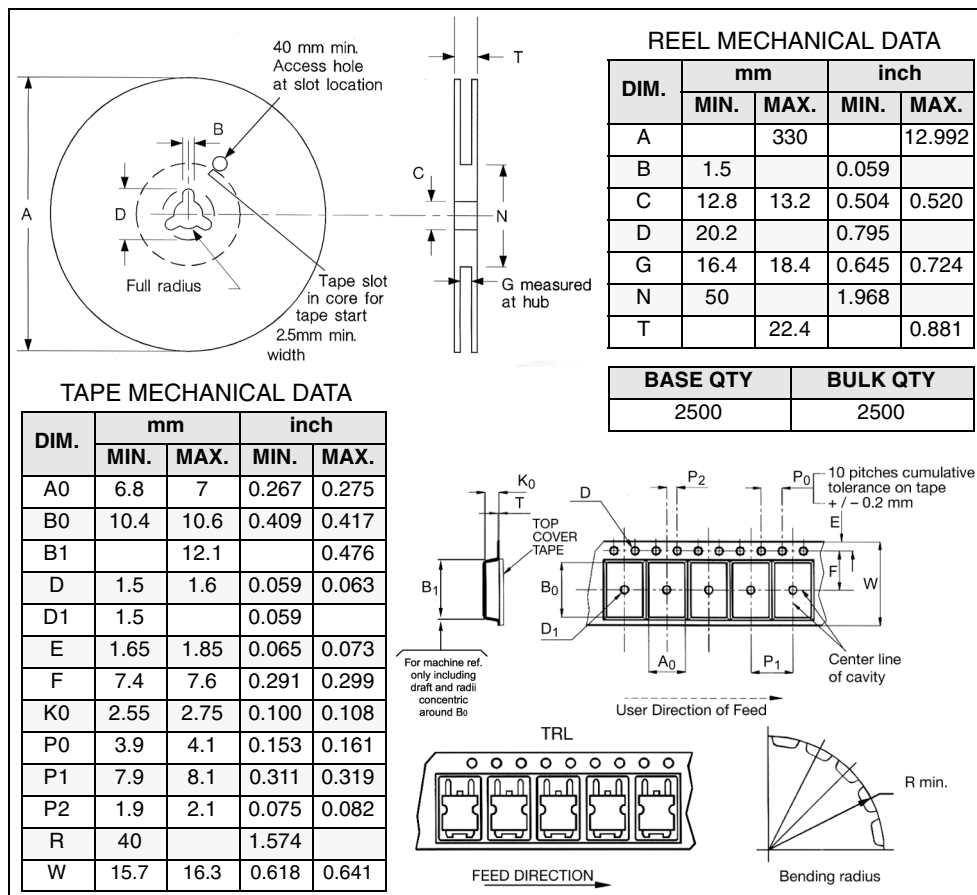


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DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



6 Revision history

Table 7. Revision history

Date	Revision	Changes
21-Nov-2005	1	New release
06-Dic-2005	2	Inserted row on Table 1.: Absolute maximum ratings
06-Mar-2006	3	The document has been reformatted
06-Jun-2006	4	Inserted DPAK
08-Feb-2007	5	Description has been updated

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