

N-Channel 200-V (D-S) 150°C MOSFET

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- · Level 3 MOS

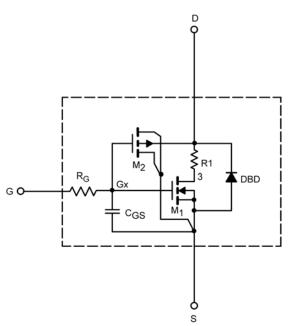
- Apply for both Linear and Switching Application
- Accurate over the –55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125° C temperature ranges under the pulsed 0-V to 15-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

SUBCIRCUIT MODEL SCHEMATIC

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

SPICE Device Model SUP36N20-54P **Vishay Siliconix**



Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static			-		
Gate Threshold Voltage	V _{GS(th)}	V_{DS} = V_{GS} , I_D = 250 μ A	3.1		V
On-State Drain Current ^a	I _{D(on)}	$V_{\text{DS}}~\geq$ 10 V, V_{GS} = 10 V	211		А
Drain-Source On-State Resistance ^a	۲ _{DS(on)}	V_{GS} = 10 V, I_D = 20 A	0.047	0.044	Ω
		V_{GS} = 15 V, I_D = 20 A	0.046	0.0435	
		V_{GS} = 10 V, I_{D} = 20 A, T_{J} = 100°C	0.072		
		V_{GS} = 10 V, I_{D} = 20 A, T_{J} = 150°C	0.090		
Forward Voltage ^a	V _{SD}	I_F = 40 A, V_{GS} = 0 V	0.90	0.86	V
Forward Transconductance ^a	g _{fs}	V_{DS} = 15 V, I _D = 20 A			S
Dynamic ^b					
Input Capacitance	C _{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	3309	3100	pF
Output Capacitance	C _{oss}		323	300	
Reverse Transfer Capacitance	C _{rss}		148	135	
Total Gate Charge ^c	Qg	$V_{\rm DS}$ = 100 V, $V_{\rm GS}$ = 15 V, $I_{\rm D}$ = 50 A	79	85	nC
		V _{DS} = 100 V, V _{GS} = 10 V, I _D = 50 A	57	57	
Gate-Source Charge ^c	Q _{gs}		14	14	
Gate-Drain Charge ^c	Q_gd		20	20	

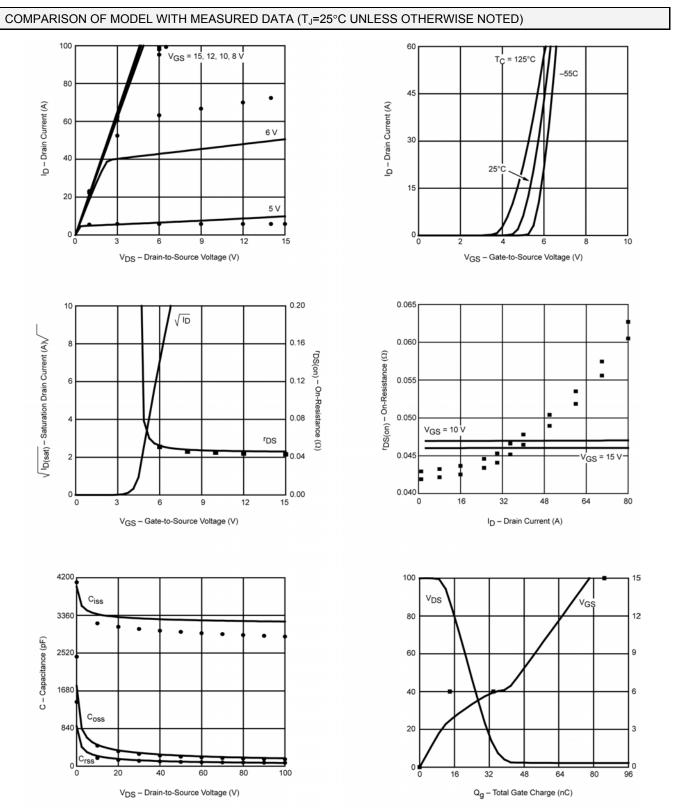
Notes

a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2%. b. Guaranteed by design, not subject to production testing. c. Independent of operating temperature.



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Note: Dots and squares represent measured data.



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