

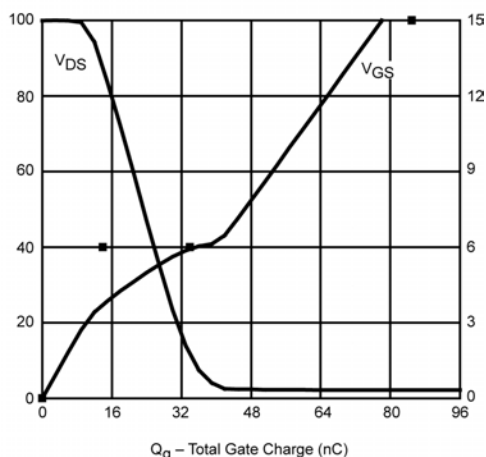
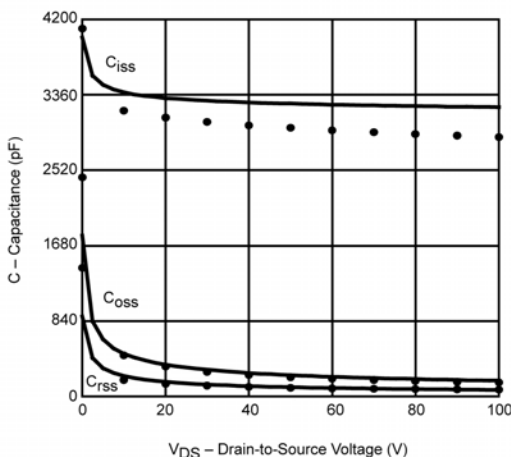
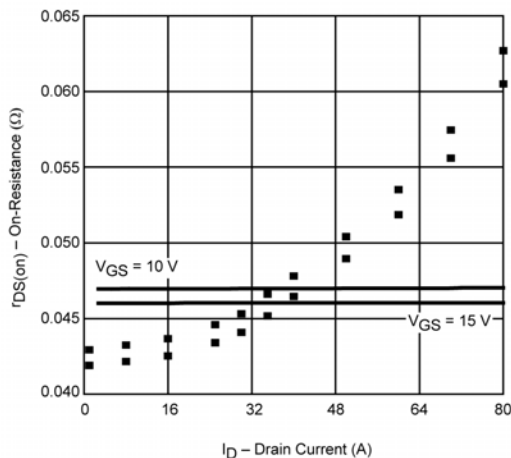
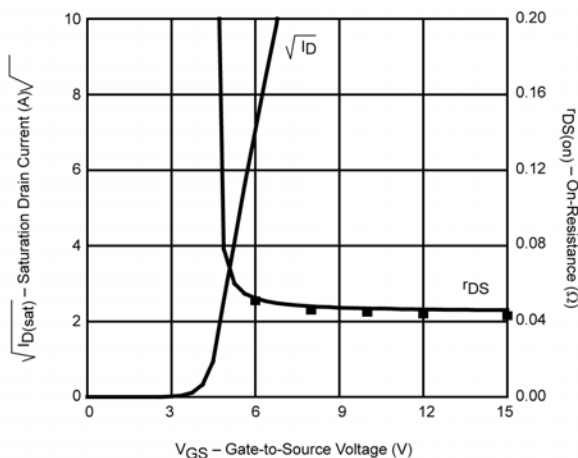
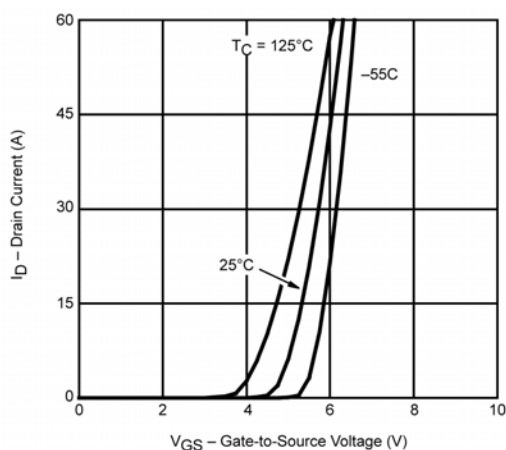
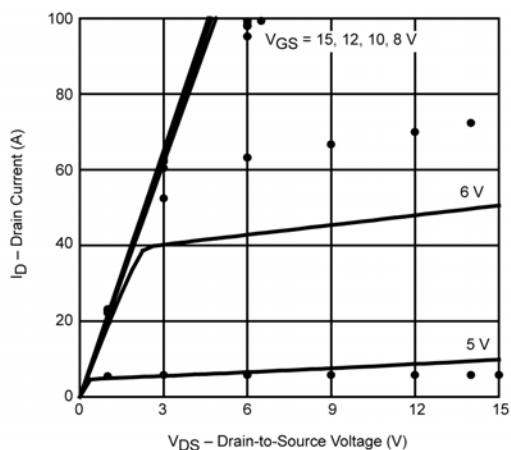
SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static					
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	3.1		V
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 10 V, V _{GS} = 10 V	211		A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 20 A	0.047	0.044	Ω
		V _{GS} = 15 V, I _D = 20 A	0.046	0.0435	
		V _{GS} = 10 V, I _D = 20 A, T _J = 100°C	0.072		
		V _{GS} = 10 V, I _D = 20 A, T _J = 150°C	0.090		
Forward Voltage ^a	V _{SD}	I _F = 40 A, V _{GS} = 0 V	0.90	0.86	V
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 20 A			S
Dynamic^b					
Input Capacitance	C _{iss}	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	3309	3100	pF
Output Capacitance	C _{oss}		323	300	
Reverse Transfer Capacitance	C _{rss}		148	135	
Total Gate Charge ^c	Q _g	V _{DS} = 100 V, V _{GS} = 15 V, I _D = 50 A	79	85	nC
		V _{DS} = 100 V, V _{GS} = 10 V, I _D = 50 A	57	57	
Gate-Source Charge ^c	Q _{gs}		14	14	
Gate-Drain Charge ^c	Q _{gd}		20	20	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



Disclaimer

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