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GL620USB

GeneLink-Lite
USB PC-to-PC File Transfer Controller

SPECIFICATION 1.6

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Index

1. Features

- Conforms to USB 12Mbps Specification, Version 1.1
- Patented architecture
- Single chip solution for host-to-host communication
- File transfer application software running on Windows 98 and Windows 2000
- Up to 8.6Mbps transfer rate
- Suitable for mobile and SOHO environment
- Tiniest solution in the market – 16-pin SOP
- On-chip 3.3V output
- 12MHz external clock
- Internal power-on reset
- Power management support

2. Functional Overview

The GL620USB provides a single-chip solution for connecting two or more PCs via their USB ports. According to USB protocol, the PC is the host and the device is a slave, where the host initiates all the USB traffic and the slave responds to the host's requests. In other words, a host cannot talk to another host via USB protocol; instead, a host can only talk to one or more devices. The GL620USB's patent-pending architecture overcomes the USB inherently incompatibility of connecting two or more PCs by providing two independent USB transceivers and SIEs for each host, i.e., data can be transferred in both directions simultaneously.

System Diagram

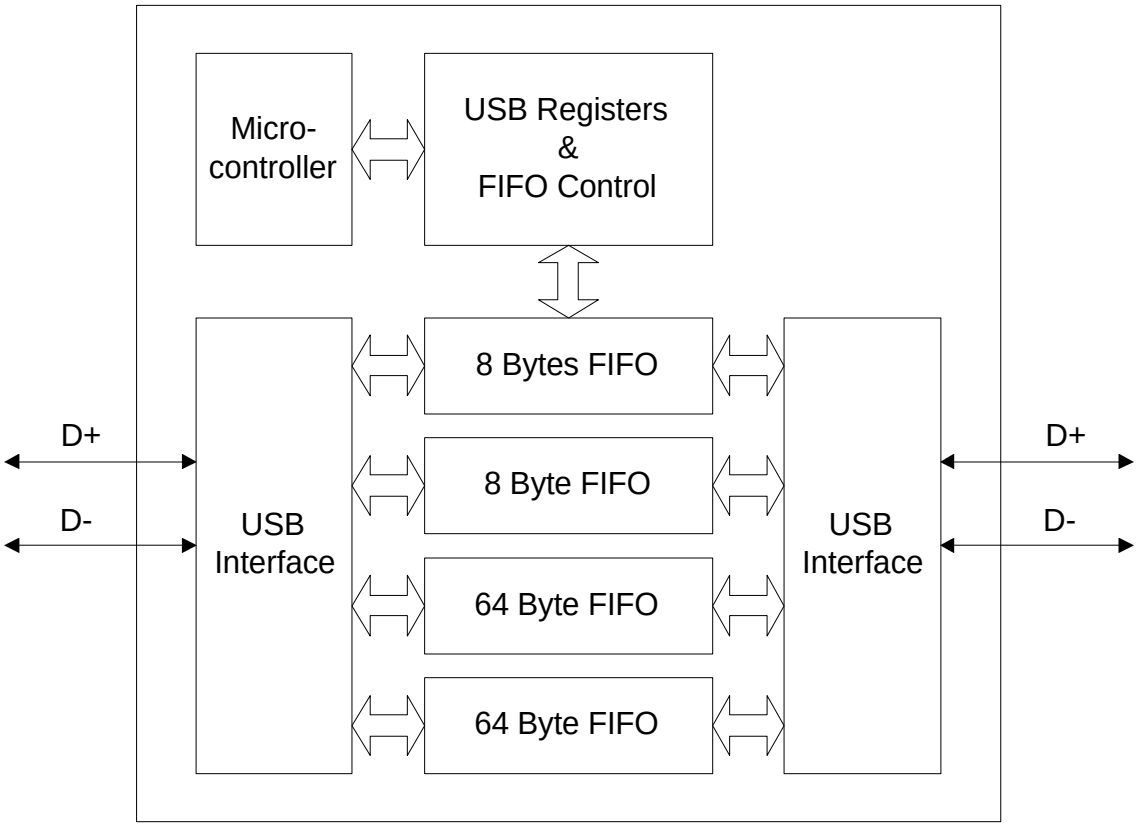
3. Applications

We provide application program to share file between 2 PCs. This application is easy to install for end users. Besides, the file transfer rate of the application program (combined with GL620USB) is up to 8.6Mbps. With this file transfer application, PCs can share files on all local drives, such as hard drive, floppy, CD-ROM and network drives.

The GL620USB-Lite file transfer function can be integrated with the following form factors:

- USB standalone cable
- USB standalone hub
- USB monitor with hub
- PC host

4. Functional Description



Block diagram of GL620USB-Lite

The GL620USB-Lite is equipped with two full-speed USB ports, and each port has four endpoints to provide different functions as follows:

- Endpoint 0: control transfer
- Endpoint 1: bulk-read transfer
- Endpoint 2: bulk-write transfer
- Endpoint 3: interrupt transfer

Two 8-bytes FIFO and four 64-bytes FIFO are built in the device as follows:

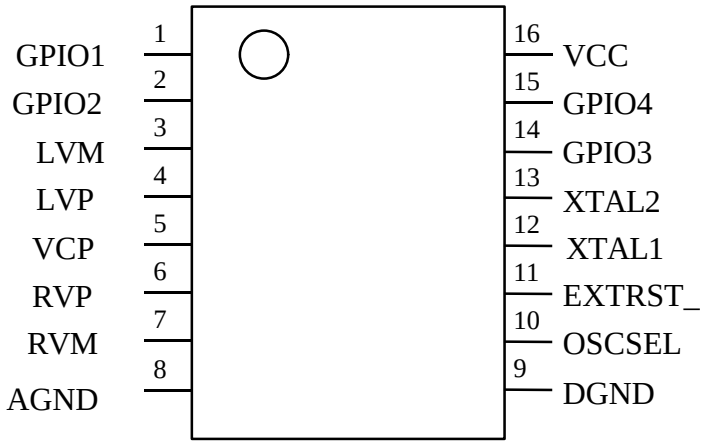
- Left 8-byte FIFO: provide a pipe to link left endpoint 0 and right endpoint 3. For example, if left host wants to communicate with right host, left host can issue a no data control transfer and the setup command will be stored

in the left 8-byte FIFO. Right host can request an interrupt transfer to get the setup command from left host. The status stage of the left side control transfer will not be terminated until that the right side get the setup command via interrupt transfer.

- Right 8-byte FIFO: provide a pipe to link right endpoint 0 and left endpoint 3.
- Left 64-bytes DATA0/DATA1 FIFOs: provide a pipe to link left endpoint 2 and right endpoint 1. For example, if left host wants to transfer data to right host, left host can issue bulk write transfer and the payload will be stored in the left 64-byte FIFOs. Right host can request a bulk read transfer to get the data from left host.
- Right 64-bytes DATA0/DATA1 FIFOs: provide a pipe to link right endpoint 2 and left endpoint 1.

5. Pin Definitions and Descriptions

PIN	SYMBOL	I/O	DESCRIPTION
1	GPIO1	B	General purpose IO pin / Driving LED capability
2	GPIO2	B	General purpose IO pin / Driving LED capability
3	LVM	B	Left D-
4	LVP	B	Left D+
5	VCP	O	3.3V output
6	RVP	B	Right D+
7	RVM	B	Right D-
8	AGND	-	Ground
9	DGND	-	Ground
10	OSCSEL	I	Selection of clock type
11	EXTRST_	I	External reset
12	XTAL1	I	12M crystal input
13	XTAL2	O	Crystal output
14	GPIO3	B	General purpose IO pin
15	GPIO4	B	General purpose IO pin
16	VCC	-	5V power



16-pin SOP

6. Electrical Characteristics

6.1 Absolute Maximum Ratings (Voltages referenced to GND)

SYMBOL	Description	MIN	MAX
VCC	DC supply voltage	-0.5V	+7V
V_I	DC input voltage	-0.5V	VCC+0.5V
$V_{I/O}$	DC input voltage range for bidirect pins	-0.5V	VCC+0.5V
$V_{AI/O}$	DC input voltage for USB D+/D- pins(PIN3, 4, 6, 7)	-0.5V	VCC+0.5V
$V_{I/OZ}$	DC voltage applied to outputs in High Z state	-0.5V	VCC+0.5V
V_{ESD}	static discharge voltage	4000V	

6.2 DC Characteristics (VCP/D+/D-)

SYMBOL	Description	MIN	TYP	MAX	UNIT
$V_{3.3}$	VCP regulator output	3.0	3.3	3.6	V
$I_{3.3}$	VCP maximum supply current	27	41	56	mA
V_{OL}	D+/D- static output LOW(R_L of 1.5K to 3.6V)			0.3	V
V_{OH}	D+/D- static output HIGH (R_L of 15K to GND)	2.8		3.6	V
V_{DI}	Differential input sensitivity	0.2			V
V_{CM}	Differential common mode range	0.8		2.5	V
V_{SE}	Single-ended receiver threshold	0.2			V
C_{IN}	Transceiver capacitance			20	pF
I_{LO}	Hi-Z state data line leakage	-10		+10	µA
Z_{DRV}	Driver output resistance	28		43	Ohms

6.3 DC Characteristics (PIN1, 2)

SYMBOL	Description	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
I_{OL}	DC output sink current at 0.4V	13.01	19.54	24.82	mA
I_{OH}	DC output source current at V_{DD} -0.4V	6.35	9.82	12.37	mA
I_{OHTTL}	DC output source current at TTL high	24.62	49.45	69.12	mA
V_{IL}	LOW level input voltage			0.7	V
V_{IH}	HIGH level input voltage	2.66			V
V_{TLH}	LOW to HIGH threshold voltage	2.02	2.38	2.66	V
V_{THL}	HIGH to LOW threshold voltage	0.7	0.83	1.0	V
V_{HYS}	Hysteresis voltage	1.1	1.55	1.79	V
V_{OL}	LOW level output voltage when I_{OL}=16mA			0.4	V

6.4 DC Characteristics (PIN10, 11)

SYMBOL	Description	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IL}	LOW level input voltage			0.69	V
V_{IH}	HIGH level input voltage	2.65			V
V_{TLH}	LOW to HIGH threshold voltage	2.01	2.37	2.65	V
V_{THL}	HIGH to LOW threshold voltage	0.69	0.82	0.99	V
V_{HYS}	Hysteresis voltage	1.1	1.55	1.79	V
R_{UP}	Pad internal pullup resister	191.27	240.69	376.34	Kohms

6.5 DC Characteristics (PIN14, 15)

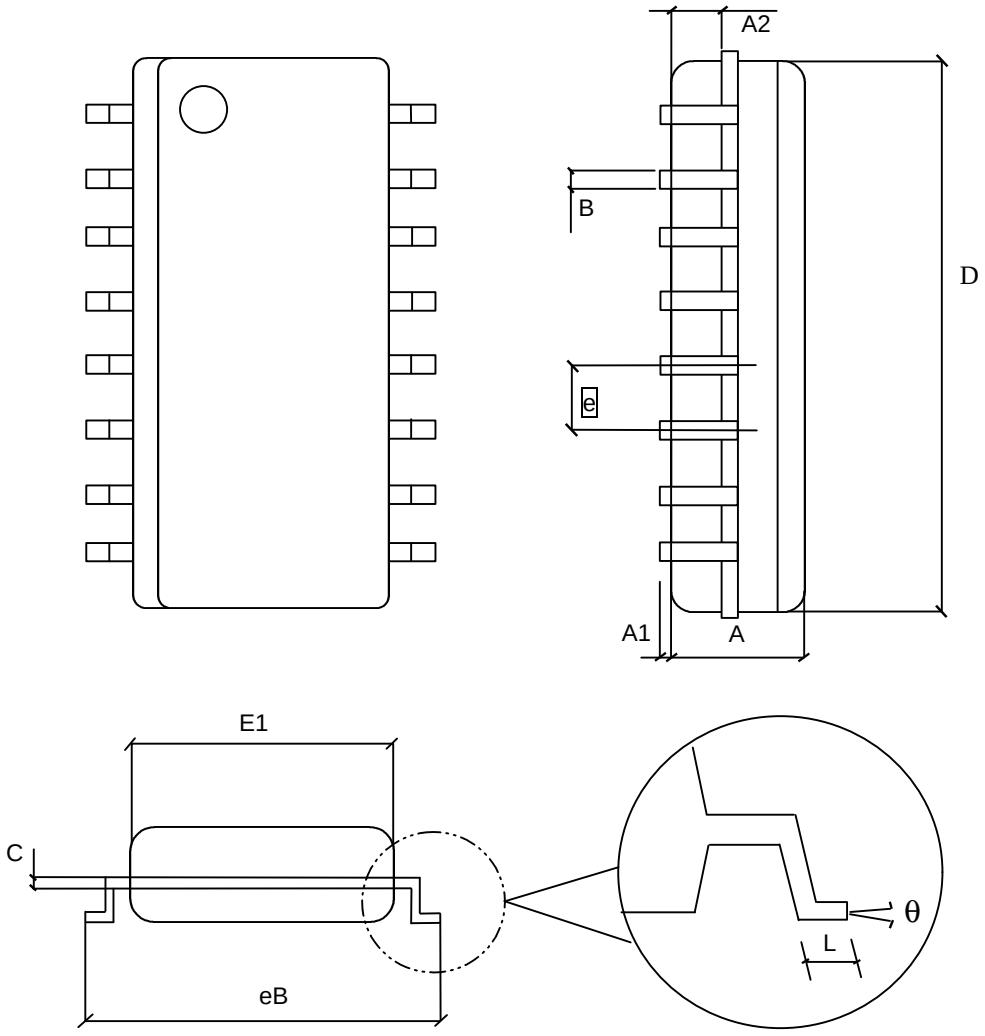
SYMBOL	Description	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
I_{OL}	DC output sink current at 0.4V	3.89	5.94	7.56	mA
I_{OH}	DC output source current at V_{DD} -0.4V	2.85	4.36	5.46	mA
I_{OHTTL}	DC output source current at TTL high	10.9	21.5	29.75	mA
V_{IL}	LOW level input voltage			0.71	V
V_{IH}	HIGH level input voltage	2.68			V
V_{TLH}	LOW to HIGH threshold voltage	2.03	2.39	2.68	V
V_{THL}	HIGH to LOW threshold voltage	0.71	0.83	1.0	V
V_{HYS}	Hysteresis voltage	1.1	1.55	1.8	V
V_{OL}	LOW level output voltage when I_{OL}=4mA			0.4	V
R_{DN}	Pad internal pulldown resister	122.08	160	267.31	Kohms

6.6 Switching Characteristics

SYMBOL	Description	MIN	TYP	MAX	UNIT
F_{X1}	X1 crystal frequency	11.97	12	12.03	MHz
T_{CYC}	X1 cycle time		83.3		ns
T_{X1L}	X1 clock LOW time	$0.45T_{cyc}$			ns
T_{X1H}	X1 clock HIGH time	$0.45T_{cyc}$			ns
T_{r30pf}	Output pad rise time from 10% to 90% swing with 30pF loading	6	8	12	ns
T_{f30pf}	Output pad fall time from 10% to 90% swing with 30pF loading	5.3	7	10.4	ns
T_{r50pf}	Output pad rise time from 10% to 90% swing with50pF loading	9.5	13	19	ns
T_{f50pf}	Output pad fall time from 10% to 90% swing with 50pF loading	7.7	10	16	ns
T_{rUSB}	D+/D- rise time with 50pF loading	4		20	ns
T_{fUSB}	D+/D- fall time with 50pF loading	4		20	ns

7. Package Diagram

Symbol	Dimension in mils			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	---	58	---	---	1.473	---
A1	6	---	---	0.152	---	---
A2	---	24	---	---	0.610	---
B	---	16	---	---	0.406	---
C	---	8	---	---	0.203	---
D	388	390	392	9.855	9.906	9.957
E1	152	154	156	3.861	3.912	3.962
e	---	50	---	---	1.270	---
eB	---	238	---	---	6.045	---
L	25	---	---	0.635	---	---
θ	0°	3°	6°	0°	3°	6°



8. Application Circuit