Genesys Logic, Inc.

GL827

USB 2.0 Single Slot SD/MMC/MS/SM/xD-Picture Card Reader Controller

Datasheet

Revision 1.09

Sep. 06, 2007

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Revision History

Revision	Date	Description
1.00	2006/04/11	First formal release
1.01	2006/05/05	Add Reset Timing
1.03	2006/06/06	1. Add Clock source selection 2. Add Reset pull up with DVDD 3. Modify DVDD(Pin15) on 48Pin package 4. Check PMOS output current
1.04	2006/06/06	Add Micro SD / MMC Micro / MS PRO Micro support
1.05	2006/08/28	1. Add 5V to 3.3 V regulator characteristic 2. Remove all the description of over-current protection 3. Delete AVDD1~4 (Pin15) on 100Pin package
1.06	2006/10/12	1. Add 48Pin LQFN package 2. Add QFN24 package and CSP23 package 3. Modify pin name for simplification and pin type 4. Support MMCv4.2
1.07	2007/03/23	1. Add Vista submission number 1218426, p8. 2. Modify xD 1.2B to 1.2C, p8. 3. Supports Slew Rate Control (SRC) to reduce EMI effect
1.08	2007/08/30	1. Add SSOP28, p7,8,14,18,19,45,46
1.09	2007/09/06	1. Update reset timing in section 6.6.8, p.38

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CHAPTER 1 GENERAL DESCRIPTION

The GL827 is USB 2.0 Single Interface Flash Card Reader controller. It supports USB 2.0 high-speed transmission to Secure Digital™ (SD), SDHC, Mini SD™, Micro SD™ , T-Flash , MultiMediaCard™ (MMC), RS MultiMediaCard™ (RS MMC), MMC Micro , HS-MMC, MMC-Mobile , Memory Stick™ (MS), Memory Stick Duo™ (MS Duo), High Speed Memory Stick™ (HS MS), Memory Stick PRO™ (MS PRO), Memory Stick PRO™ Duo (MS PRO Duo), Memory Stick ROM, MS PRO Micro, SmartMedia™ (SM) , and xD-Picture Card ™ (xD) on one chip. As a single chip solution for USB 2.0 flash card reader, the GL827 complies with Universal Serial Bus specification rev. 2.0, USB Storage Class specification ver.1.0, and flash card interface specification each.

The GL827 can support different kinds of interfaces in single slot. For the best performance consideration, the GL827 integrates high efficiency card interface hardware engine for data transfer. The GL827 also supports firmware upgrade via USB interface (100 Pin LQFP), and external flash read/ write for firmware upgrade and other applications.

The GL827 pin assignment design fits to card sockets to provide easier PCB layout. 100 Pin LQFP (14mmx14mm), 48 Pin LQFP/LQFN (7mm x 7mm), QFN24 (4mm x 4mm), SSOP28 (150mil) are available package types.

CHAPTER 2 FEATURES

- USB specification compliance
  - Comply with 480Mbps Universal Serial Bus specification rev. 2.0.
  - Comply with USB Storage Class specification rev. 1.0.
  - Support 1 device address and up to 4 endpoints: Control (0)/ Bulk Read (1)/ Bulk Write (2)/Interrupt (3).
- Integrated USB building blocks
  - USB2.0 transceiver macro (UTM), Serial Interface Engine (SIE), Build-in power-on reset (POR) and low-voltage detector (LVD)
- Embedded 8051 micro-controller
  - Operate @ 60 MHz clock, 12 clocks per instruction cycle
  - Embedded 48K Byte mask ROM and internal 256 byte SRAM
  - Embedded 4K Byte external SRAM
  - Support up to external 48K code ROM
- Supports firmware upgrade to external flash via USB (ISP : In System Programming) (Only for LQFP100)
- USB 2.0 certified (USB-IF Pass, TID: 40000207/ 40550012)
- WHQL submission number 1062005.
- Vista submission number 1218426.
- xD-Picture (Only for LQFP100/ LQFP48/ LQFN48)
  - xD-Picture specification v1.2C. Type-M / Type-H
- SmartMedia™ (Only for LQFP100/ LQFP48/ LQFN48)
  - 8 bit data width and different speed
  - Support different page size, and automatic append redundant area data (8 / 16 bytes)
- Memory Stick™ / Memory Stick PRO / Memory Stick PRO Duo / Memory Stick Micro (For all packages)
  - Comply with Memory Stick specification
  - Support INS signal
  - Support automatic CRC16 generation and verification
- Secure Digital™ and MultiMediaCard™ (For all packages)
  - Supports SD specification v1.0 / v1.1 / v2.0
  - Supports MMC specification v3.X / v4.0 / v4.1 / v4.2.
  - x1 / x4 / x8 data transmission. (For QFN24 and CSP23 up to x4)
  - Automatic CRC7 generation for command and CRC7 verification for response on CMD
  - Support automatic CRC16 generation and verification on DAT0:7
  - In addition to full packet transaction, optional single byte / bit operation on both CMD and DAT line / lines
  - Process data in block or byte
- On board 12 MHz Crystal driver circuit or 12/48 MHz Clock input.
- On-Chip 5V to 3.3V regulator. No external regulator required.
- On-Chip power MOSFETs for supplying flash media card power.
- Available in 100 Pin LQFP (14x14 mm) package
- Available in 48 Pin LQFP/LQFN (7x7 mm) package
- Available in 24 Pin QFN (4x4 mm) package
- Available in 28 Pin SSOP (150mil) package
- Order in Advance in 23 Pin CSP (2x2 mm) package

CHAPTER 3 PIN ASSIGNMENT

3.1 Pinout

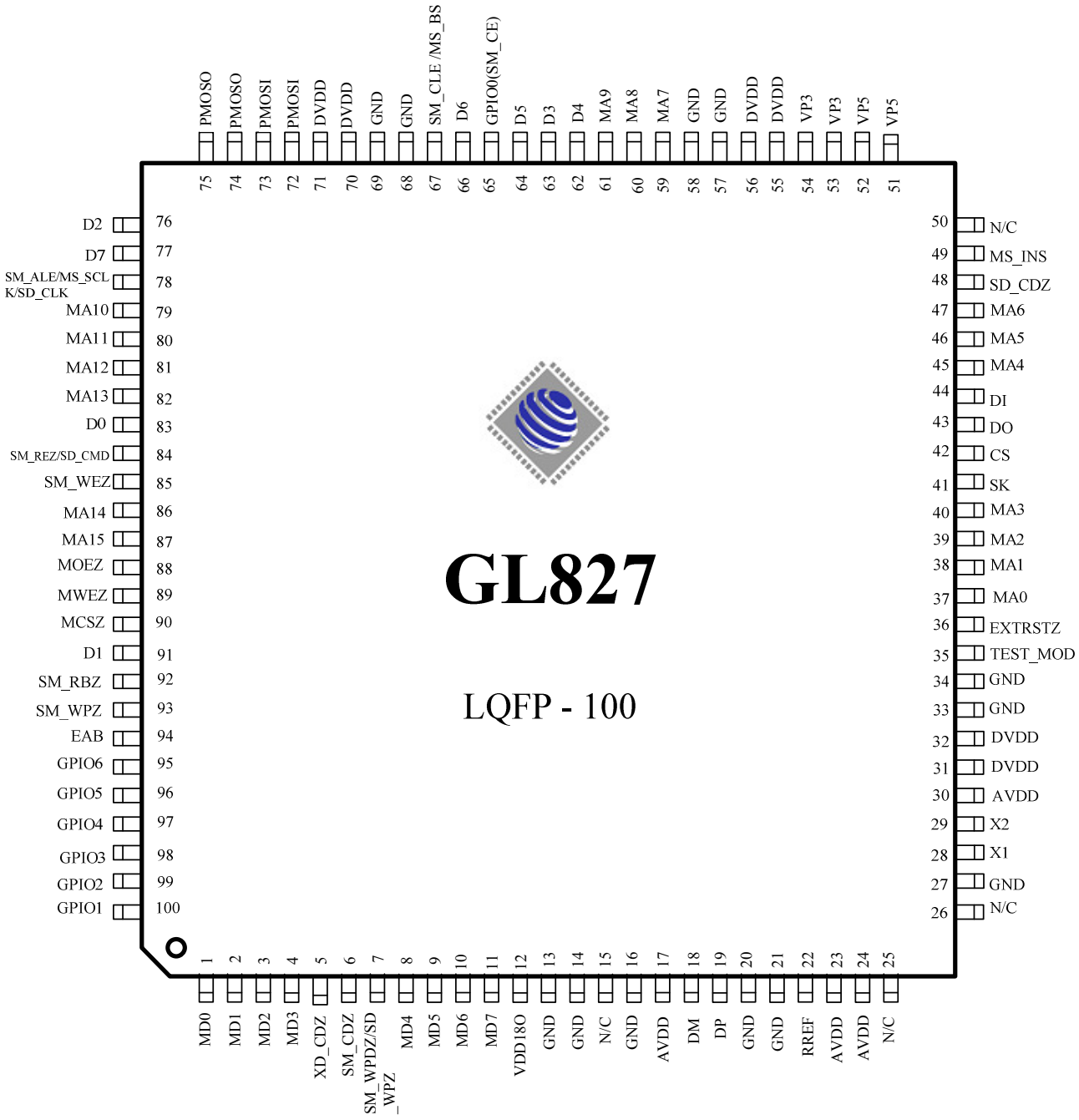


Figure 3.1 – 100 Pin LQFP Pinout Diagram

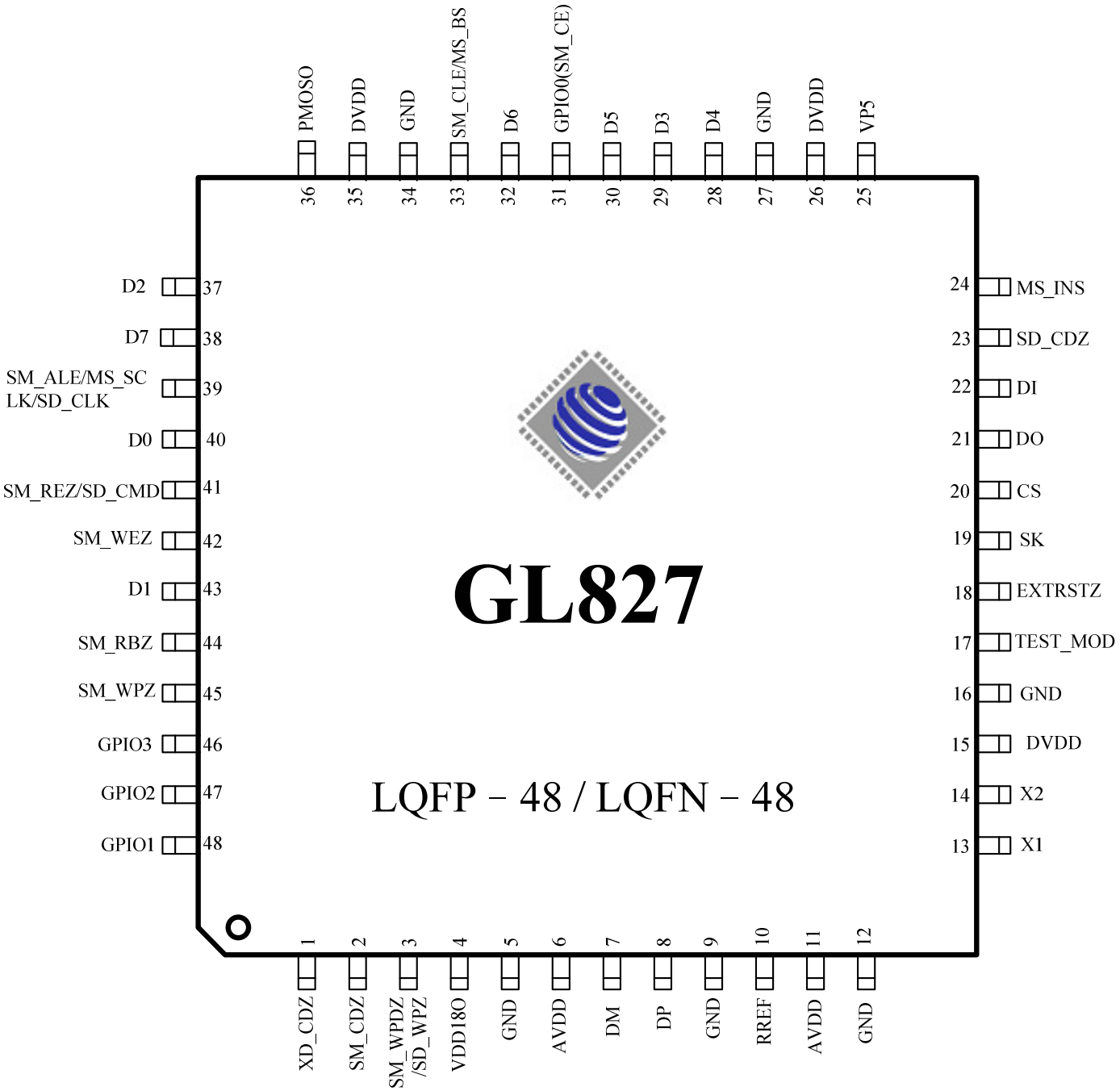


Figure 3.2 – 48 Pin LQFP/LQFN Pinout Diagram

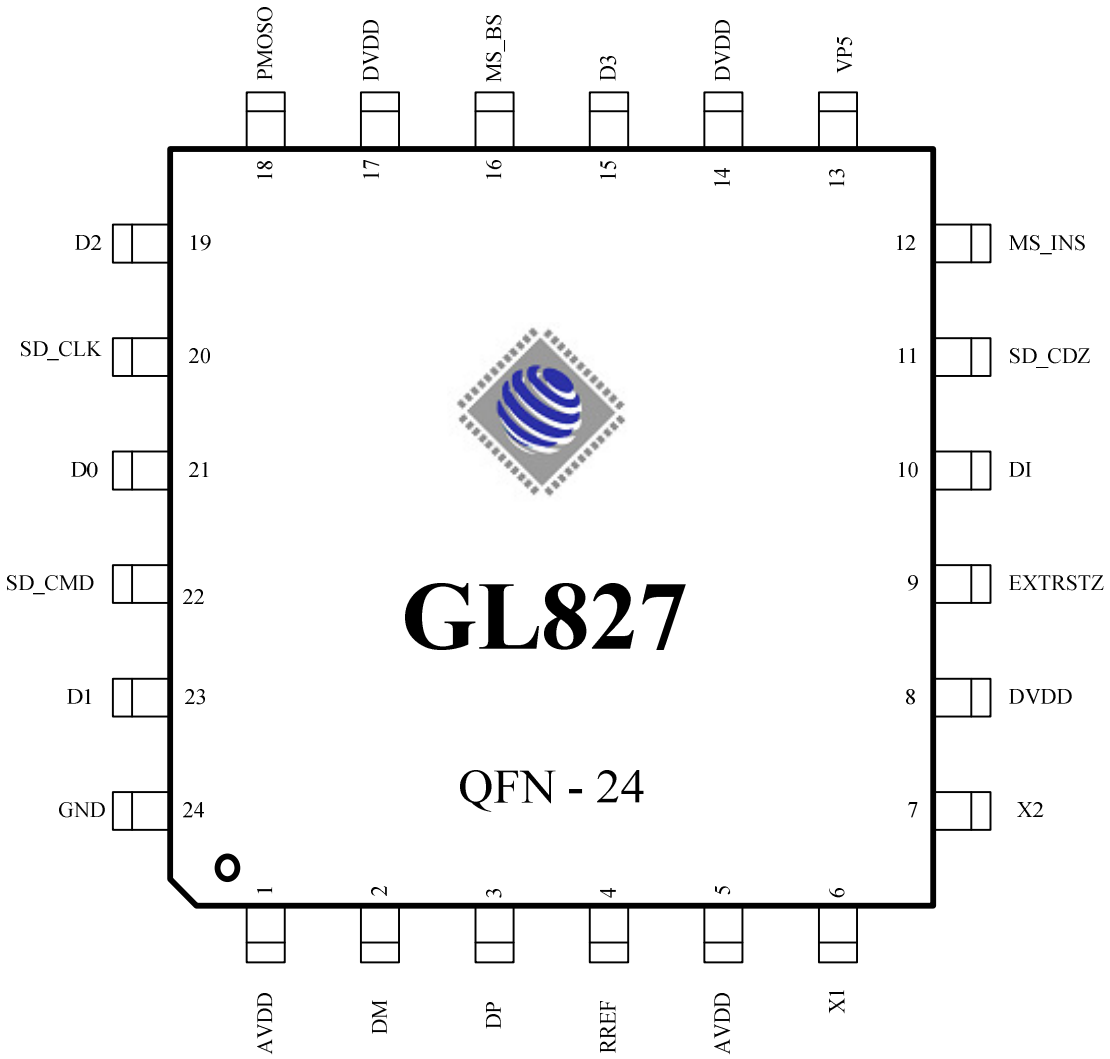


Figure 3.3 – 24 Pin QFN Pinout Diagram

Note: With Access LED / Without SD Write Protect

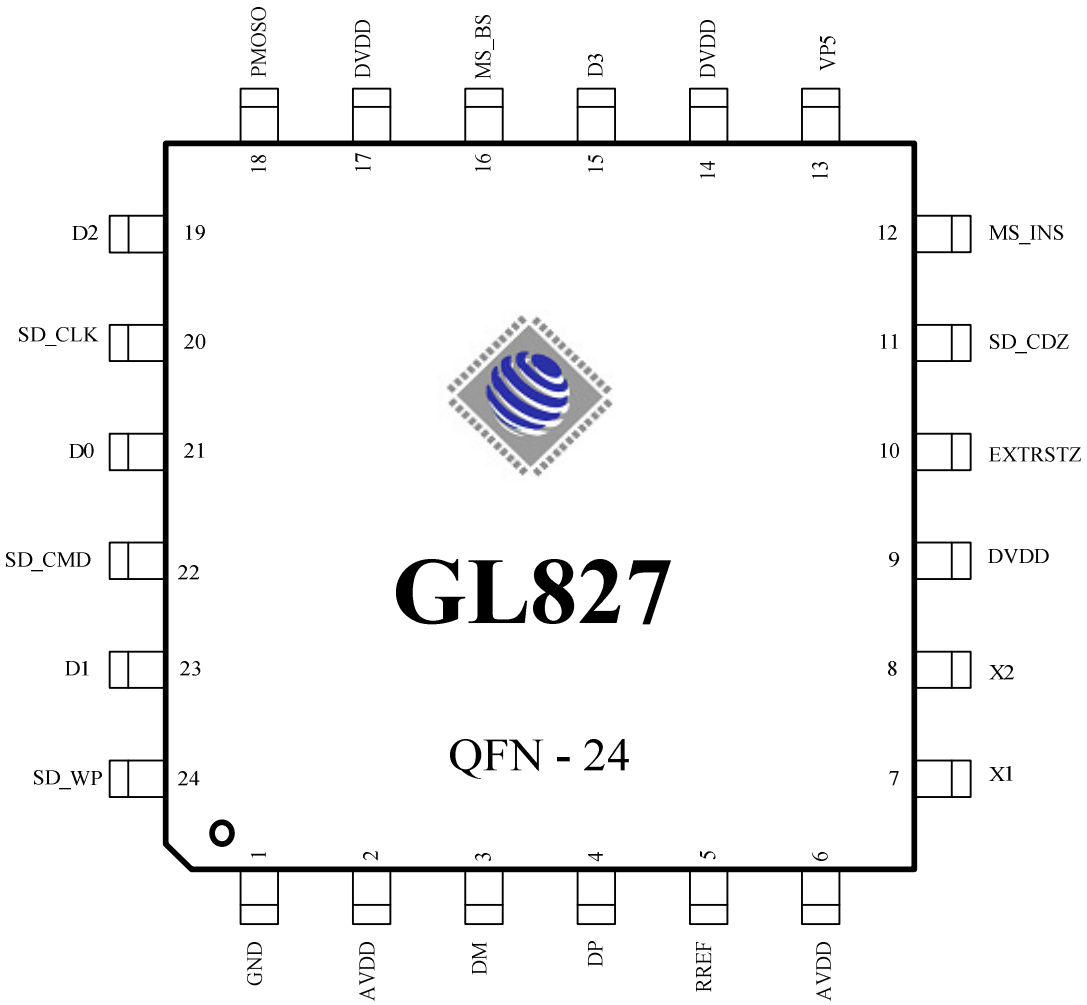


Figure 3.4 – 24 Pin QFN Pinout Diagram

Note: With SD Write Protect / Without Access LED (For combo card application)

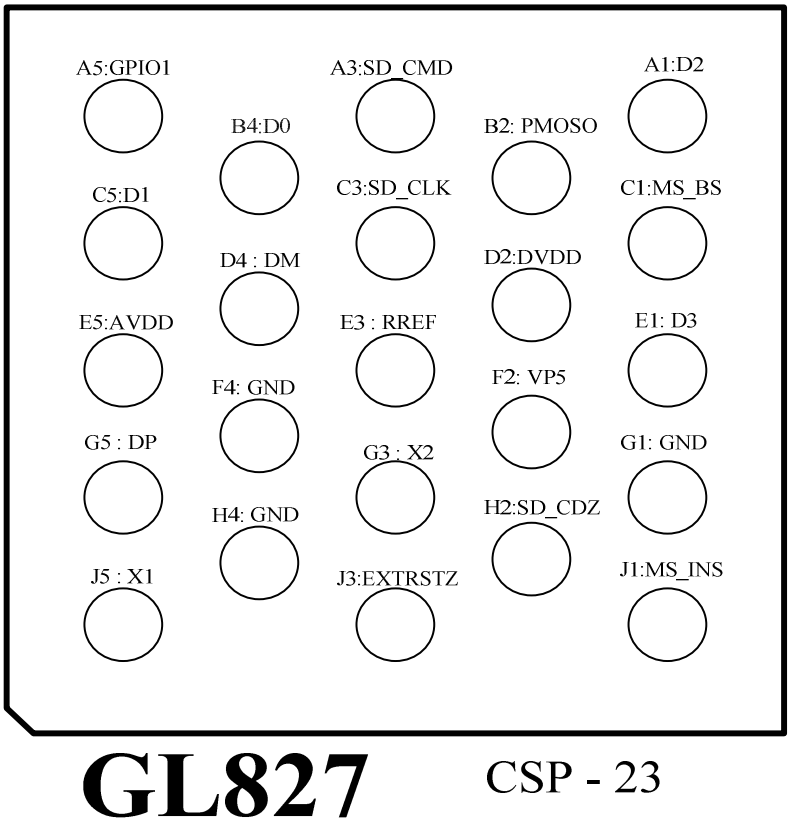


Figure 3.5 – 23 Pin CSP Pinout Diagram

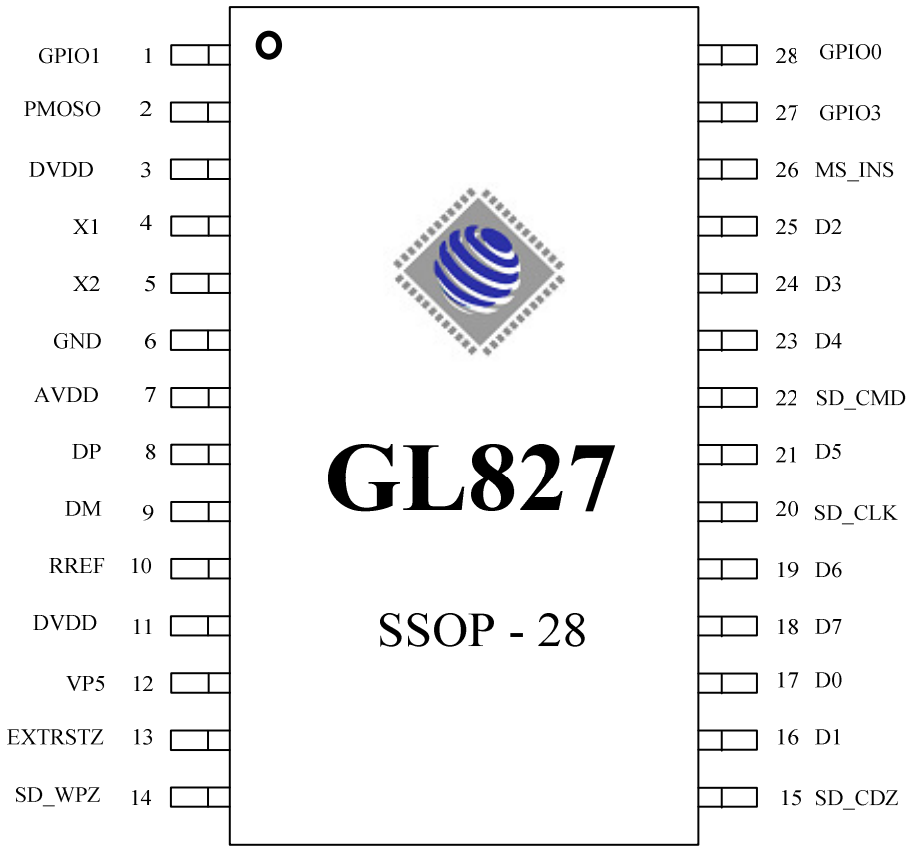


Figure 3.6 – 28 Pin SSOP Pinout Diagram

3.2 Pin List

Table 3.1 – LQFP 100 Pin List

Pin#	GL827 Pin name	Type	Pin#	GL827 Pin name	Type	Pin#	GL827 Pin name	Type
1	MD0	B/I, pd	35	TEST_MOD	I, pd	69	GND	Power
2	MD1	B/I, pd	36	EXTRSTZ	I, pu	70	DVDD	Power
3	MD2	B/I, pd	37	MA0	O	71	DVDD	Power
4	MD3	B/I, pd	38	MA1	O	72	PMOSI	PMOS
5	XD_CDZ	B/I, pd	39	MA2	O	73	PMOSI	PMOS
6	SM_CDZ	B/I, pd	40	MA3	O	74	PMOSO	PMOS
7	SM_WPDZ/SD_WPZ	B/I, f	41	SK	B/I, pd	75	PMOSO	PMOS
8	MD4	B/I, pd	42	CS	B/I, pd	76	D2	B/I, f
9	MD5	B/I, pd	43	DO	B/I, pd	77	D7	B/I, f
10	MD6	B/I, pd	44	DI	B/I, pd	78	SM_ALE/ MS_SCLK/ SD__CLK	B/I, f
11	MD7	B/I, pd	45	MA4	O	79	MA10	O
12	VDD18O	Power	46	MA5	O	80	MA11	O
13	GND	Power	47	MA6	O	81	MA12	O
14	GND	Power	48	SD_CDZ	B/I, pd	82	MA13	O
15	N/C	—	49	MS_INS	B/I, pd	83	D0	B/I, f
16	GND	Power	50	N/C	—	84	SM_REZ/SD_CMD	B/I, f
17	AVDD	Power	51	VP5	Power	85	SM_WEZ	B/I, pd
18	DM	A	52	VP5	Power	86	MA14	O
19	DP	A	53	VP3	Power	87	MA15	O
20	GND	Power	54	VP3	Power	88	MOEZ	B/O, pu
21	GND	Power	55	DVDD	Power	89	MWEZ	B/O, pu
22	RREF	A	56	DVDD	Power	90	MCSZ	B/O, pu
23	AVDD	Power	57	GND	Power	91	D1	B/I, f
24	AVDD	Power	58	GND	Power	92	SM_RBZ	B/I, pd
25	N/C	—	59	MA7	O	93	SM_WPZ	B/I, pd
26	N/C	—	60	MA8	O	94	EAB	B/I, pd
27	GND	Power	61	MA9	O	95	GPIO6	B/I, pd
28	X1	OSC	62	D4	B/I, f	96	GPIO5	B/I, pd
29	X2	OSC	63	D3	B/I, f	97	GPIO4	B/I, pd
30	AVDD	Power	64	D5	B/I, f	98	GPIO3	B/I, pd
31	DVDD	Power	65	GPIO0 (SM_CE)	B/O, pd	99	GPIO2	B/I, pd
32	DVDD	Power	66	D6	B/I, f	100	GPIO1	B/I, pd
33	GND	Power	67	SM_CLE/MS_BS	B/I, f			
34	GND	Power	68	GND	Power			

Table 3.2 – LQFP48 /LQFN48 Pin List

Pin#	GL827 Pin name	Type	Pin#	GL827 Pin name	Type	Pin#	GL827 Pin name	Type
1	XD_CDZ	B/I, pd	17	TEST_MOD	I, pd	33	SM_CLE/MS_BS	B/I, f
2	SM_CDZ	B/I, pd	18	EXTRSTZ	I, pu	34	GND	Power
3	SM_WPDZ/ SD_WPZ	B/I, f	19	SK	B/I, pd	35	DVDD	Power
4	VDD18O	Power	20	CS	B/I, pd	36	PMOSO	PMOS
5	GND	Power	21	DO	B/I, pd	37	D2	B/I, f
6	AVDD	Power	22	DI	B/I, pd	38	D7	B/I, f
7	DM	A	23	SD_CDZ	B/I, pd	39	SM_ALE/MS_SCLK/ SD_CLK	B/I, f
8	DP	A	24	MS_INS	B/I, pd	40	D0	B/I, f
9	GND	Power	25	VP5	Power	41	SM_REZ/SD_CMD	B/I, f
10	RREF	A	26	DVDD	Power	42	SM_WEZ	B/I, pd
11	AVDD	Power	27	GND	Power	43	D1	B/I, f
12	GND	Power	28	D4	B/I, f	44	SM_RBZ	B/I, pd
13	X1	OSC	29	D3	B/I, f	45	SM_WPZ	B/I, pd
14	X2	OSC	30	D5	B/I, f	46	GPIO3	B/I, pd
15	DVDD	Power	31	GPIO0 (SM_CE)	B/O, pd	47	GPIO2	B/I, pd
16	GND	Power	32	D6	B/I, f	48	GPIO1	B/I, pd

Table 3.3 – QFN24 Pin List

Pin#	GL827 Pin name	Type	Pin#	GL827 Pin name	Type	Pin#	GL827 Pin name	Type
1	AVDD	Power	9	EXTRSTZ	I, pu	17	DVDD	Power
2	DM	A	10	DI	B/I, pd	18	PMOSO	PMOS
3	DP	A	11	SD_CDZ	B/I, pd	19	D2	B/I, f
4	RREF	A	12	MS_INS	B/I, pd	20	SD_CLK	B/I, f
5	AVDD	Power	13	VP5	Power	21	D0	B/I, f
6	X1	OSC	14	DVDD	Power	22	SD_CMD	B/I, f
7	X2	OSC	15	D3	B/I, f	23	D1	B/I, f
8	DVDD	Power	16	MS_BS	B/I, f	24	GND	Power

Note: With Access LED / Without SD Write Protect

Table 3.4 – QFN24 Pin List

Pin#	GL827 Pin name	Type	Pin#	GL827 Pin name	Type	Pin#	GL827 Pin name	Type
1	GND	Power	9	DVDD	Power	17	DVDD	Power
2	AVDD	Power	10	EXTRSTZ	I, pu	18	PMOSO	PMOS
3	DM	A	11	SD_CDZ	B/I, pd	19	D2	B/I, f
4	DP	A	12	MS_INS	B/I, pd	20	SD_CLK	B/I, f
5	RREF	A	13	VP5	Power	21	D0	B/I, f
6	AVDD	Power	14	DVDD	Power	22	SD_CMD	B/I, f
7	X1	OSC	15	D3	B/I, f	23	D1	B/I, f
8	X2	OSC	16	MS_BS	B/I, f	24	SD_WP	B/I, pd

Note: With SD Write Protect / Without Access LED (For combo card application)

Table 3.5 – CSP23 Pin List

Pin#	GL827 Pin name	Type	Pin#	GL827 Pin name	Type	Pin#	GL827 Pin name	Type
A1	D2	B/I, f	D2	DVDD	Power	G1	GND	Power
A3	SD_CMD	B/I, f	D4	DM	A	G3	X2	OSC
A5	GPIO1	B/I, pd	E1	D3	B/I, f	G5	DP	A
B2	PMOSO	PMOS	E3	RREF	A	H2	SD_CDZ	B/I, pd
B4	D0	B/I, f	E5	AVDD	Power	H4	GND	Power
C1	MS_BS	B/I, f	F2	VP5	Power	J1	MS_INS	B/I, pd
C3	SD_CLK	B/I, f	F4	GND	Power	J3	EXTRSTZ	I, pu
C5	D1	B/I, f				J5	X1	OSC

Table 3.6 – SSOP28 Pin List

Pin#	GL827 Pin name	Type	Pin#	GL827 Pin name	Type	Pin#	GL827 Pin name	Type
1	GPIO1	B/I, pd	11	DVDD	Power	21	D5	B/I, f
2	PMOSO	PMOS	12	VP5	Power	22	SD_CMD	B/I, f
3	DVDD	Power	13	EXTRSTZ	I, pu	23	D4	B/I, f
4	X1	OSC	14	SD_WPZ	B/I, f	24	D3	B/I, f
5	X2	OSC	15	SD_CDZ	B/I, f	25	D2	B/I, f
6	GND	Power	16	D1	B/I, f	26	MS_INS	B/I, pd
7	AVDD	Power	17	D0	B/I, f	27	GPIO3	B/I, pd
8	DP	A	18	D7	B/I, f	28	GPIO0	B/I, pd
9	DM	A	19	D6	B/I, f			
10	RREF	A	20	SD_CLK	B/I, f			

3.3 Pin Descriptions

Table 3.7 - Pin Descriptions

Pin name	LQFP100	LQFP48	SSOP28	QFN24	QFN24	CSP23	Type	Description
VDD18O	12	4	N/A	N/A	N/A	N/A	P	Internal regulator 1.8V output
GND	13,14,16,20,21, 27	5,9,12	6	N/A	N/A	F4,H4	P	Analog ground
AVDD	17,23,24,30	6,11	7	1,5	2,6	E5	P	Analog power
N/C	15	N/A	N/A	N/A	N/A	N/A	A	Test only
DM	18	7	9	2	3	D4	A	USB D-
DP	19	8	8	3	4	G5	A	USB D+
RREF	22	10	10	4	5	E3	A	Reference resistor
X1	28	13	4	6	7	J5	OSC	12MHz/48MHz input. This pin can be connected to one terminal of crystal or external 12MHz/48MHz clock source.
X2	29	14	5	7	8	G3	OSC	12MHz/48MHz output. This is another terminal of the crystal or NC when using an external 12MHz/48MHz clock source is used to drive PLL.
DVDD	31,32,55,56,70, 71	15,26,35	3,,11	8,14,17	9,14,17	D2	P	Digital power 3.3V
GND	33,34,57,58,68, 69	16,27,34	6	24	1	G1	P	Digital ground
VP5	51,52	25	12	13	13	F2	P	Regulator 5V Input
VP3	53,54	N/A	N/A	N/A	N/A	N/A	P	Regulator 3.3V output
PMOSI	72,73	N/A	N/A	N/A	N/A	N/A	PMOS	Power MOS 3.3V input
PMOSO	74,75	36	2	18	18	B2	PMOS	Power MOS 3.3V output
TEST_MOD	35	17	N/A	N/A	N/A	N/A	I, pd	Test mode selection
EXTRSTZ	36	18	13	9	10	J3	I, pu	External reset. It is active low. The low pulse should be 1 us width at least.
EAB	94	N/A	N/A	N/A	N/A	N/A	B/I, pu	Ext flash selection
SM_CDZ	6	2	N/A	N/A	N/A	N/A	B/I, pd	SmartMedia Card detection. Normal High,

								active low.
XD_CDZ	5	1	N/A	N/A	N/A	N/A	B/I, pd	xD-Picture Card detection. Normal High, active low.
MS_INS	49	24	26	12	12	J1	B/I, pd	Memory Stick INS. Normal High, active low.
SD_CDZ	48	23	15	11	11	H2	B/I, pd	SD& MMC Card detection. Normal High, active low.
D0~D7	83,91,76,63,62, 64,66,77	40,43,37, 29,28,30, 32,38	17,16,25, 24,23,21, 19,18	21,23, 19,15	21,23, 19,15	B4,C5, A1,E1	B/I, f	SM data 0~7 MS data 0~3 SD data 0~3 MMC data 0~7
GPIO0 (SM_CE)	65	31	28	N/A	N/A	N/A	B/O, pd	SmartMedia card Chip Enable
SM_ALE/ MS_SCLK/ SD_CLK	78	39	20	20	20	C3	B/I, f	SmartMedia ALE/ MemoryStick SCLK/ SD/MMC CLK
SM_WPDZ/ SD_WPZ	7	3	14	N/A	24	N/A	B/I, f	SM_WPDZ: SmartMedia seal. SD_WPZ: SD Write Protect Detection. When no card is inserted, pull low. When SM or SD card is inserted, the pin is pull up and active low.
SM_CLE/ MS_BS	67	33	22 (MS_BS/ SD_CMD)	16	16	C1	B/I, f	SmartMedia CLE/ Memory Stick BS
SM_REZ/ SD_CMD	84	41		22	22	A3	B/I, f	SmartMedia REZ/ SD/MMC CMD
SM_WEZ	85	42	N/A	N/A	N/A	N/A	B/I, pd	SmartMedia WE
SM_RBZ	92	44	N/A	N/A	N/A	N/A	B/I, pd	SmartMedia RDY/BSY
SM_WPZ	93	45	N/A	N/A	N/A	N/A	B/I, pd	SmartMedia Write Protect Detection. When no card is inserted, pull low. When SM card is inserted, the pin is pull up and active low.
GPIO1~6	100~95	48~46	1, 27	N/A	N/A	A5	B/I, pd	GPIO1~6 GPIO3 : Power LED
SK	43	19	N/A	N/A	N/A	N/A	B/I, pd	93C46 Clock
CS	44	20	N/A	N/A	N/A	N/A	B/I, pd	93C46 CS

DO	45	21	N/A	N/A	N/A	N/A	B/I, pd	93C46 Data out
DI	46	22	N/A	10	N/A	N/A	B/I, pd	93C46 Data in / Access LED
MD0~7	1~4, 8~11	N/A	N/A	N/A	N/A	N/A	B/I, pd	Ext. flash data 0~7
MA0~15	37~40,35~47,59~61,79~82,86~87	N/A	N/A	N/A	N/A	N/A	O	Ext. flash address 0~15
MOEZ	88	N/A	N/A	N/A	N/A	N/A	B/O, pu	Ext. flash OE
MWEZ	89	N/A	N/A	N/A	N/A	N/A	B/O, pu	Ext. flash WE
MCSZ	90	N/A	N/A	N/A	N/A	N/A	B/O, pu	Ext. flash CS

Notation:

Type	**A**	Analog
	B	Bi-directional
	B/I	Bi-directional, default input
	B/O	Bi-directional, default output
	I	Input
	O	Output
	OSC	Oscillator
	P	Power / Ground
	f	Internal floating
	pd	Internal pull down
	pu	Internal pull up

CHAPTER 4 BLOCK DIAGRAM

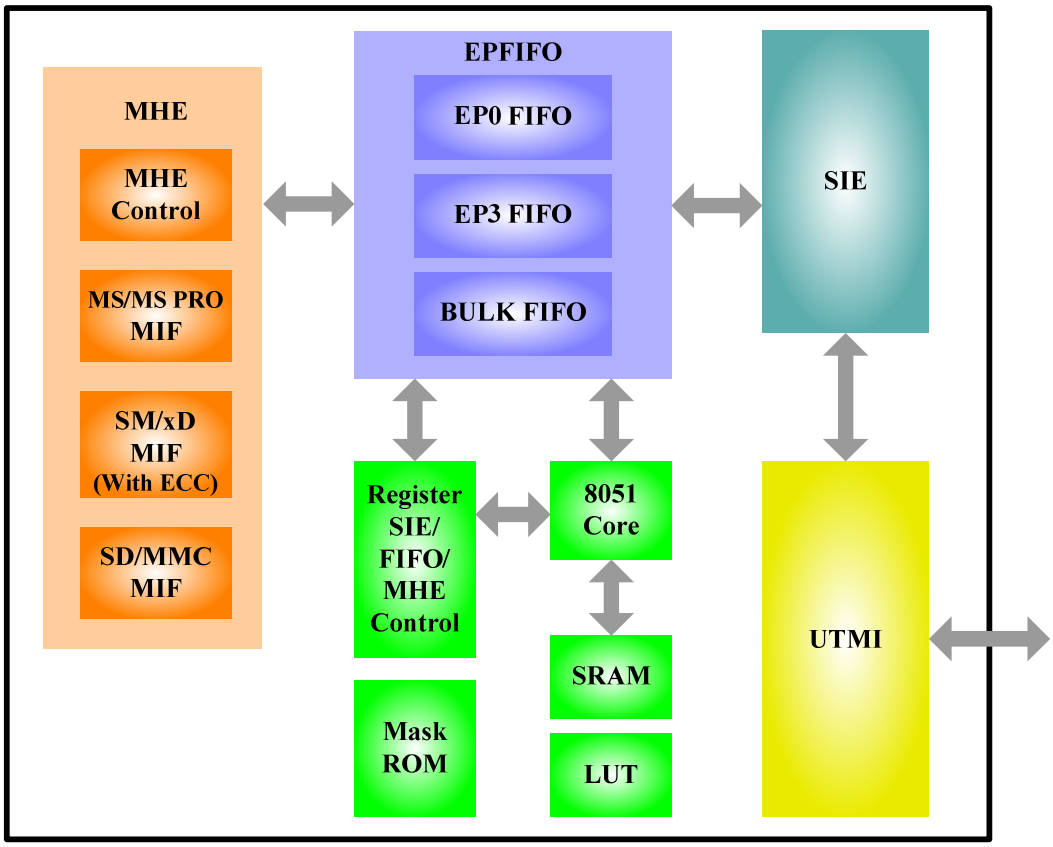


Figure 4.1 - Block Diagram

CHAPTER 5 FUNCTION DESCRIPTION

UTM

The USB 2.0 Transceiver Macrocell is the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB 2.0 rate to one that is compatible with the general logic.

SIE

The Serial Interface Engine, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

EPFIFO

Endpoint FIFO includes Control FIFO (FIFO0), interrupt FIFO (FIFO3), Bulk In/Out FIFO (BULKFIFO)

- **Control FIFO** FIFO of control endpoint 0.
  It is 64-byte FIFO, and it is used for endpoint 0 data transfer.
- **Interrupt FIFO** 64-byte depth FIFO of endpoint 3 for status interrupt
- **Bulk In/Out FIFO** It can be in the TX mode or RX mode:
  1. It contains ping-pong FIFO (512 bytes each bank) for transmit/receive data continuously.
  2. It can be directly accessed by Uc
  3. Automatic hardware SmartMedia ECC error correction support

MHE

It contains 4 MIFs (Media Interface)

- **MIFs**
  1. SmartMedia / xD/ Flash
  2. SD / MMC
  3. MemoryStick
  4. MemoryStick PRO
- **Remote wakeup**
  Support Card insert wakeup while suspend.
- **External reset circuit**
  Non-inverting, Schmitt input with weak pull-up using DVDD power.

CLOCK Source Selection

It selects 12/48 MHz input by exterior pull resistor.

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Table 6.1 - Absolute Maximum Ratings

Parameter	Value
Storage Temperature	-65°C to +150 °C
Ambient Temperature	-40°C to +80 °C
Supply Voltage to Ground Potential	-0.5V to +4.0V
DC Input Voltage to Any Pin	-0.5V to +5.8V

6.2 Operating Conditions

Table 6.2 - Operating Conditions

Parameter	Value
Ta (Ambient Temperature Under Bias)	0°C to 70°C
Supply Voltage	+3.0V to +3.6V
Ground Voltage	0V
F_{OSC} (Oscillator or Crystal Frequency)	12 MHz ± 0.05% 12 MHz ± 0.25% (for USB full-speed only)

6.3 DC Characteristics

Table 6.3 - DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{REG}	Regulation Supply Voltage		4.5	-	5.5	V
V_{CC}	Supply Voltage		3.0	-	3.6	V
V_{IH}	Input High Voltage		2.0	-	3.6	V
V_{IL}	Input Low Voltage		-0.3	-	0.8	V
I_I	Input Leakage current	$0 < V_{IN} < V_{CC}$	-10	-	10	µA
V_{OH}	Output High Voltage		2.4	-	-	V
V_{OL}	Output Low Voltage		-	-	0.4	V
I_{OH}	Output Current High	VDD=3.3V V_{OH}=2.4V	-	8	-	mA
I_{OL}	Output Current Low	VDD=3.3V V_{OL}=0.4V		8	-	mA
C_{IN}	Input Pin Capacitance		-	5	-	pF
I_{SUSP}	Suspend current	1.5K external pull-up included	-	-	450	µA
I_{CC}	Supply current	Connect to USB with 8051 operating	-	-	60	mA

6.4 PMOS Characteristics

Table 6.4 - PMOS Driving Strength versus Junction Temperature

(Core Power=1.8V, IO Power=3.3V)

Junction Temperature	25 °C
Driving Strength (mA)	158.4 ± 10%
On-Resistance (ohm)	1.61 ± 10%

Note:
1. Driving strength is defined as the PMOS sinking current when Vio=3.3V, Vd=3.0V.
2. On-resistance is calculated by 0.2V divided by driving strength.

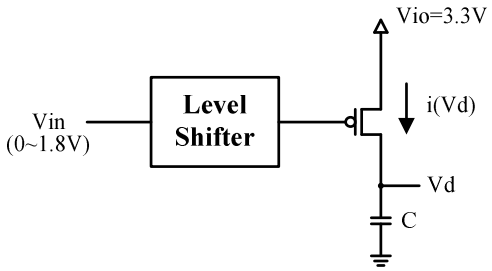


Figure 6.1 - Embedded PMOS Switch Architecture

6.5 5V to 3.3 V Regulator Characteristics

Table 6.5 – Regulator Output Current

Parameters	Description	Test Conditions	Min.	Typ..	Max.	Units
Iq	Quiescent current	no loading	10	18	25	uA
Io_max	Output driving capability	V33 > 2.9V	200	500	600	mA
Vo_0mA	V33 voltage without loading		3.0	3.4	3.57	V
Vo_200mA	V33 voltage with 200mA load		2.9	3.34	3.52	V

6.6 AC Characteristics

6.6.1 UTMI Transceiver

The GL827 is fully compatible with Universal Serial Bus specification rev. 2.0 and USB 2.0 Transceiver Macercell Interface (UTMI) specification rev. 1.01. Please refer to the specification for more information.

6.6.2 External Flash

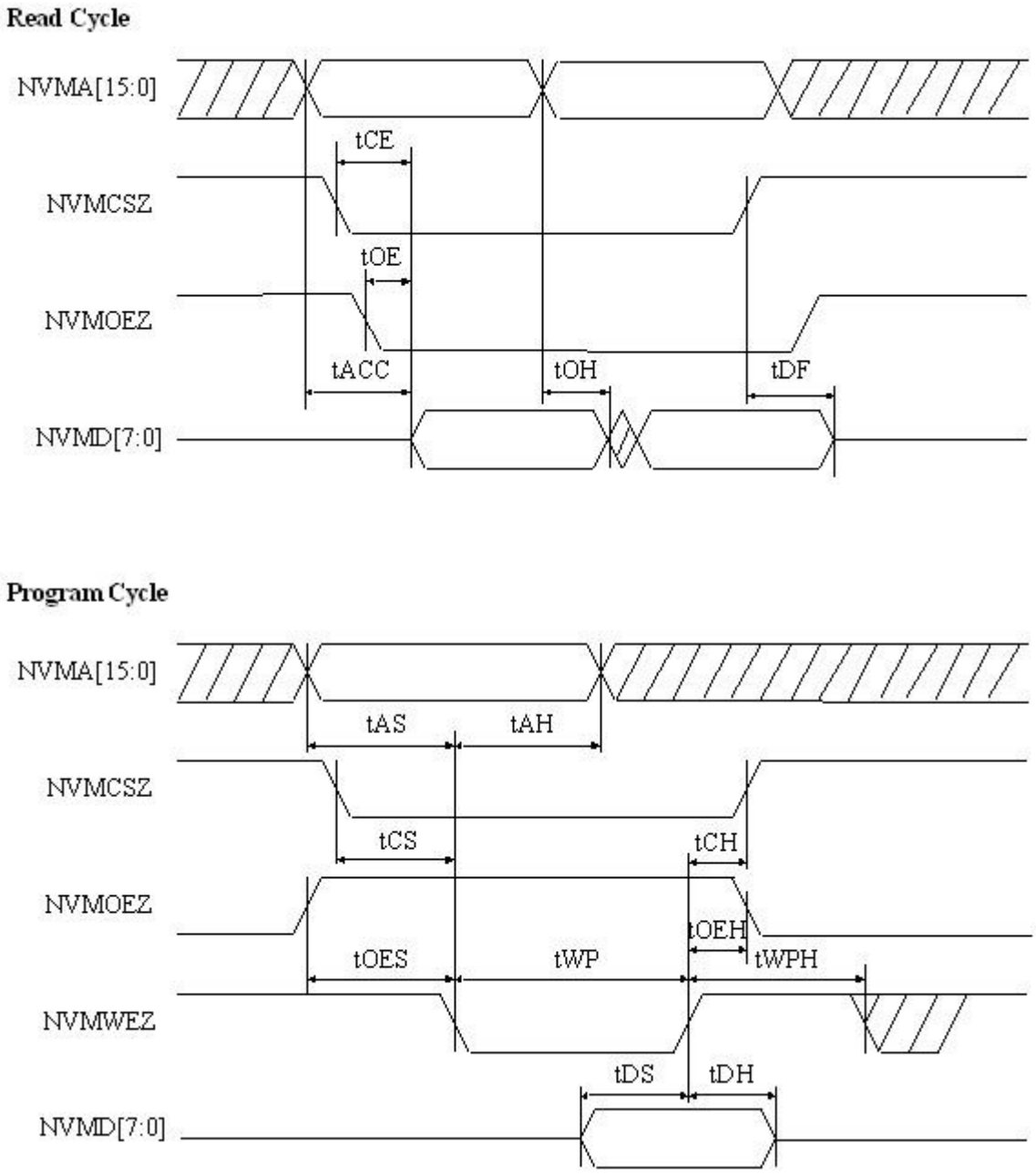


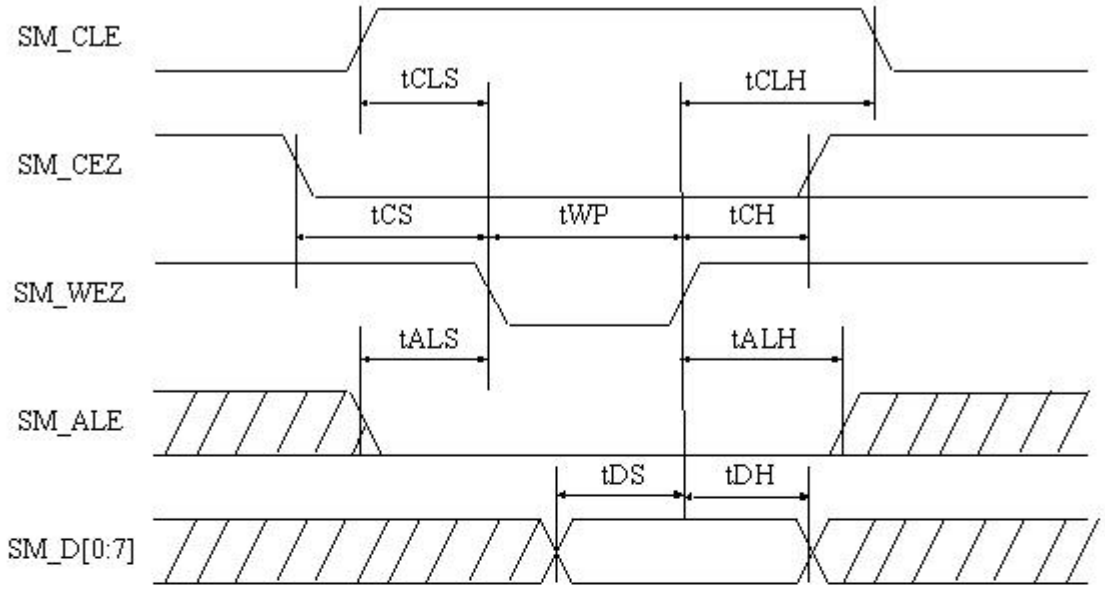
Figure 6.2 - Timing Diagram of External Flash

AC Characteristics of Flash Interface (C_{LOAD} = 30pF)

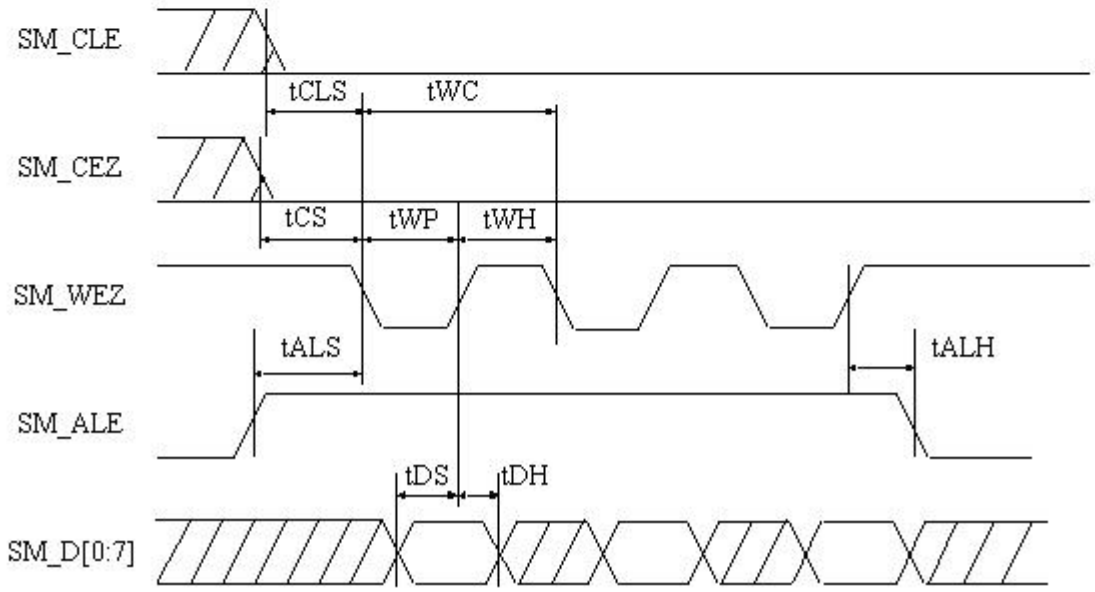
Symbol	Parameter	Max	Unit
tACC	Address to Output Delay (max)	83	ns
tCE	NVMCSZ to Output Delay (max)	83	
tDF	NVMCEZ or NVMOEZ, whichever occurred first, to Output Float (max)	0	
tOH	Output Hold from NVMOEZ, NVMCSZ or Address, whichever occurred first (min)	0	
tAS	Address Setup Time (min)	760	
tAH	Address Hold Time (min)	760	
tOES	NVMOEZ Setup Time (min)	300	
tCS	NVMCSZ Setup Time (min)	0	
tCH	NVMCSZ Hold Time (min)	0	
tWP	Write Pulse Width (min)	66	
tWPH	Write Pulse Width High (min)	300	
tDS	Data Setup Time (min)	300	
tDH	Data Hold Time (min)	0	
tOEH	NVMOEZ Hold Time (min)	16	

6.6.3 SmartMedia

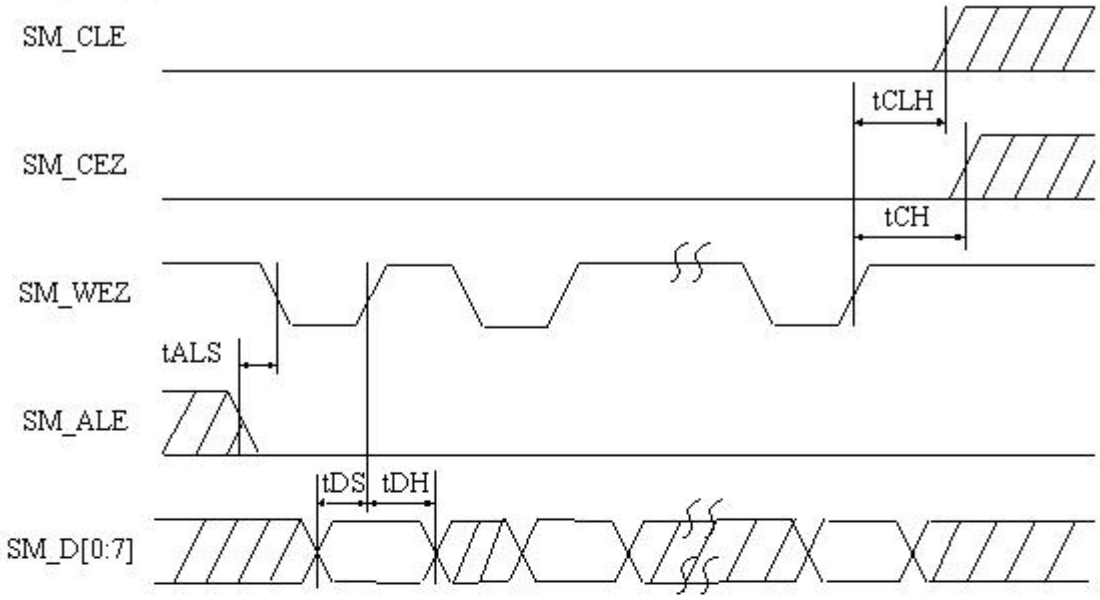
Command Input Cycle



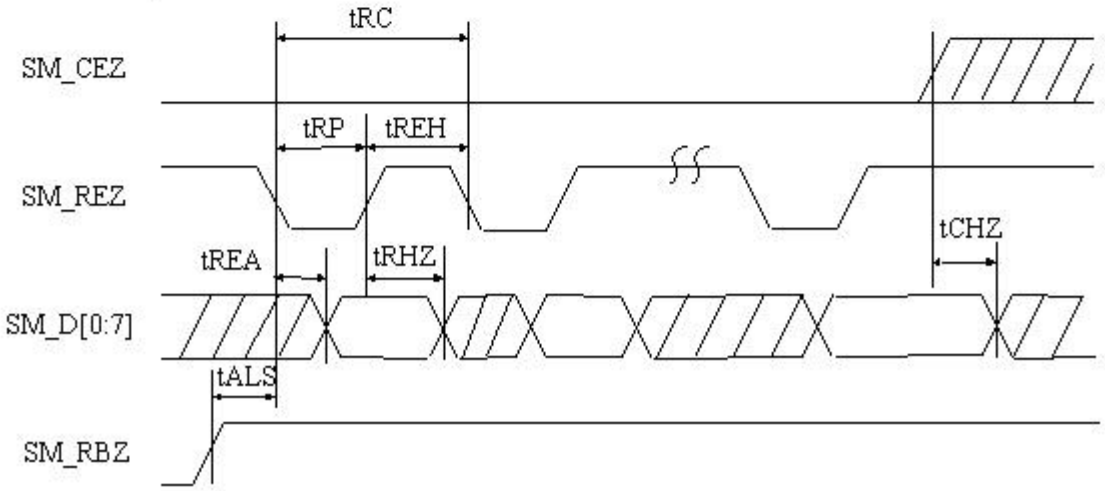
Address Input Cycle



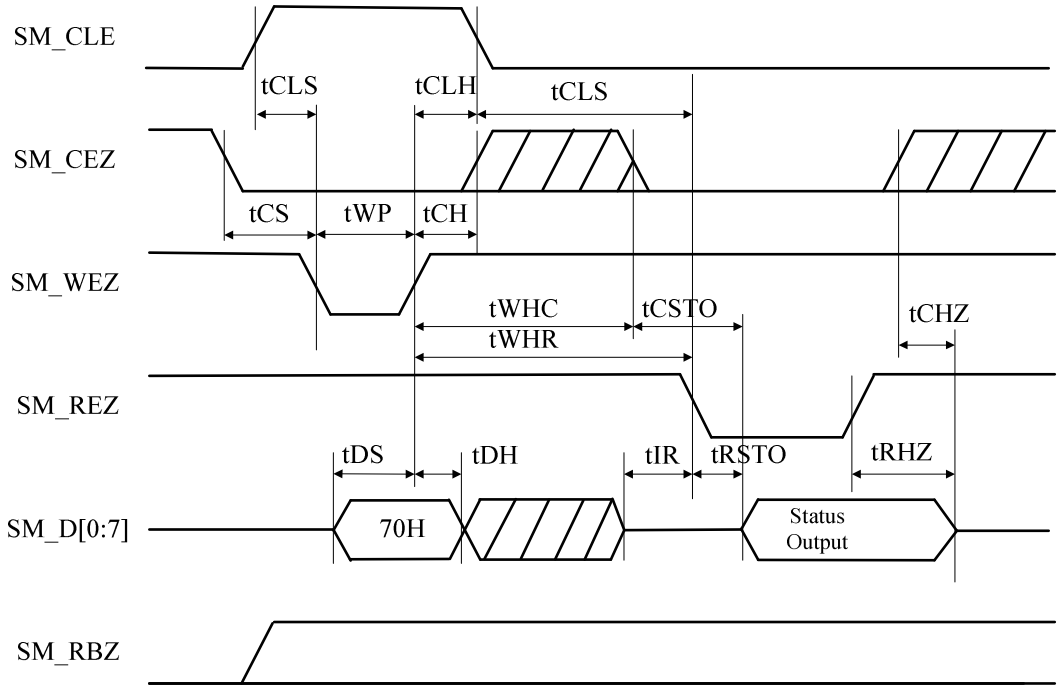
Data Input Cycle



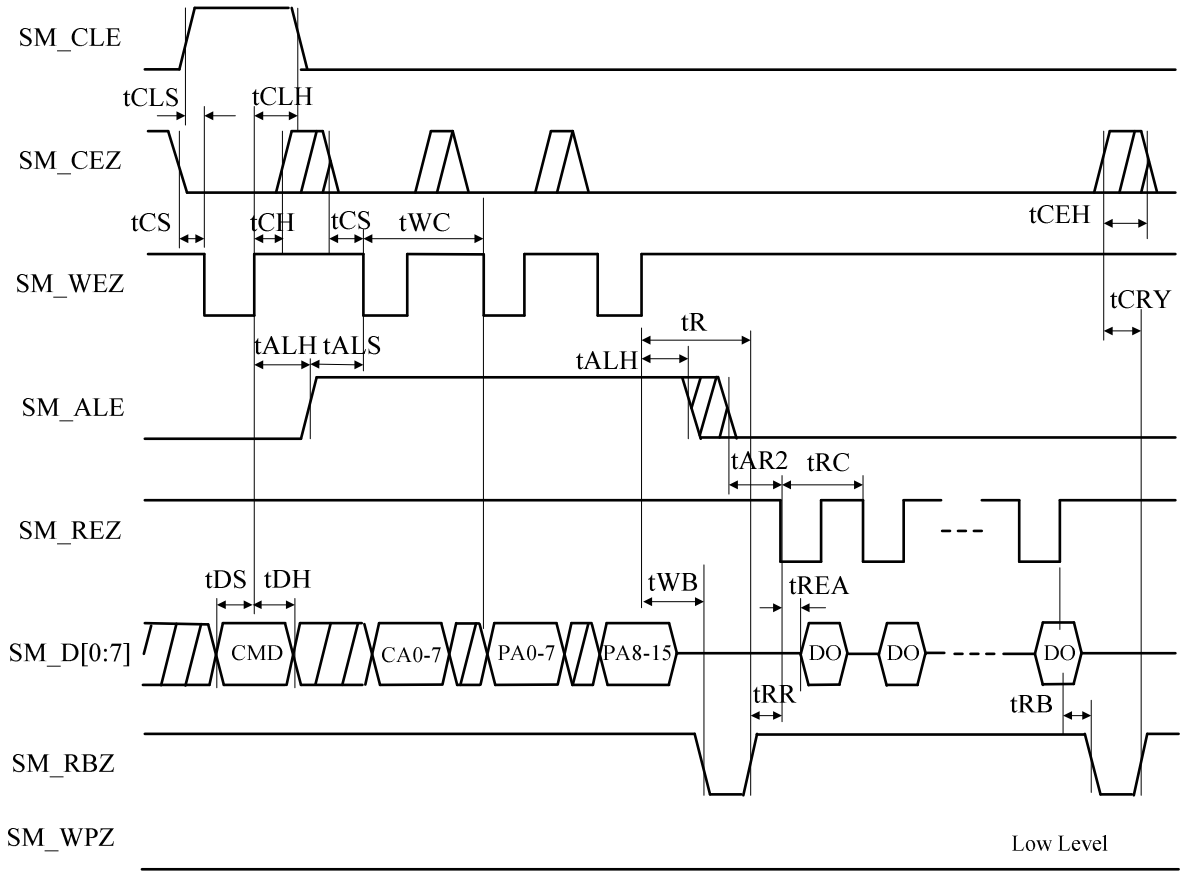
Serial Read Cycle



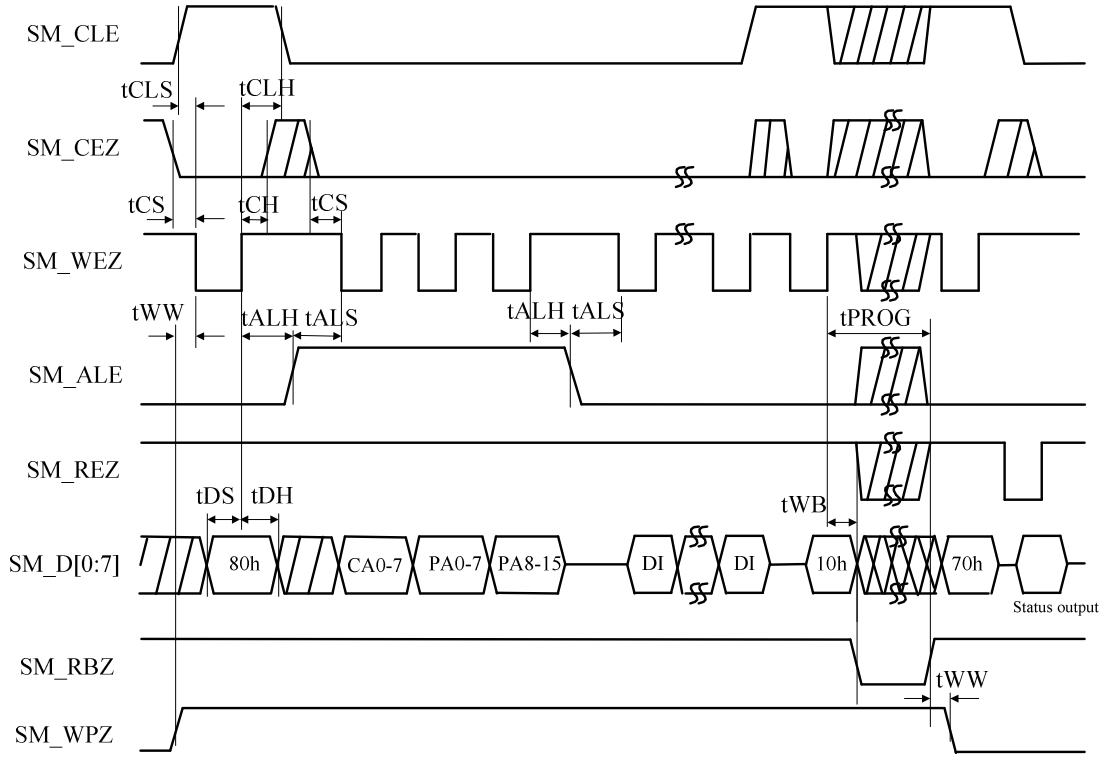
Status Read Cycle



Read Cycle



Auto Page Program Timing



ID Read Timing

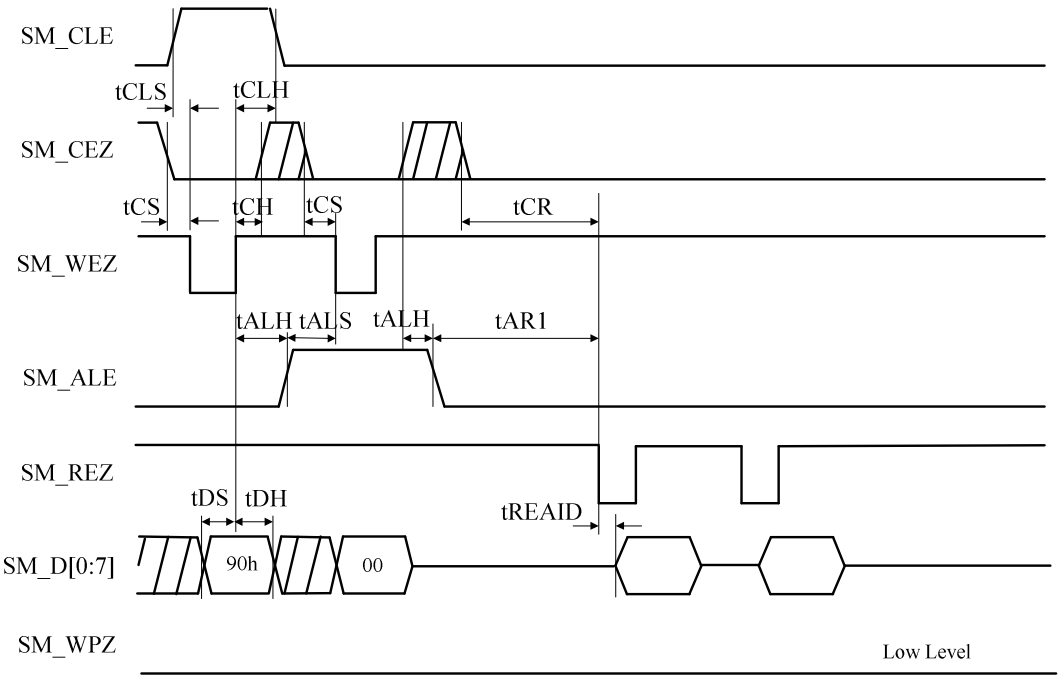


Figure 6.3 - Timing Diagram of SmartMedia

AC Characteristics of Smart Media Interface (C_{LOAD} = 30 pF)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
tCLS	CLE Setup Time	20	-	ns
tCLH	CLE Hold Time	40	-	ns
tCS	-CE Setup Time	20	-	ns
tCH	-CE Hold Time	40	-	ns
tWP	-WE Pulse Width	40	-	ns
tALS	ALE Setup Time	20	-	ns
tALH	ALE Hold Time	40	-	ns
tDS	Data Setup Time	30	-	ns
tDH	Data Hold Time	20	-	ns
tWC	Write Cycle Time	80	-	ns
tWH	-WE High Hold Time	20	-	ns
tWW	-WP High to –WE Low	100	-	ns
tRR	Ready to –RE Low	20	-	ns
tRP	Read Pulse Width	60	-	ns
tRC	Read cycle Time	80	-	ns
tREA	-RE Access Time (Serial Data Access)	-	45	ns
tCEH	-CE High Hold Time (At the Last Serial Read)	250	-	ns
tREAID	-RE Access Time (ID Read)	-	90	ns
tRHZ	-RE High to Output Hi-Z	5	30	ns
tCHZ	-CE High to Output Hi-Z	-	30	ns
tREH	-RE High Hold Time	20	-	ns
tRSTO	-RE Access Time	-	45	ns
tCSTO	-CE Access Time	-	55	ns
tRHW	-RE High to -WE Low	0	-	ns
tWHC	-WE High to –CE Low	50	-	ns
tWHR	-WE High to –RE Low	60	-	ns
tAR1	ALE Low to –RE Low (Address Register Read, ID Read)	200	-	ns
tCR	-CE Low to –RE Low (Data Register Read, ID Read)	200	-	ns
tWB	-WE High to Busy	-	200	ns
tAR2	ALE Low to RE Low (Read Cycle)	150		ns
tRB	Last –RE High to Busy (at Sequential Read)	-	500	ns
tCRY	-CE High to Ready	-	1	µs

6.6.4 xD

The Timing diagrams are the same as SM.

AC Characteristics:

Parameter	Description	Spec. Min	Spec. Max	Unit
tCLS	CLE Set up Time	20	-	ns
tCLH	CLE Hold Time	40	-	
tCS	CE Setup up Time	20	-	
tCH	CE Hold Time	40	-	
tWP	WE Pulse Width	40	-	
tALS	ALE Setup Time	20	-	
tALH	ALE Hold Time	40	-	
tDS	Data Setup Time	30	-	
tDH	Data Hold Time	20	-	
tWC	Write Cycle Time	80	-	
tWH	WE High Hold Time	20	-	
tWW	WP High to WE Low	100	-	
tRR	Ready to RE Low	20	-	
tRP	Read Pulse Width	60	-	
tRC	Read Cycle Time	80	-	
tREA	RE Access Time(Serial Data Access)	-	45	
tCEH	CE High Hold Time	250	-	
tREAID	RE Access Time(ID Read)	-	90	
tRHZ	RE High to Output Hi-Z	5	30	
tCHZ	CE High to Output Hi-Z	-	30	
tREH	RE High Hold Time	20	-	
tRSTO	RE Access Time	-	45	
tCSTO	CE Access Time	-	55	
tRHW	RE High to WE Low	0	-	
tWHC	WE High to CE Low	50	-	
tWHR	WE High to RE Low	60	-	
TAR1	ALE Low to RE Low	200	-	
tCR	CE Low to RE Low	200	-	
tWB	WE High to Busy	-	200	
TAR2	ALE LOW to RE LOW	150	-	
tRB	Last RE High to Busy	-	200	

6.6.5 Memory Stick

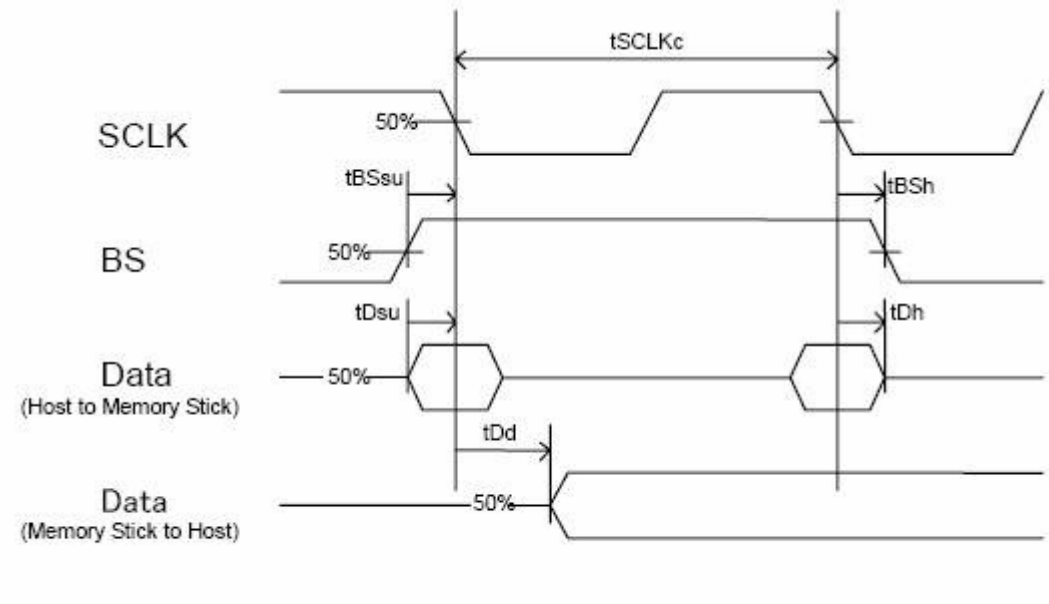


Figure 6.4 - MemoryStick Parallel Transfer Operation Timing

Memory Stick Frequency Mode

Parameter	Description	Mode	Typ	Unit	Remark
F_{SCLK}	SCLK frequency	0	1.5M	Hz	
		1	6M		
		2	15M		
		3	20M		

AC Characteristics of Memory Stick Interface (C_{LOAD} = 30 pF)

PARAMETER	DESCRIPTION	F_{SCLK} = 1.5 MHZ	F_{SCLK} = 6 MHZ	F_{SCLK} = 15 MHZ	F_{SCLK} = 20 MHZ	UNIT
tSCLKc	SCLK Cycle	666.6	166.6	66.6	50.0	ns
tSCLKwh	SCLK H pulse length (min)	323.3	73.3	23.3	15	ns
tSCLKwl	SCLK L pulse length (min)	323.3	73.3	23.3	15	ns
tSCLKr	SCLK rise time (min)	5	5	5	5	ns
tSCLKr	SCLK rise time (max)	10	10	10	10	ns
tSCLKf	SCLK Fall time (min)	5	5	5	5	ns
tSCLKf	SCLK Fall time (max)	10	10	10	10	ns
tBSsu	BS setup time (min)	5	5	5	5	ns
tBSh	BS hold time (min)	5	5	5	5	ns

tDsu	DATA setup time (min)	5	5	5	5	ns
tDh	DATA hold time (min)	5	5	5	5	ns
tDd	DATA output delay time (max)	5	5	5	5	ns

6.6.6 Memory Stick PRO

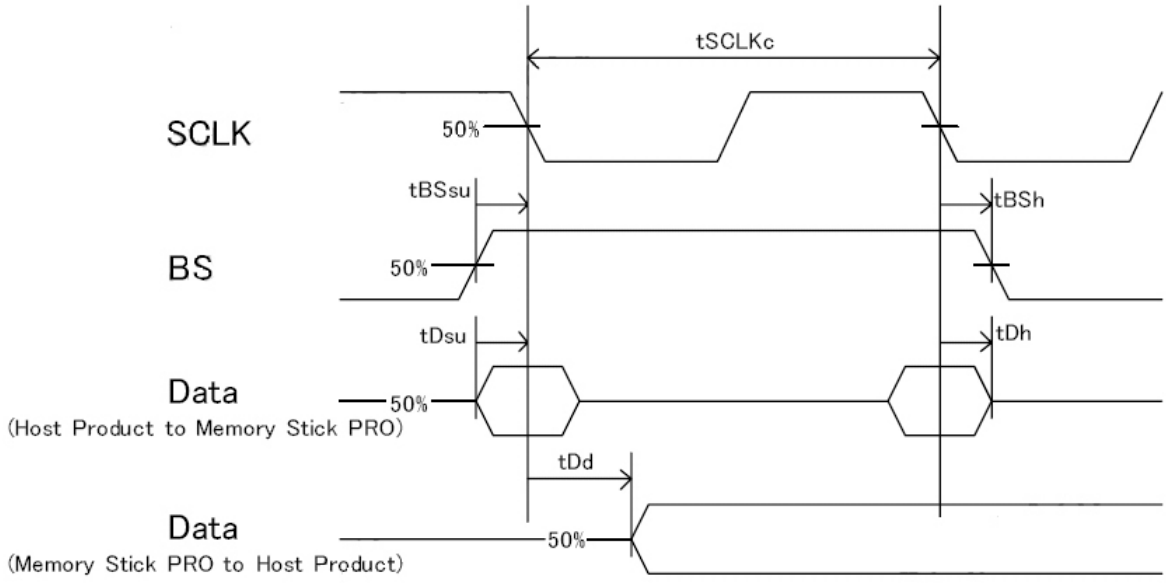


Figure 6.5 - MemoryStick PRO Parallel Transfer Operation Timing

Memory Stick PRO Frequency Mode

Parameter	Description	Mode	Typ.	Unit	Remark
F_{SCLK}	SCLK frequency	0	1.5M	Hz	Same as Memory Stick
		1	6M		
		2	15M		
		3	20M		
		4	30M		
		5	40M		

AC Characteristics of MS Interface (C_{LOAD} = 15 pF)

PARAMETER	DESCRIPTION	F_{SCLK} = 30 MHZ	F_{SCLK} = 40 MHZ	UNIT
tSCLKc	SCLK Cycle	33.3	25.0	ns
tSCLKwh	SCLK H pulse length (min)	9	5	ns

tSCLKwl	SCLK L pulse length (min)	9	5	ns
tSCLKr	SCLK rise time (min)	5	5	ns
tSCLKr	SCLK rise time (max)	7.5	7.5	ns
tSCLKf	SCLK Fall time (min)	5	5	ns
tSCLKf	SCLK Fall time (max)	7.5	7.5	ns
tBSsu	BS setup time (min)	8	8	ns
tBSh	BS hold time (min)	1	1	ns
tDsu	DATA setup time (min)	8	8	ns
tDh	DATA hold time (min)	1	1	ns
tDd	DATA output delay time (max)	5	5	ns

6.6.7 Secure Digital

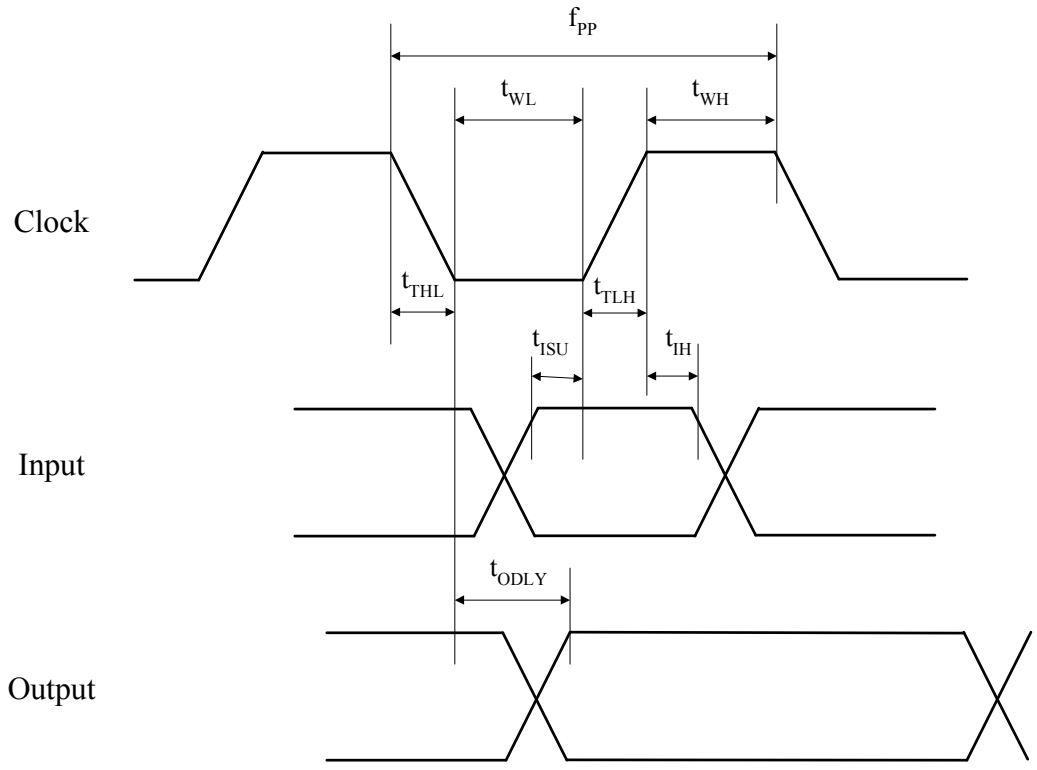


Figure 6.6 - Timing Diagram of Secure Digital (Default)

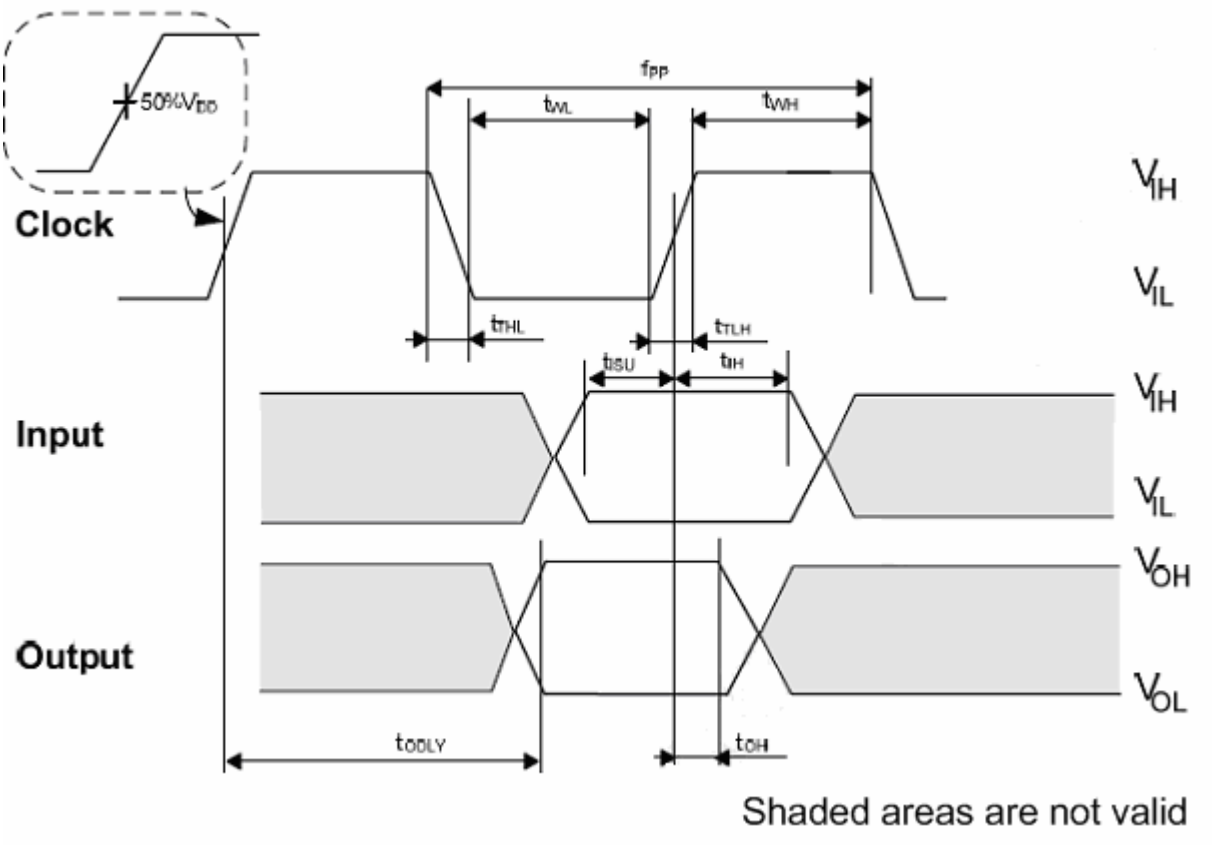


Figure 6.7 - Timing Diagram of Secure Digital (High-Speed Mode)

SD Interface Timing (C_L = 30PF)

SYMBOL	PARAMETER	CLOCK RATE		UNIT
f_{PP}	Clock frequency Data Transfer Mode	48	24	MHz
f_{OD}	Clock frequency Identification Mode	375	375	KHz
t_{WL}	Clock low time (min)	7.4	16.8	ns
t_{WH}	Clock high time (min)	7.4	16.8	ns
t_{TLH}	Clock rise time (max)	3	4	ns
t_{THL}	Clock fall time (max)	3	4	ns
t_{ISU}	Input set-up time (min)	6	6	ns
t_{IH}	Input hold time (min)	0	0	ns

6.6.8 Reset Timing

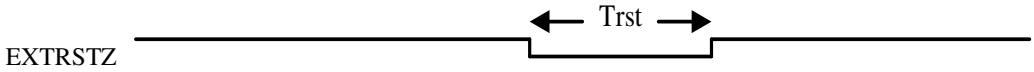


Figure 6.8 - Timing Diagram of Reset width

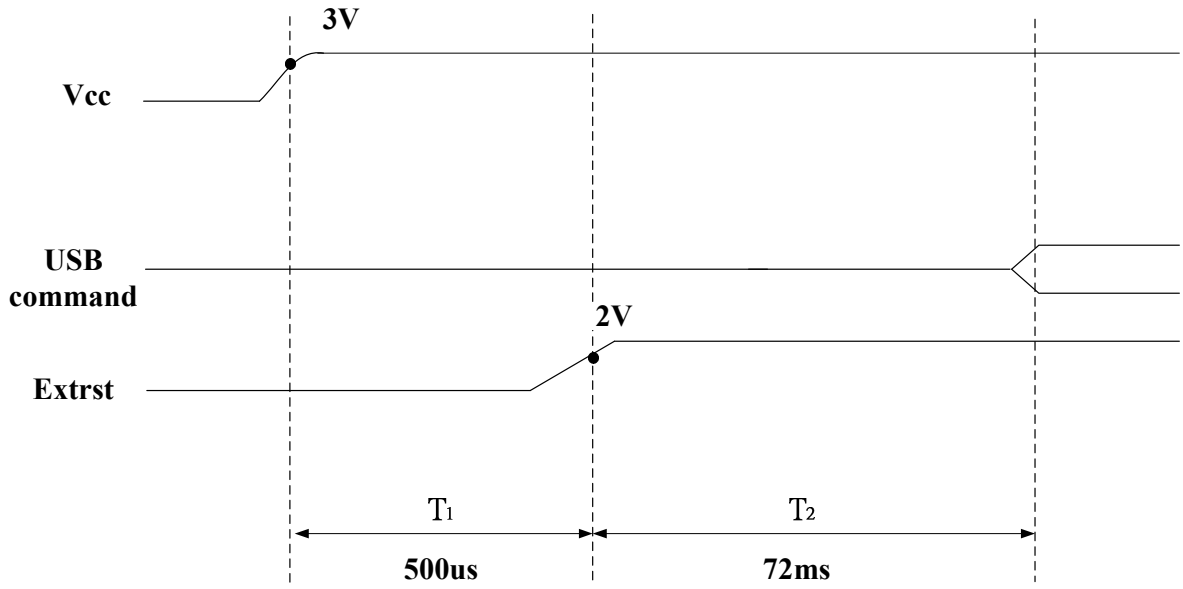


Figure 6.9 - Timing Diagram of Power Good to USB command receive ready

Parameter	Description	Min	Typ	Max	Unit
Trst	Chip reset sense timing width	2	-	-	us
T1	External reset valid from power up to high		500		us
T2	Reset deassertion to respond USB command ready	72			ms

6.6.9 EEPROM 93C46 Timing

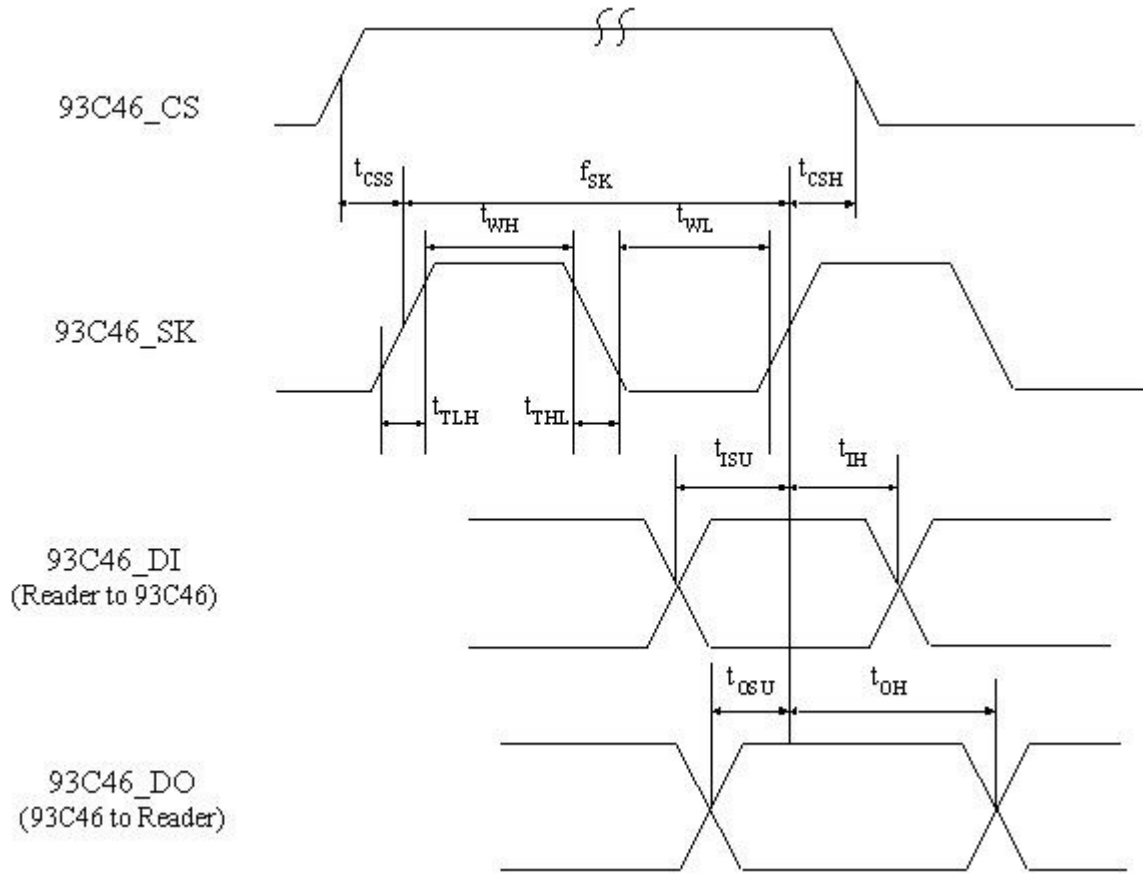


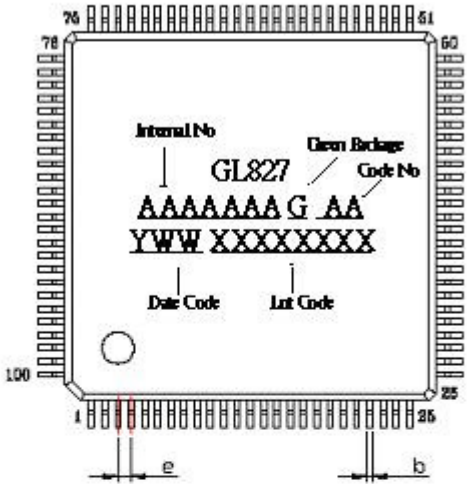
Figure 6.9 - Timing Diagram of EEPROM 93C46

AC Characteristics of 93C46 Interface (with C_{LOAD} = 15 pF)

PARAMETER	DESCRIPTION	MINIMUM	MAXIMUM	UNIT
f_{SK}	SK clock frequency	200k	400k	Hz
t_{WH}	SK H pulse length	500	–	ns
t_{WL}	SK L pulse length	500	5	ns
t_{TLH}	SK rise time	–	10	ns
t_{THL}	SK fall time	–	10	ns
t_{CSS}	CS setup time	1	–	µs
t_{CSH}	CS hold time	1	–	µs
t_{ISU}	DI setup time	1	–	µs
t_{IH}	DI hold time	1	–	µs

t_{OSU}	DO setup time	5	–	ns
t_{OH}	DO hold time	5	–	ns

CHAPTER 7 PACKAGE DIMENSION



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A			1.60 (63)
A1	0.05 (2)		0.15 (6)
A2	1.35 (53)	1.40 (55)	1.45 (57)
b	0.17 (7)	0.22 (9)	0.27 (11)
c	0.09 (4)		0.20 (8)
D	16.00 (630) BSC		
D1	14.00 (551) BSC		
E	16.00 (630) BSC		
E1	14.00 (551) BSC		
e	0.50 (20) BSC		
L	0.45 (18)	0.60 (24)	0.75 (30)
L1	1.00 (39) REF		
Y			0.10 (4)
θ	0°	3.5°	7°

NOTE: 1. REFER TO JEDEC MS-026/BED REV.B
2. ALL DIMENSIONS IN MILLIMETERS.

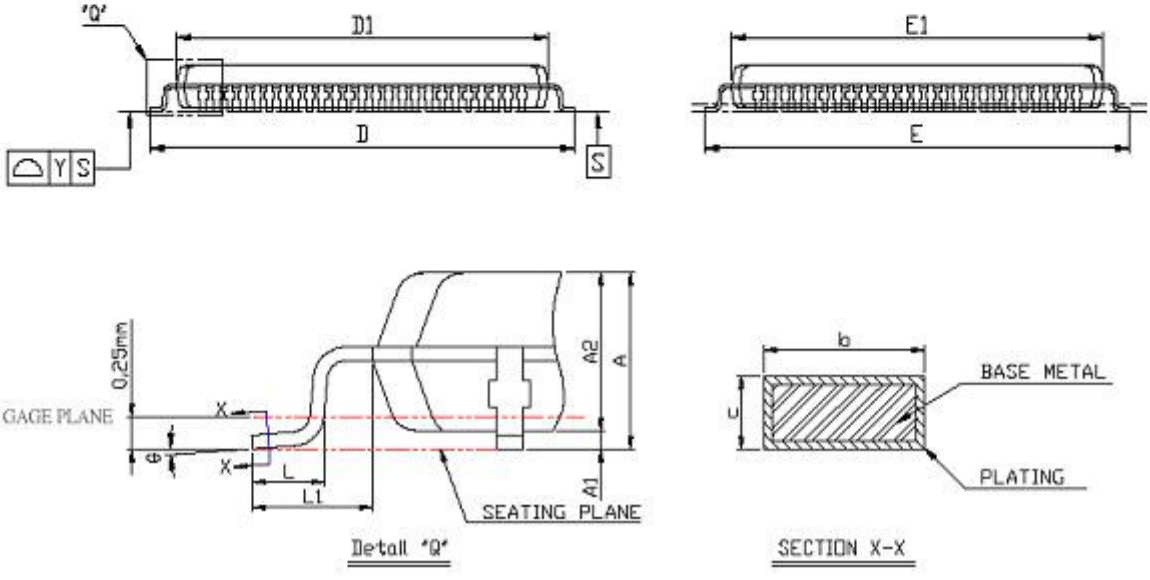
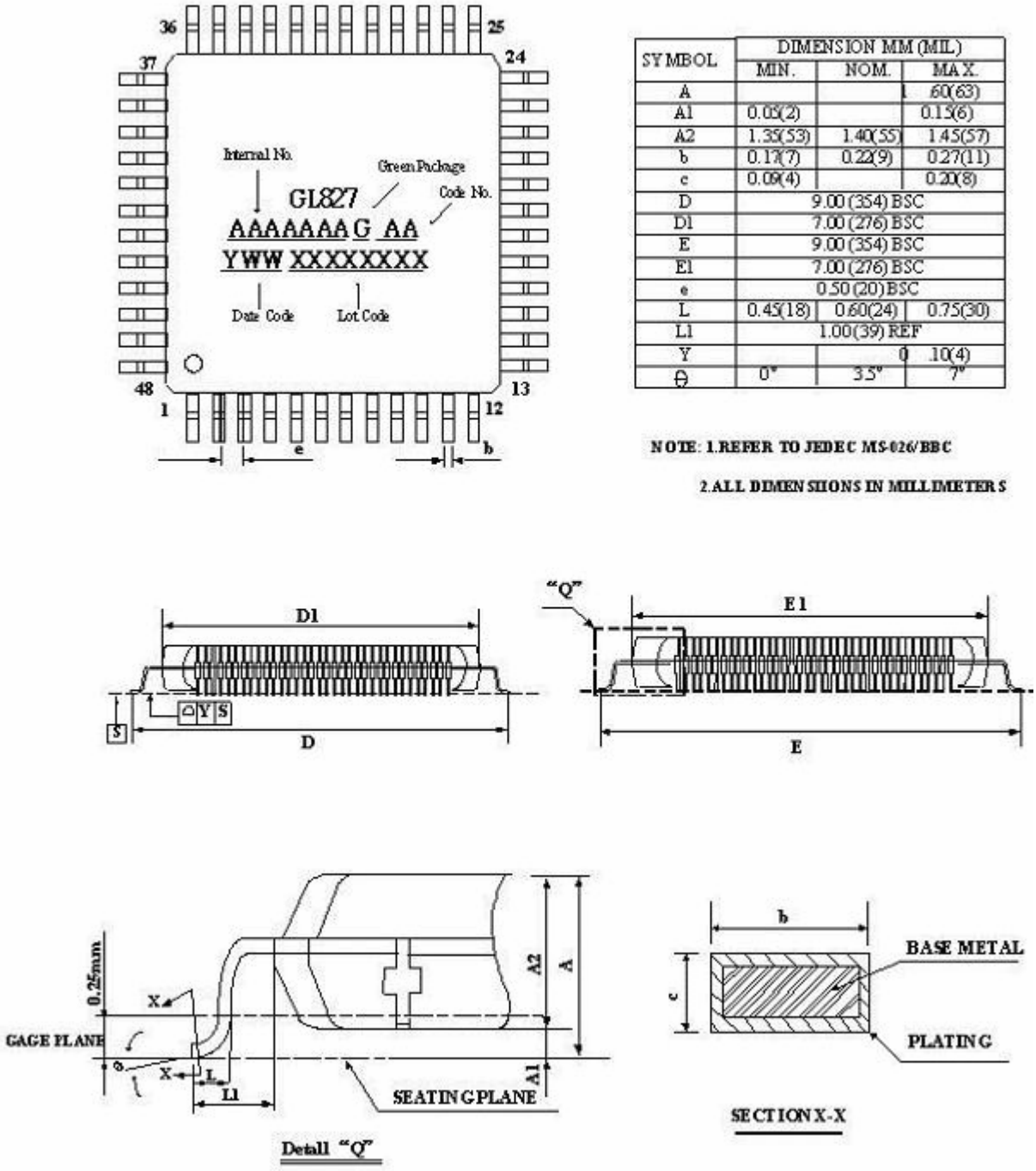


Figure 7.1 - GL827 100 Pin LQFP Package



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A			1.60(63)
A1	0.05(2)		0.15(6)
A2	1.35(53)	1.40(55)	1.45(57)
b	0.17(7)	0.22(9)	0.27(11)
c	0.09(4)		0.20(8)
D	9.00 (354) BSC		
D1	7.00 (276) BSC		
E	9.00 (354) BSC		
E1	7.00 (276) BSC		
e	0.50 (20) BSC		
L	0.45(18)	0.60(24)	0.75(30)
L1	1.00(39) REF		
Y			0.10(4)
θ	0°	3.5°	7°

Figure 7.2 - GL827 48 Pin LQFP Package

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.61 (24)	0.66 (26)	0.70 (28)
A1	0.00 (0)	0.02 (0.8)	0.05 (2)
A3		0.13 (5) REF	
b	0.18 (7)	0.25 (10)	0.30 (12)
D		7.00 (276) BSC	
E		7.00 (276) BSC	
D2	5.10 (201)	5.20 (205)	5.30 (209)
E2	5.10 (201)	5.20 (205)	5.30 (209)
e		0.50 (20) BSC	
L	0.30 (12)	0.40 (16)	0.50 (20)
y	---	0.08 (3)	---
k	0.20 (8)	---	---

NOTE: 1. ALL DIMENSIONS IN MILLIMETERS.

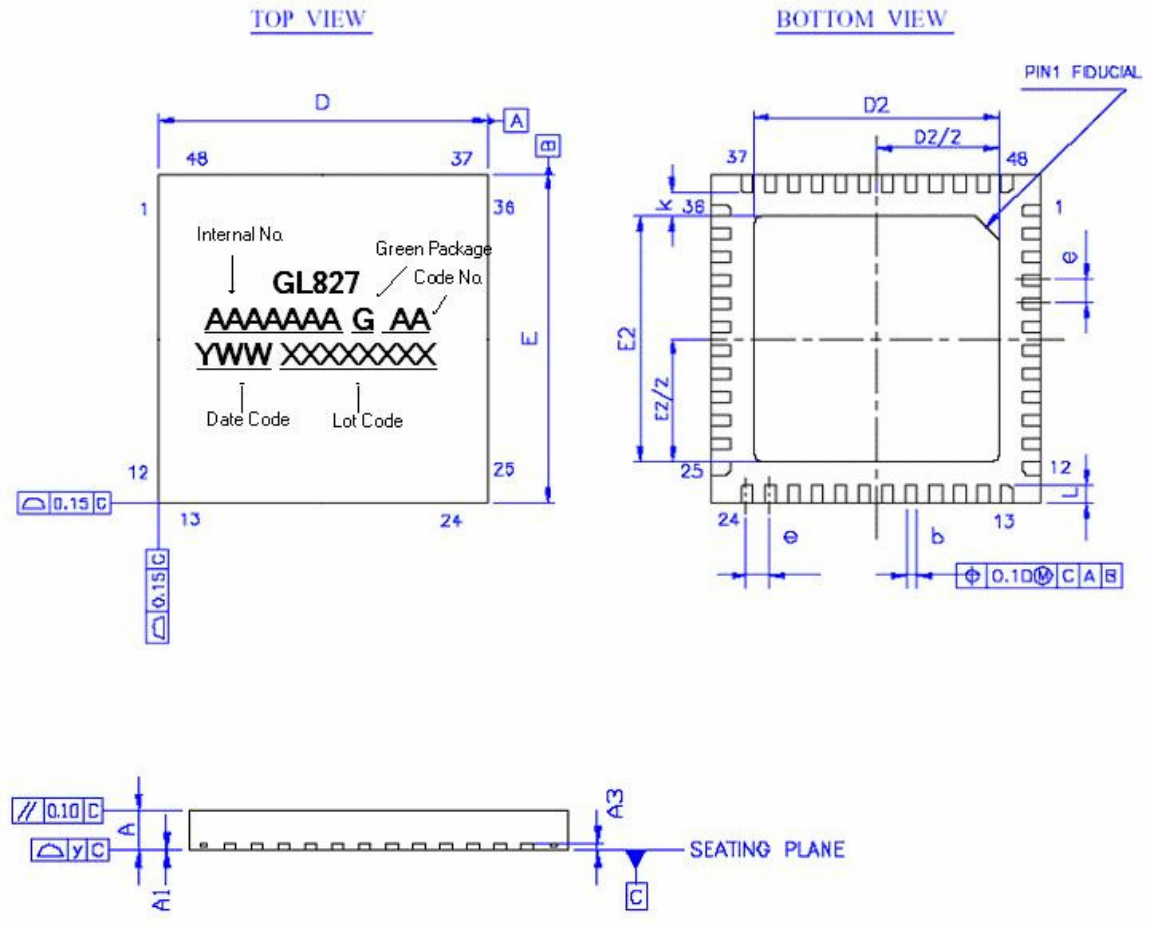


Figure 7.3 - GL827 48 Pin LQFN Package

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (28)	0.75 (30)	0.80 (32)
A1	0.00 (0)	0.02 (0.8)	0.05 (2)
A3	0.20 (8) REF		
b	0.18 (7)	0.25 (10)	0.30 (12)
D	3.90 (154)	4.00 (158)	4.10 (161)
E	3.90 (154)	4.00 (158)	4.10 (161)
D2	1.90 (75)	2.00 (79)	2.10 (83)
E2	1.90 (75)	2.00 (79)	2.10 (83)
e	0.50 (20) BSC		
L	0.30 (12)	0.40 (16)	0.50 (20)
y	0.08 (3)		

NOTE: 1. REFER TO JEDEC MO-220
2. ALL DIMENSIONS IN MILLIMETERS.

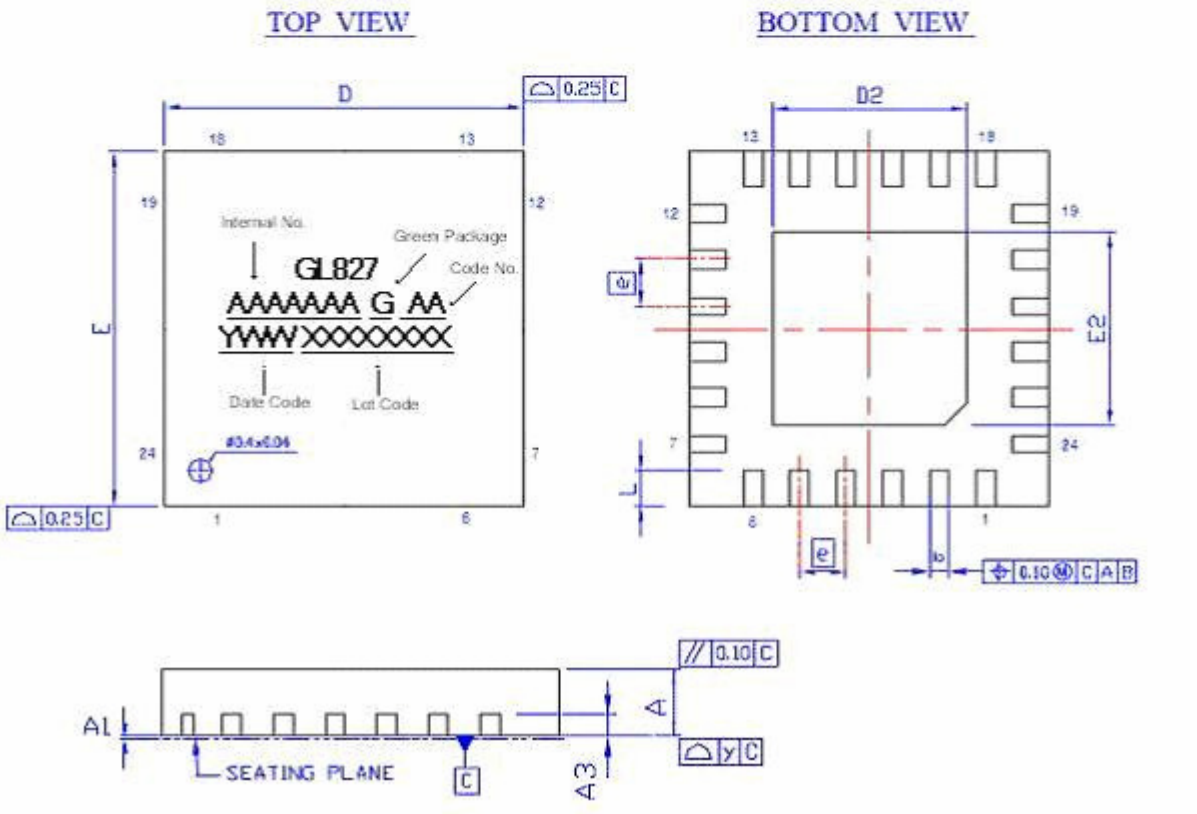


Figure 7.4 - GL827 24 Pin QFN Package

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	-	-	0.70 (28)
A1	-	-	0.25 (10)
A2	-	-	0.45 (18)
b	0.20 (8)	0.25 (10)	0.30 (12)
D	1.907 (75)	2.007 (79)	2.107 (83)
D1	0.380 (15)		
E	1.906 (75)	2.006 (79)	2.106 (83)
E1	0.380 (15)		
ZD	0.243 (9.6) REF		
ZE	0.243 (9.6) REF		

NOTE: 1. ALL DIMENSIONS IN MILLIMETERS.

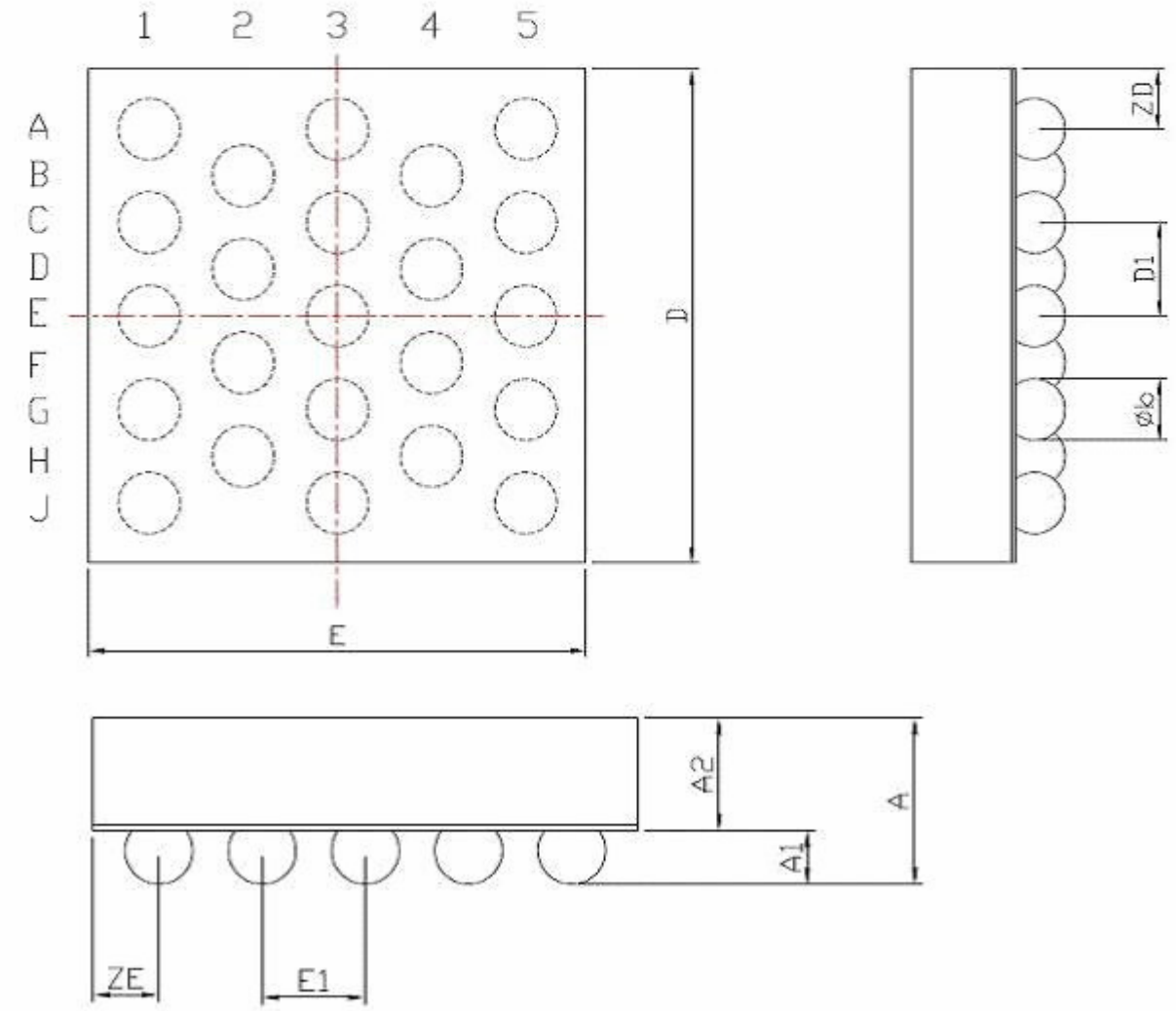
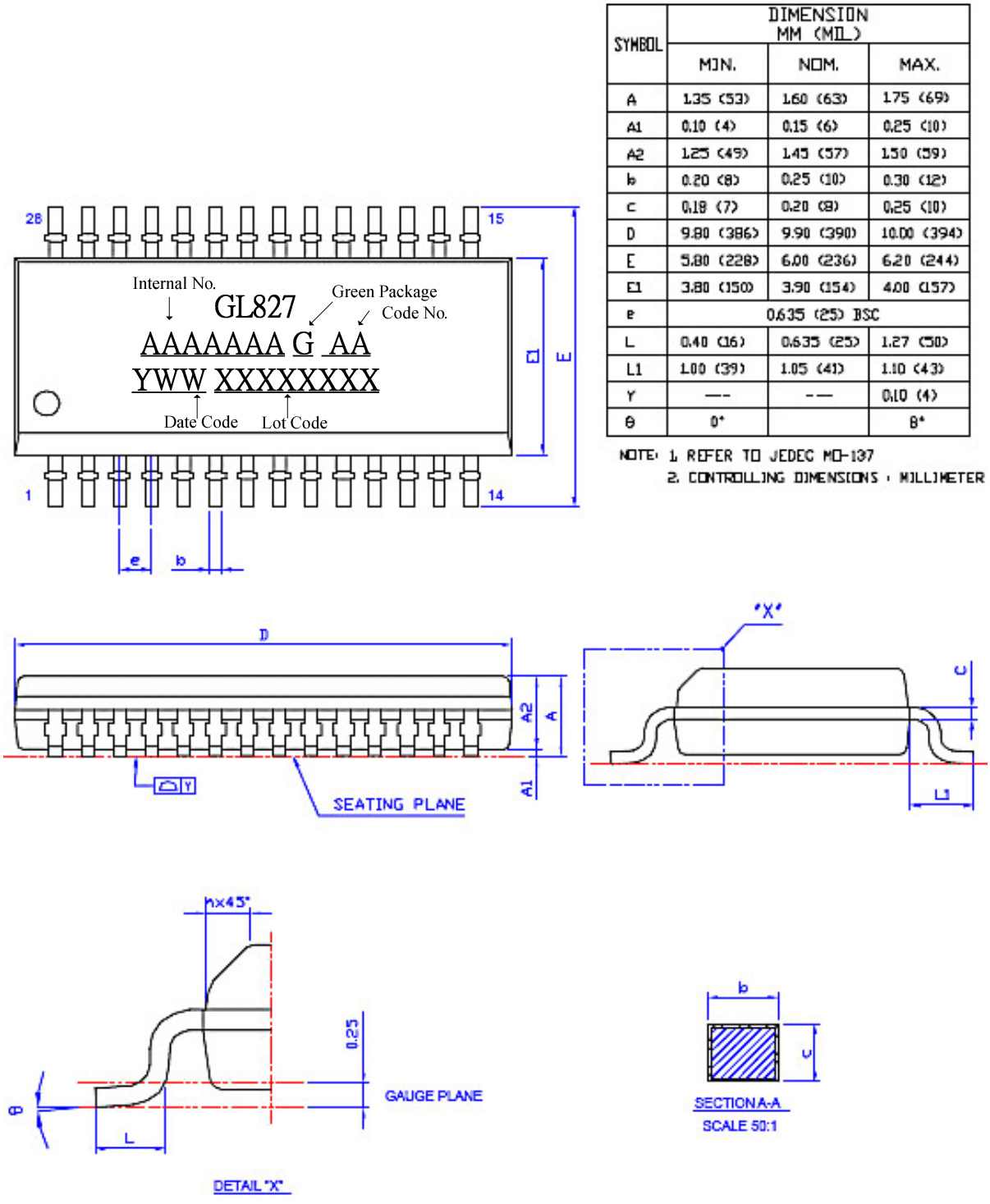


Figure 7.5 - GL827 23 Pin CSP Package



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	1.35 (53)	1.60 (63)	1.75 (69)
A1	0.10 (4)	0.15 (6)	0.25 (10)
A2	1.25 (49)	1.45 (57)	1.50 (59)
b	0.20 (8)	0.25 (10)	0.30 (12)
c	0.18 (7)	0.20 (8)	0.25 (10)
D	9.80 (386)	9.90 (390)	10.00 (394)
E	5.80 (228)	6.00 (236)	6.20 (244)
E1	3.80 (150)	3.90 (154)	4.00 (157)
e	0.635 (25) BSC		
L	0.40 (16)	0.635 (25)	1.27 (50)
L1	1.00 (39)	1.05 (41)	1.10 (43)
Y	---	---	0.10 (4)
θ	0°		8°

NOTE: 1. REFER TO JEDEC MO-137
2. CONTROLLING DIMENSIONS : MILLIMETER

Figure 7.6 - GL827 28 Pin SSOP Package

CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Normal/Green	Version	Status
GL827-MWG	100-pin LQFP	Green Package	XX	**For RD verify**
GL827-MNG	48-pin LQFP	Green Package	XX	Available
GL827-PNG	48-pin LQFN	Green Package	XX	Available
GL827-OGG	24-pin QFN	Green Package	XX	Available
GL827-HHG	28-pin SSOP	Green Package	XX	Available
	23-pin CSP	Green Package	XX	Order in Advance