

GTL2007

13-bit GTL to LVTTTL translator with power good control

Rev. 01 — 2 June 2005

Product data sheet

1. General description

The GTL2007 is a customized translator between dual Xeon processors, Platform Health Management, South Bridge and Power Supply LVTTTL and GTL signals.

The GTL2007 is derived from the GTL2006 with an enable function added that disables the error output to the monitoring agent for platforms that monitor the individual error conditions from each processor. This enable function can be used so that false error conditions are not passed to the monitoring agent when the system is unexpectedly powered down. This unexpected power-down could be from a power supply overload, a CPU thermal trip, or some other event of which the monitoring agent is unaware.

A typical implementation would be to connect each enable line to the system power good signal or the individual enables to the VRD power good for each processor.

The Nocona and Dempsey/Blackford Xeon processors specify a V_{TT} of 1.2 V and 1.1 V, as well as a nominal V_{ref} of 0.76 V and 0.73 V respectively. To allow for future voltage level changes that may extend V_{ref} to 0.63 of V_{TT} (minimum of 0.693 V with V_{TT} of 1.1 V) the GTL2009 allows a minimum V_{ref} of 0.66 V. Characterization results show that there is little DC or AC performance variation between these levels.

The GTL2007 is the companion chip to the GTL2009 3-bit GTL Front-Side Bus frequency comparator that is used in dual-processor Xeon applications.

2. Features

- Operates as a GTL to LVTTTL sampling receiver or LVTTTL to GTL driver
- 3.0 V to 3.6 V operation
- LVTTTL I/O not 5 V tolerant
- Series termination on the LVTTTL outputs of 30 Ω
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 500 mA
- Package offered: TSSOP28

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3. Quick reference data

Table 1: Quick reference data

$T_{amb} = 25^{\circ}\text{C}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	propagation delay; An-to-Bn or Bn-to-An	$C_L = 50\text{ pF}$; $V_{CC} = 3.3\text{ V}$	-	5.5	-	ns
t_{PHL}			-	5.5	-	ns
C_{io}	input/output capacitance; A-to-B	outputs disabled; V_I and $V_O = 0\text{ V}$ or 3.0 V	-	2.0	3.0	pF
	input/output capacitance; B-to-A		-	1.5	2.5	pF

4. Ordering information

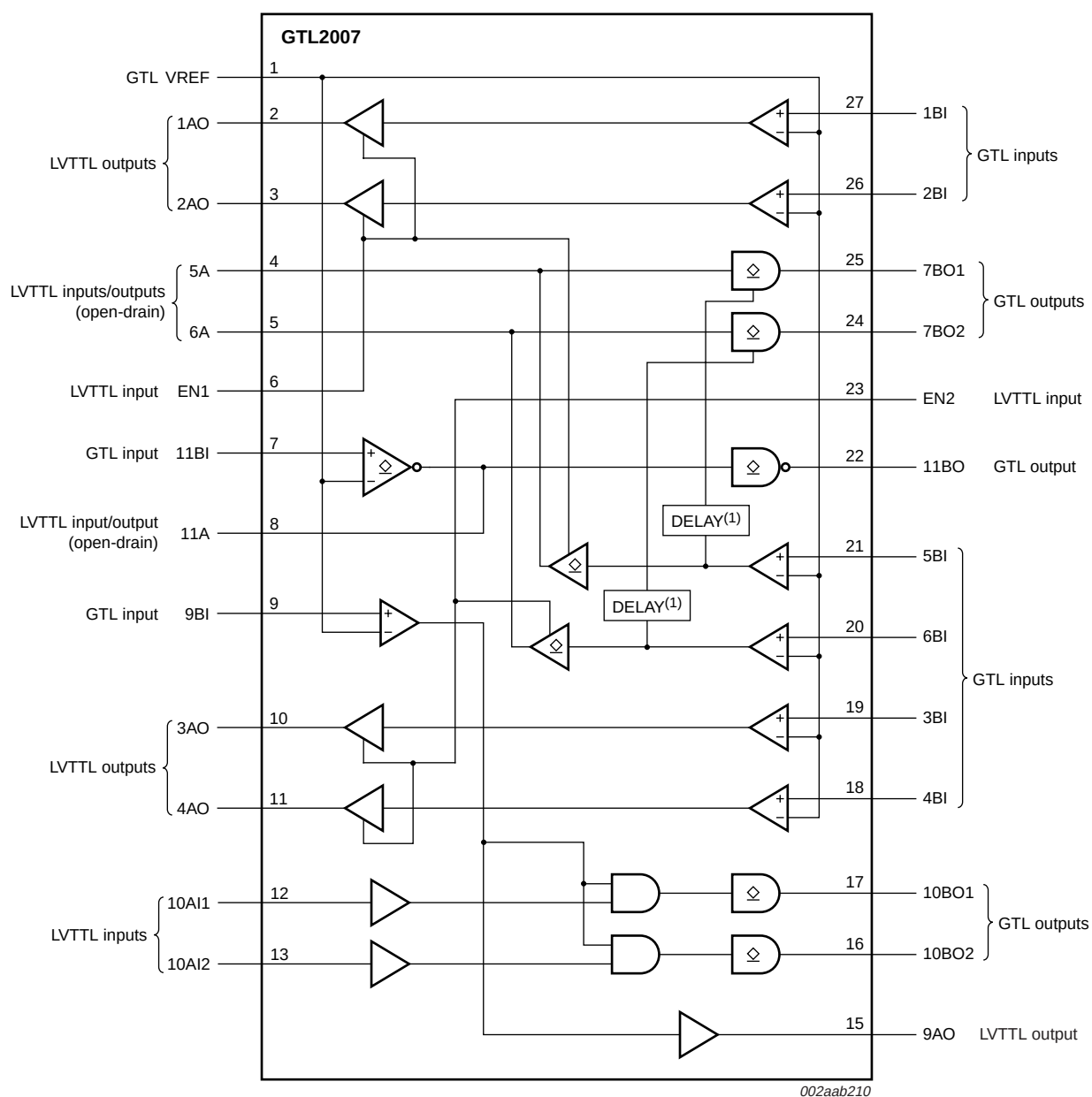
Table 2: Ordering information

$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Type number	Topside mark	Package		
		Name	Description	Version
GTL2007PW	GTL2007	TSSOP28	plastic thin shrink small outline package; 28 leads; body width 4.4 mm	SOT361-1

Standard packing quantities and other packaging data are available at
www.semiconductors.philips.com/standardics/packaging.

5. Functional diagram



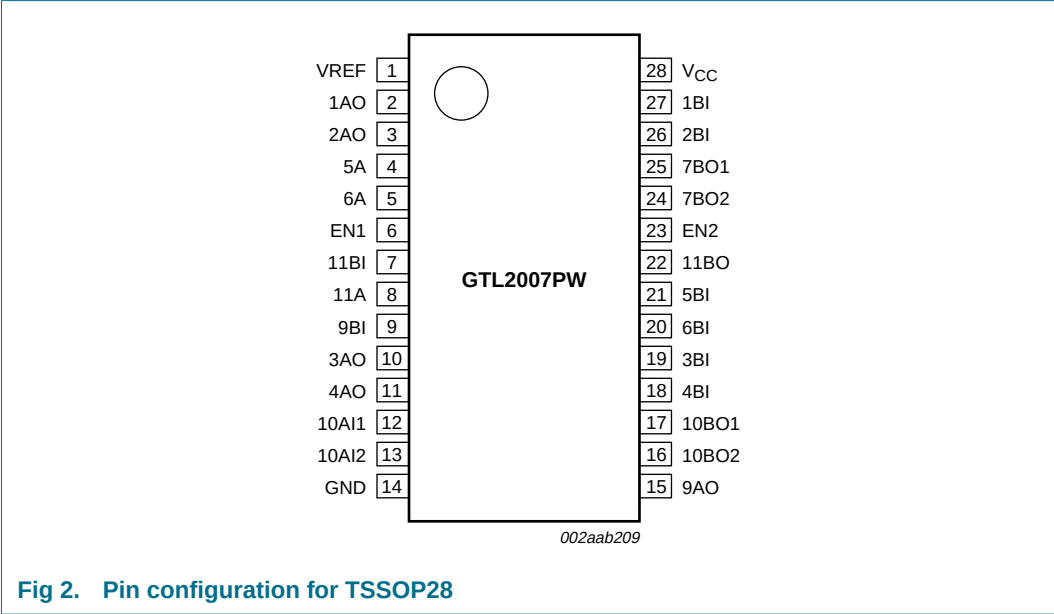
- (1) The enable on 7BO1/7BO2 include a delay that prevents the transient condition where 5BI/6BI go from LOW to HIGH, and the LOW to HIGH on 5A/6A lags up to 100 ns from causing a LOW glitch on the 7BO1/7BO2 outputs.

Fig 1. Logic diagram of GTL2007



6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
VREF	1	GTL reference voltage
1AO	2	data output (LVTTL)
2AO	3	data output (LVTTL)
5A	4	data input/output (LVTTL), open-drain
6A	5	data input/output (LVTTL), open-drain
EN1	6	enable input (LVTTL)
11BI	7	data input (GTL)
11A	8	data input/output (LVTTL), open-drain
9BI	9	data input (GTL)
3AO	10	data output (LVTTL)
4AO	11	data output (LVTTL)
10AI1	12	data input (LVTTL)
10AI2	13	data input (LVTTL)
GND	14	ground (0 V)
9AO	15	data output (LVTTL)
10BO2	16	data output (GTL)
10BO1	17	data output (GTL)
4BI	18	data input (GTL)
3BI	19	data input (GTL)

Table 3: Pin description ...continued

Symbol	Pin	Description
6BI	20	data input (GTL)
5BI	21	data input (GTL)
11BO	22	data output (GTL)
EN2	23	enable input (LVTTL)
7BO2	24	data output (GTL)
7BO1	25	data output (GTL)
2BI	26	data input (GTL)
1BI	27	data input (GTL)
V _{CC}	28	positive supply voltage

7. Functional description

Refer to [Figure 1 “Logic diagram of GTL2007” on page 3.](#)

7.1 Function tables

Table 4: GTL input signals

H = HIGH voltage level; L = LOW voltage level.

Input	Output ^[1]
1BI/2BI/3BI/4BI/9BI	1AO/2AO/3AO/4AO/9AO
L	L
H	H

[1] 1AO, 2AO, 3AO, 4AO and 5A/6A condition changed by ENn power good signal as described in [Table 5](#) and [Table 6](#).

Table 5: EN1 power good signal

H = HIGH voltage level; L = LOW voltage level.

EN1	1AO and 2AO	5A
L	H	5BI disconnected
H	follows BI	5BI connected

Table 6: EN2 power good signal

H = HIGH voltage level; L = LOW voltage level.

EN2	3AO and 4AO	6A
L	H	6BI disconnected
H	follows BI	6BI connected

Table 7: SMI signals*H = HIGH voltage level; L = LOW voltage level.*

Input	Input	Output
10AI1/10AI2	9BI	10BO1/10BO2
L	L	L
L	H	L
H	L	L
H	H	H

Table 8: PROCHOT signals*H = HIGH voltage level; L = LOW voltage level.*

Input	Input/output	Output
5BI/6BI	5A/6A (open-drain)	7BO1/7BO2
L	L	H [1]
H	L [2]	L
H	H	H

[1] The enable on 7BO1/7BO2 includes a delay that prevents the transient condition where 5BI/6BI go from LOW to HIGH, and the LOW to HIGH on 5A/6A lags up to 100 ns from causing a low glitch on the 7BO1/7BO2 outputs.

[2] Open-drain input/output terminal is driven to logic LOW state by other driver.

Table 9: NMI signals*H = HIGH voltage level; L = LOW voltage level.*

Input	Input/output	Output
11BI	11A (open-drain)	11BO
L	H	L
L	L [1]	H
H	L	H

[1] Open-drain input/output terminal is driven to logic LOW state by other driver.

8. Application design-in information

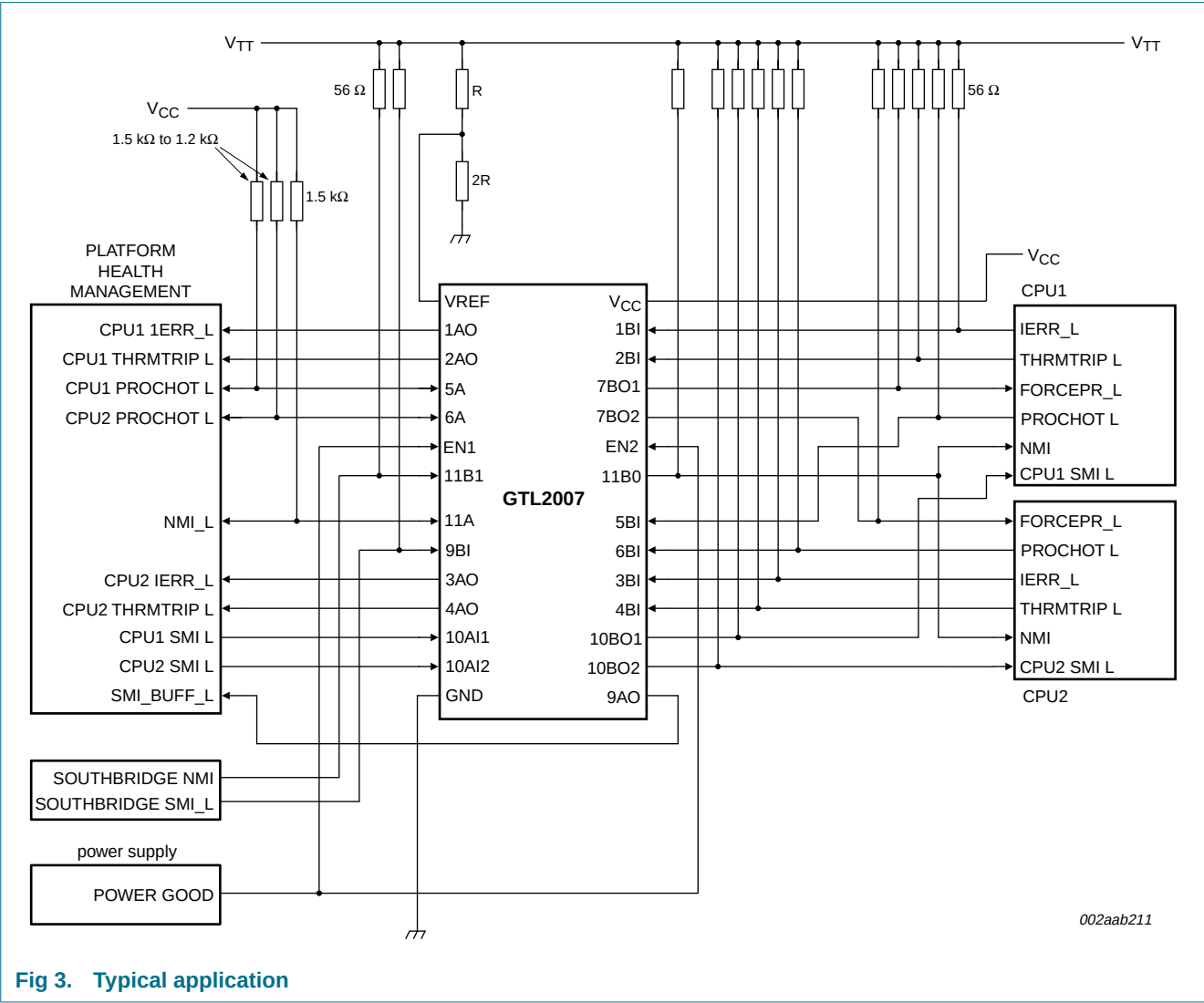


Fig 3. Typical application

9. Limiting values

Table 10: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). [\[1\]](#)

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	DC supply voltage		-0.5	+4.6	V
I_{IK}	input clamping diode current	$V_I < 0$ V	-	-50	mA
V_I	DC input voltage	A port (LVTTTL)	-0.5 [3]	+4.6	V
		B port (GTL)	-0.5 [3]	+4.6	V
I_{OK}	output diode clamping current	$V_O < 0$ V	-	-50	mA
V_O	DC output voltage	output in OFF or HIGH state; A port	-0.5 [3]	+4.6	V
		output in OFF or HIGH state; B port	-0.5 [3]	+4.6	V
I_{OL}	current into any output in the LOW state	A port	-	32	mA
		B port	-	30	mA
I_{OH}	current into any output in the HIGH state	A port	-	-32	mA
T_{stg}	storage temperature		-60	+150	°C
$T_{j(max)}$	maximum junction temperature		[2] -	+125	°C

- [1] Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under [Section 10 "Recommended operating conditions"](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- [2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
- [3] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

10. Recommended operating conditions

Table 11: Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		3.0	3.3	3.6	V
V_{TT}	termination voltage	GTL	-	1.2	-	V
V_{ref}	reference voltage	GTL	0.64	0.8	1.1	V
V_I	input voltage	A port	0	3.3	3.6	V
		B port	0	V_{TT}	3.6	V
V_{IH}	HIGH-level input voltage	A port and ENn	2	-	-	V
		B port	$V_{ref} + 0.050$	-	-	V
V_{IL}	LOW-level input voltage	A port and ENn	-	-	0.8	V
		B port	-	-	$V_{ref} - 0.050$	V
I_{OH}	HIGH-level output current	A port	-	-	-16	mA
I_{OL}	LOW-level output current	A port	-	-	16	mA
		B port	-	-	15	mA
T_{amb}	ambient temperature	operating in free-air	-40	-	+85	°C

11. Static characteristics

Table 12: Static characteristics

Recommended operating conditions; voltages are referenced to GND (ground = 0 V). $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
V_{OH}	HIGH-level output voltage	A port; $V_{CC} = 3.0\text{ V}$ to 3.6 V ; $I_{OH} = -100\text{ }\mu\text{A}$	^[2] $V_{CC} - 0.2$	3.0	-	V
		A port; $V_{CC} = 3.0\text{ V}$; $I_{OH} = -16\text{ mA}$	^[2] 2.1	2.3	-	V
V_{OL}	LOW-level output voltage	A port; $V_{CC} = 3.0\text{ V}$; $I_{OL} = 4\text{ mA}$	^[2] -	0.15	0.4	V
		A port; $V_{CC} = 3.0\text{ V}$; $I_{OL} = 8\text{ mA}$	^[2] -	0.3	0.55	V
		A port; $V_{CC} = 3.0\text{ V}$; $I_{OL} = 16\text{ mA}$	^[2] -	0.6	0.8	V
		B port; $V_{CC} = 3.0\text{ V}$; $I_{OL} = 15\text{ mA}$	^[2] -	0.13	0.4	V
I_I	input current	A port; $V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$	-	-	± 1	μA
		A port; $V_{CC} = 3.6\text{ V}$; $V_I = 0\text{ V}$	-	-	± 1	μA
		B port; $V_{CC} = 3.6\text{ V}$; $V_I = V_{TT}$ or GND	-	-	± 1	μA
I_{CC}	supply current	A or B port; $V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$ or GND; $I_O = 0\text{ mA}$	-	8	12	mA
ΔI_{CC} ^[3]	additional quiescent current (per input)	A port or control inputs; $V_{CC} = 3.6\text{ V}$; $V_I = V_{CC} - 0.6\text{ V}$	-	-	500	μA
C_{io}	input/output capacitance	A port; $V_O = 3.0\text{ V}$ or 0 V	-	2.5	3.5	pF
		B port; $V_O = V_{TT}$ or 0 V	-	1.5	2.5	pF

[1] All typical values are measured at $V_{CC} = 3.3\text{ V}$ and $T_{amb} = 25^{\circ}\text{C}$.

[2] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[3] This is the increase in supply current for each input that is at the specified LVTTTL voltage level rather than V_{CC} or GND.

12. Dynamic characteristics

Table 13: Dynamic characteristics

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
$V_{ref} = 0.73\text{ V}; V_{TT} = 1.1\text{ V}$						
t_{PLH}	propagation delay, An to Bn	see Figure 4	1	4	8	ns
t_{PHL}			2	5.5	10	ns
t_{PLH}	propagation delay, nBI to nAO	see Figure 5	2	5.5	10	ns
t_{PHL}			2	5.5	10	ns
t_{PLH}	propagation delay, 9BI to 10BOn		2	6	11	ns
t_{PHL}			2	6	11	ns
t_{PLH}	propagation delay, 11BI to 11BO		2	8	13	ns
t_{PHL} ^[2]			2	14	21	ns
t_{PLZ}	disable time from LOW level, nBI to nA (I/O)	see Figure 6	2	13	18	ns
t_{PZL}	enable time to LOW level, nBI to nA (I/O)		2	12	16	ns
t_{PLH}	propagation delay, 5BI to 7BO1 or 6BI to 7BO2	see Figure 7	4	7	12	ns
t_{PHL}			100	205	350	ns
t_{PLH}	propagation delay, EN1 to nAO or EN2 to nAO	see Figure 8	2	6.5	10	ns
t_{PHL}			2	6.5	10	ns
t_{PLZ}	disable time from LOW level, EN1 to 5A (I/O) or EN2 to 6A (I/O)	see Figure 9	1	3	7	ns
t_{PZL}	enable time to LOW level, EN1 to 5A (I/O) or EN2 to 6A (I/O)		2	7	10	ns
$V_{ref} = 0.76\text{ V}; V_{TT} = 1.2\text{ V}$						
t_{PLH}	propagation delay, An to Bn	see Figure 4	1	4	8	ns
t_{PHL}			2	5.5	10	ns
t_{PLH}	propagation delay, nBI to nAO	see Figure 5	2	5.5	10	ns
t_{PHL}			2	5.5	10	ns
t_{PLH}	propagation delay, 9BI to 10BOn		2	6	11	ns
t_{PHL}			2	6	11	ns
t_{PLH}	propagation delay, 11BI to 11BO		2	8	13	ns
t_{PHL} ^[2]			2	14	21	ns
t_{PLZ}	disable time from LOW level, nBI to nA (I/O)	see Figure 6	2	13	18	ns
t_{PZL}	enable time to LOW level, nBI to nA (I/O)		2	12	16	ns
t_{PLH}	propagation delay, 5BI to 7BO1 or 6BI to 7BO2	see Figure 7	4	7	12	ns
t_{PHL}			100	205	350	ns

Table 13: Dynamic characteristics ...continued
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
t_{PLH}	propagation delay, EN1 to nAO or EN2 to nAO	see Figure 8	2	6.5	10	ns
t_{PHL}			2	6.5	10	ns
t_{PLZ}	disable time from LOW level, EN1 to 5A (I/O) or EN2 to 6A (I/O)	see Figure 9	1	3	7	ns
t_{PZL}	enable time to LOW level, EN1 to 5A (I/O) or EN2 to 6A (I/O)		2	7	10	ns

- [1] All typical values are at $V_{CC} = 3.3\text{ V}$ and $T_{amb} = 25\text{ }^{\circ}\text{C}$.
[2] Includes $\sim 7.6\text{ ns}$ RC rise time of test load pull-up on 11A, $1.5\text{ k}\Omega$ pull-up and 21 pF load on 11A has about 23 ns RC rise time.

12.1 Waveforms

$V_M = 1.5\text{ V}$ at $V_{CC} \geq 3.0\text{ V}$ for A ports; $V_M = V_{ref}$ for B ports.

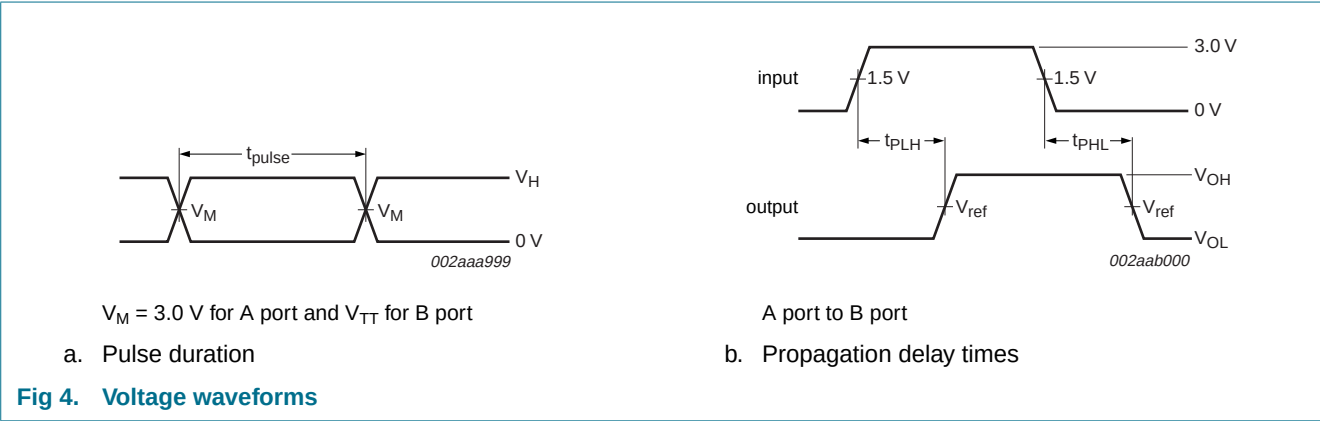
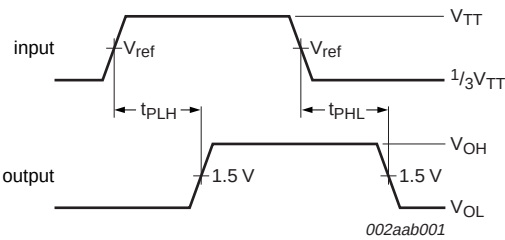


Fig 4. Voltage waveforms



PRR $\leq$ 10 MHz; $Z_O = 50 \Omega$; $t_r \leq 2.5$ ns; $t_f \leq 2.5$ ns

Fig 5. Propagation delay, nBI to nAO

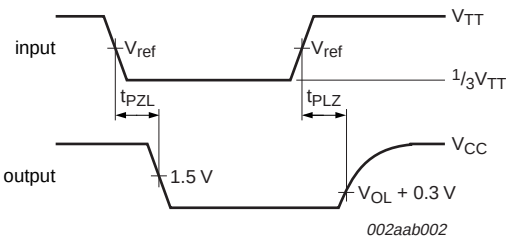


Fig 6. nBI to nA (I/O)

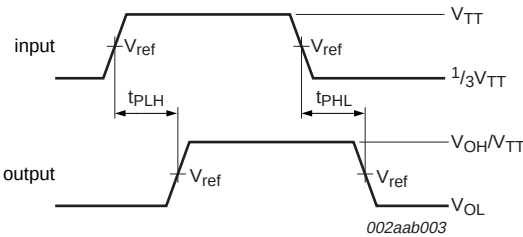


Fig 7. 5BI to 7BO or 6BI to 7BO2

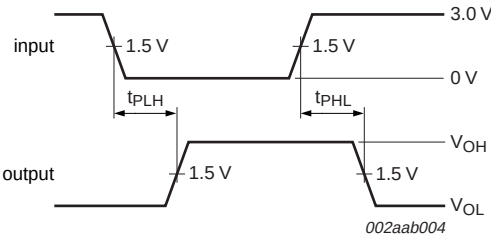


Fig 8. EN1 to nAO or EN2 to nAO

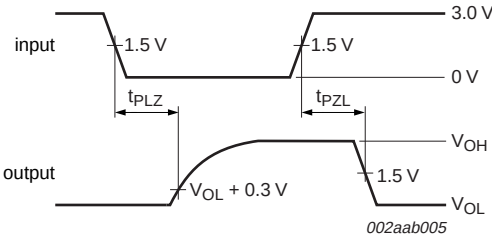


Fig 9. EN1 to 5A (I/O) or EN2 to 6A (I/O)

13. Test information

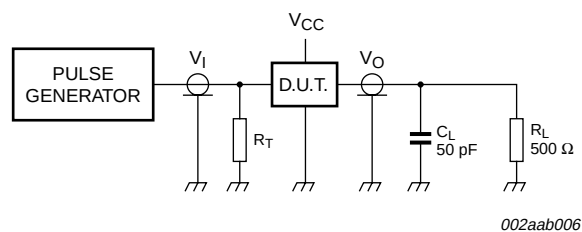


Fig 10. Load circuit for A outputs

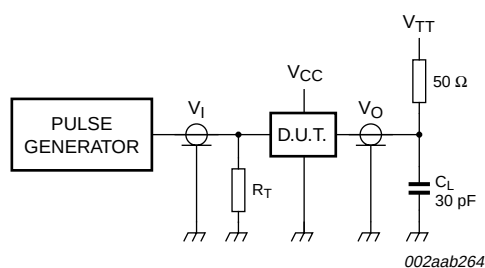


Fig 11. Load circuit for B outputs

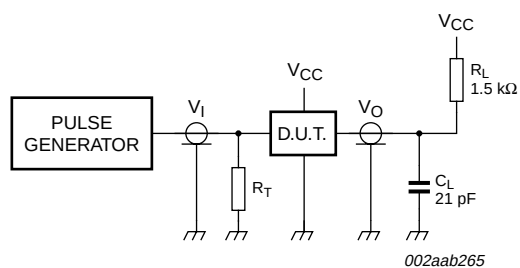


Fig 12. Load circuit for open-drain LVTTTL I/O

R_L — Load resistor

C_L — Load capacitance; includes jig and probe capacitance

R_T — Termination resistance; should be equal to Z_{OUT} of pulse generators.

14. Package outline

TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm

SOT361-1

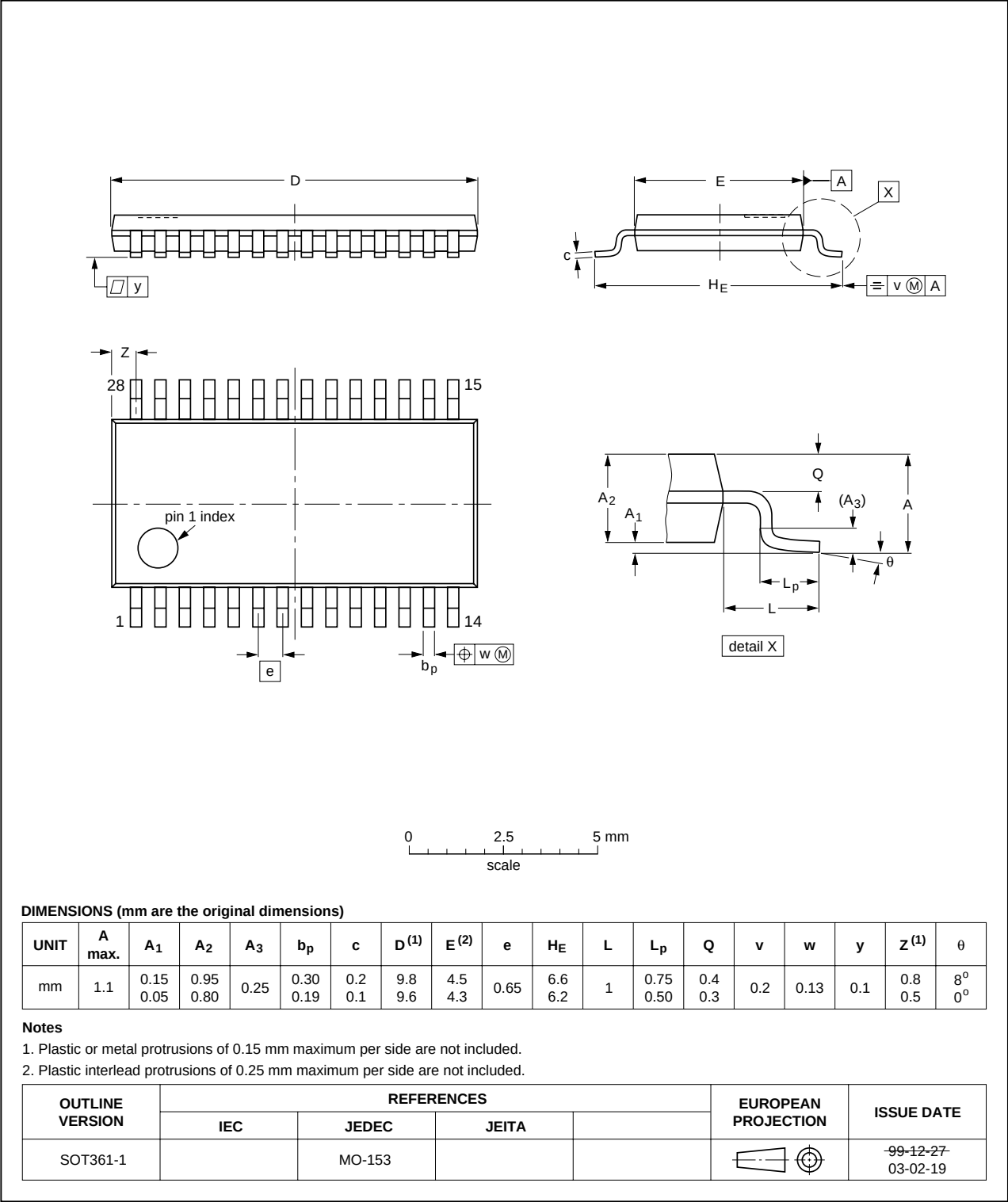


Fig 13. Package outline SOT361-1 (TSSOP28)

15. Soldering

15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
 - for all BGA, HTSSON..T and SSOP..T packages
 - for packages with a thickness ≥ 2.5 mm
 - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm³ so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm³ so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

- smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

15.5 Package related soldering information

Table 14: Suitability of surface mount IC packages for wave and reflow soldering methods

Package ^[1]	Soldering method	
	Wave	Reflow ^[2]
BGA, HTSSON..T ^[3] , LBGA, LFBGA, SQFP, SSOP..T ^[3] , TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable ^[4]	suitable
PLCC ^[5] , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ^{[5] [6]}	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended ^[7]	suitable
CWQCCN..L ^[8] , PMFP ^[9] , WQCCN..L ^[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

- [4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- [5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- [6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- [7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
- [8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
- [9] Hot bar soldering or manual soldering is suitable for PMFP packages.

16. Abbreviations

Table 15: Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Silicon
CPU	Central Processing Unit
ESD	Electrostatic Discharge
GTL	Gunning Transceiver Logic
HBM	Human Body Model
LVTTTL	Low Voltage Transistor-Transistor Logic
MM	Machine Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic
VRD	Voltage Regulator Down

17. Revision history

Table 16: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
GTL2007_1	20050602	Product data sheet	-	9397 750 13264	-

18. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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