



STGY50NC60WD

N-channel 600V - 50A - Max247
Very fast PowerMESH™ IGBT

PRELIMINARY DATA

General features

Type	V _{CES}	V _{CE(sat)} (max)@25°C	I _C @100°C
STGY50NC60WD	600V	< 2.5V	50A

- High frequency operation
- Low C_{RES} / C_{IES} ratio (no cross-conduction susceptibility)
- Very soft ultra fast recovery antiparallel diode

Description

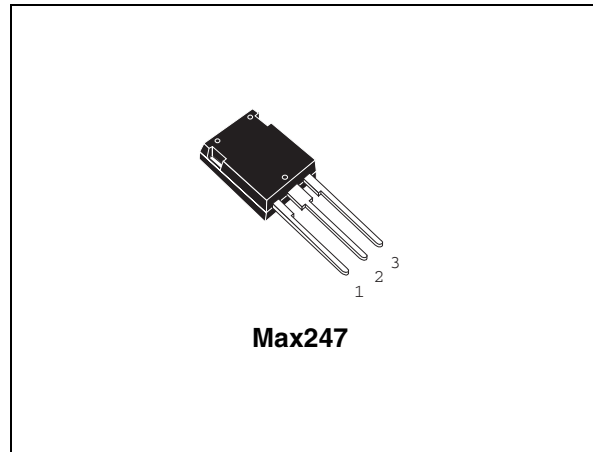
Using the latest high voltage technology based on a patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, the PowerMESH™ IGBTs, with outstanding performances. The suffix "W" identifies a family optimized for very high frequency application.

Applications

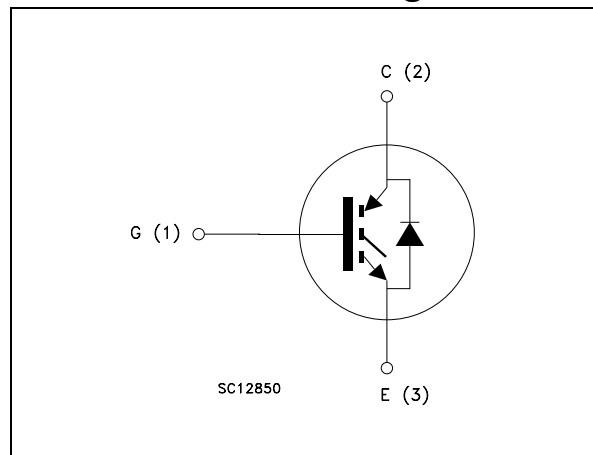
- High frequency inverters
- SMPS and PFC in both hard switch and resonant topologies
- Motor drivers, UPS

Order codes

Part number	Marking	Package	Packaging
STGY50NC60WD	GY50NC60WD	Max247	Tube



Internal schematic diagram



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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage ($V_{GS} = 0$)	600	V
$I_C^{(1)}$	Collector current (continuous) at $T_C = 25^\circ\text{C}$	80	A
$I_C^{(1)}$	Collector current (continuous) at $T_C = 100^\circ\text{C}$	50	A
$I_{CM}^{(2)}$	Collector current (pulsed)	190	A
I_F	Diode RMS forward current at $T_C = 25^\circ\text{C}$	30	A
V_{GE}	Gate-emitter voltage	± 20	V
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	260	W
T_{stg}	Storage temperature	– 55 to 150	$^\circ\text{C}$
T_j	Operating junction temperature		

1. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{JMAX} - T_C}{R_{THJ-C} \times V_{CESAT(MAX)}(T_C, I_C)}$$

2. Pulse width limited by max junction temperature

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max IGBT	0.48	$^\circ\text{C/W}$
$R_{thj-case}$	Thermal resistance junction-case max diode	1.5	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	$^\circ\text{C/W}$
$T_L^{(1)}$	Maximum lead temperature for soldeing purpose	300	$^\circ\text{C}$

1. 1.6mm from case, for 10sec

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	$I_C = 1\text{mA}$, $V_{GE} = 0$	600			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE} = 15\text{V}$, $I_C = 40\text{A}$ $V_{GE} = 15\text{V}$, $I_C = 40\text{A}$, $T_C = 125^{\circ}\text{C}$		1.9 1.7	2.5	V V
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}$, $I_C = 250\mu\text{A}$	3.75		5.75	V
I_{CES}	Collector cut-off current ($V_{GE} = 0$)	$V_{GE} = \text{Max rating}$, $T_C = 25^{\circ}\text{C}$ $V_{GE} = \text{Max rating}$, $T_C = 125^{\circ}\text{C}$			250 1	μA mA
I_{GES}	Gate-emitter leakage current ($V_{CE} = 0$)	$V_{GE} = \pm 20\text{V}$, $V_{CE} = 0$			± 100	nA
g_{fs}	Forward transconductance	$V_{CE} = 15\text{V}$, $I_C = 20\text{A}$		20		S

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies}	Input capacitance	$V_{CE} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GE} = 0$		4700		pF
C_{oes}	Output capacitance			410		pF
C_{res}	Reverse transfer capacitance			90		pF
Q_g	Total gate charge	$V_{CE} = 390\text{V}$, $I_C = 40\text{A}$, $V_{GE} = 15\text{V}$, Figure 2		155		nC
Q_{ge}	Gate-emitter charge			32.4		nC
Q_{gc}	Gate-collector charge			82.2		nC

Table 5. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	$V_{CC} = 390V$, $I_C = 40A$ $R_G = 10\Omega$, $V_{GE} = 15V$, <i>Figure 3</i>		52 17 2400		ns ns A/ μs
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	$V_{CC} = 390V$, $I_C = 40A$ $R_G = 10\Omega$, $V_{GE} = 15V$, $T_j = 125^\circ C$ <i>Figure 3</i>		50 19 2000		ns ns A/ μs
$t_{r(Voff)}$ $t_{d(Voff)}$ t_f	Off voltage rise time Turn-off delay time Current fall time	$V_{CC} = 390V$, $I_C = 40A$ $R_G = 10\Omega$, $V_{GE} = 15V$, <i>Figure 3</i>		31 240 35		ns ns ns
$t_{r(Voff)}$ $t_{d(Voff)}$ t_f	Off voltage rise time Turn-off delay time Current fall time	$V_{CC} = 390V$, $I_C = 40A$ $R_G = 10\Omega$, $V_{GE} = 15V$, $T_j = 125^\circ C$ <i>Figure 3</i>		60 280 63		ns ns ns

Table 6. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$E_{on}^{(1)}$ $E_{off}^{(2)}$ E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	$V_{CC} = 390V$, $I_C = 40A$ $R_G = 10\Omega$, $V_{GE} = 15V$, <i>Figure 1</i>		365 560 925	470 790 1260	μJ μJ μJ
$E_{on}^{(1)}$ $E_{off}^{(2)}$ E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	$V_{CC} = 390V$, $I_C = 40A$ $R_G = 10\Omega$, $V_{GE} = 15V$, $T_j = 125^\circ C$ <i>Figure 1</i>		635 910 1545		μJ μJ μJ

1. E_{on} is the turn-on losses when a typical diode is used in the test circuit in *Figure 4*. If the IGBT is offered in a package with a co-pak diode, the co-pak diode is used as external diode. IGBTs & Diode are at the same temperature ($25^\circ C$ and $125^\circ C$)
2. Turn-off losses include also the tail of the collector current

Table 7. Collector-emitter diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_f	Forward on-voltage	$I_f = 20A$ $I_f = 20A, T_j = 125^\circ C$		1.5 1	2.2	V V
t_{rr}	Reverse recovery time	$I_f = 20A, V_R = 40V,$ $T_j = 25^\circ C, di/dt = 100 A/\mu s$		44		ns
Q_{rr}	Reverse recovery charge	$T_j = 25^\circ C, di/dt = 100 A/\mu s$		66		nC
I_{rrm}	Reverse recovery current	Figure 4		3		A
t_{rr}	Reverse recovery time	$I_f = 12A, V_R = 40V,$ $T_j = 125^\circ C, di/dt = 100A/\mu s$		88		ns
Q_{rr}	Reverse recovery charge	$T_j = 125^\circ C, di/dt = 100A/\mu s$		237		nC
I_{rrm}	Reverse recovery current	Figure 4		5.4		A

3 Test circuit

Figure 1. Test circuit for inductive load switching

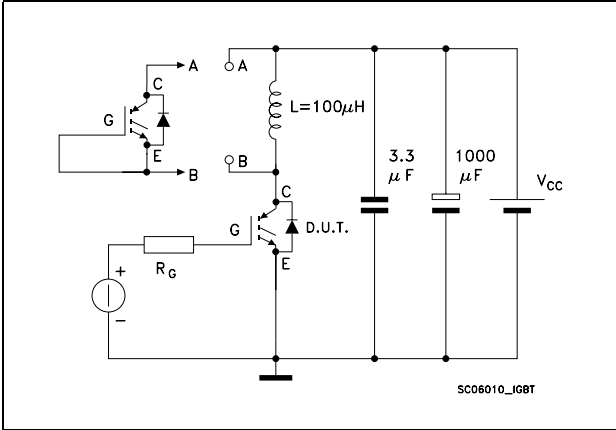


Figure 2. Gate charge test circuit

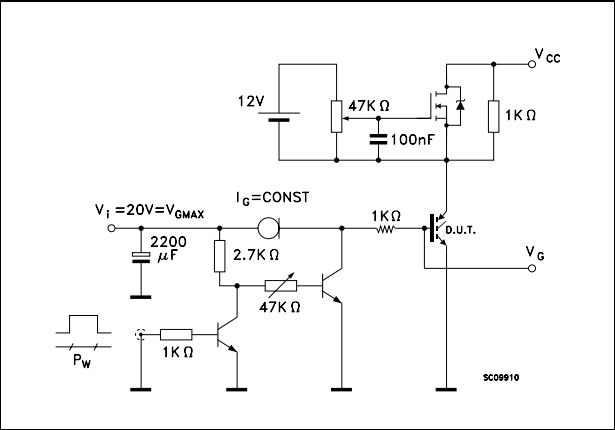


Figure 3. Switching waveform

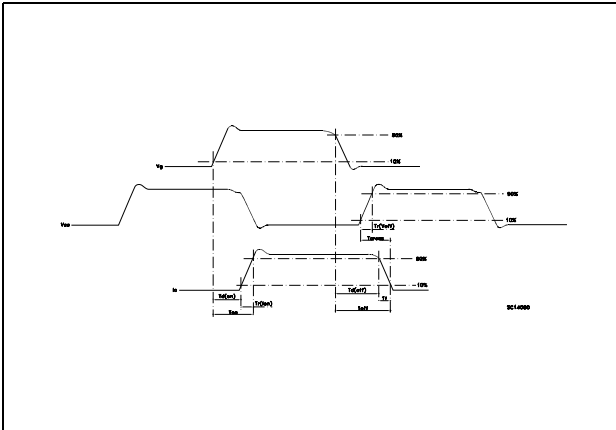
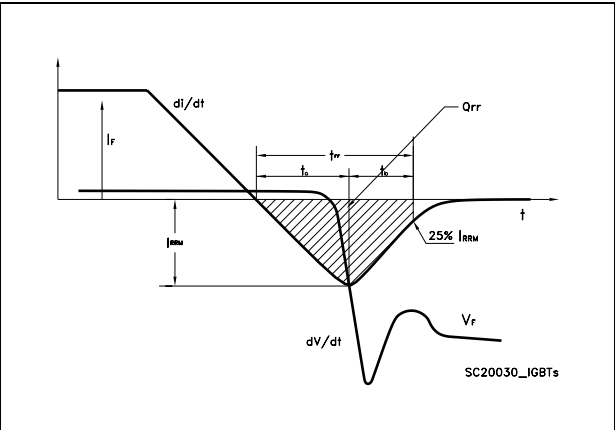


Figure 4. Diode recovery time waveform

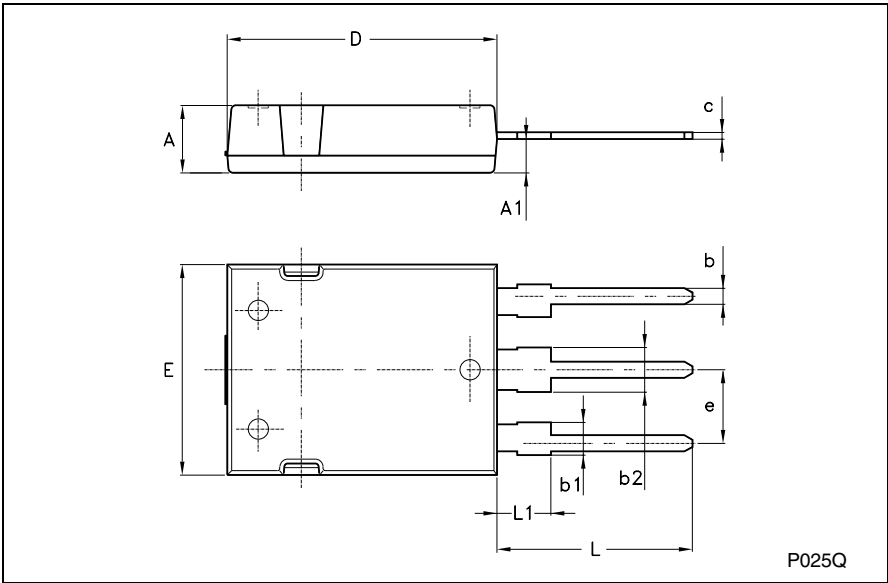


4 **Package mechanical data**

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Max247 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.70		5.30			
A1	2.20		2.60			
b	1.00		1.40			
b1	2.00		2.40			
b2	3.00		3.40			
c	0.40		0.80			
D	19.70		20.30			
e	5.35		5.55			
E	15.30		15.90			
L	14.20		15.20			
L1	3.70		4.30			



5 Revision history

Table 8. Revision history

Date	Revision	Changes
09-Oct-2006	1	Initial release.

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