

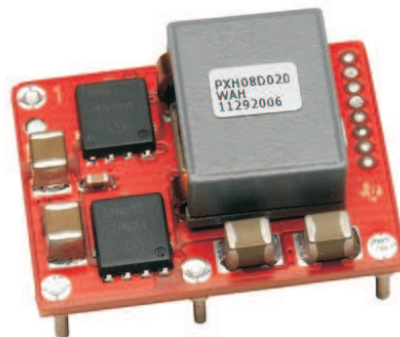
20-A, 4.75-V to 14-V INPUT, NON-ISOLATED, WIDE-OUTPUT, DIGITAL POWERTRAIN™ MODULE

FEATURES

- Up to 20-A Output Current
- 4.75-V to 14-V Input Voltage
- Programmable Wide-Output Voltage (0.7 V to 3.6 V)
- Efficiencies up to 96%
- Digital I/O
 - PWM signal
 - INHIBIT
 - Current limit flag (FAULT)
 - Synchronous Rectifier Enable (SRE)
- Analog I/O
 - Temperature
 - Output current
- Safety Agency Approvals: (Pending)
 - UL/IEC/CSA-C22.2 60950-1
- Operating Temperature: –40°C to 85°C

APPLICATIONS

- Digital Power Systems using UCD92XX Digital Controllers



DESCRIPTION

The PTD08A020W is a high-performance 20-A rated, non-isolated digital PowerTrain module. This module is the power conversion section of a digital power system which incorporates TI's UCD7230 MOSFET driver IC. The PTD08A020W must be used in conjunction with a digital power controller such as the UCD9240 or UCD9110 family. The PTD08A020W receives control signals from the digital controller and provides parametric and status information back to the digital controller. Together, PowerTrain modules and a digital power controller form a sophisticated, robust, and easily configured power management solution.

Operating from an input voltage range of 4.75 V to 14 V, the PTD08A020W provides step-down power conversion to a wide range of output voltages from, 0.7 V to 3.6 V. The wide input voltage range makes the PTD08A020W particularly suitable for advanced computing and server applications that utilize a loosely regulated 8-V, 9.6-V or 12-V intermediate distribution bus. Additionally, the wide input voltage range increases design flexibility by supporting operation with tightly regulated 5-V or 12-V intermediate bus architectures.

The module incorporates output over-current and temperature monitoring which protects against most load faults. Output current and module temperature signals are provided for the digital controller to permit user defined over-current and over-temperature warning and fault scenarios.

The module uses double-sided surface mount construction to provide a low profile and compact footprint. Package options include both through-hole and surface mount configurations that are lead (Pb) - free and RoHS compatible.



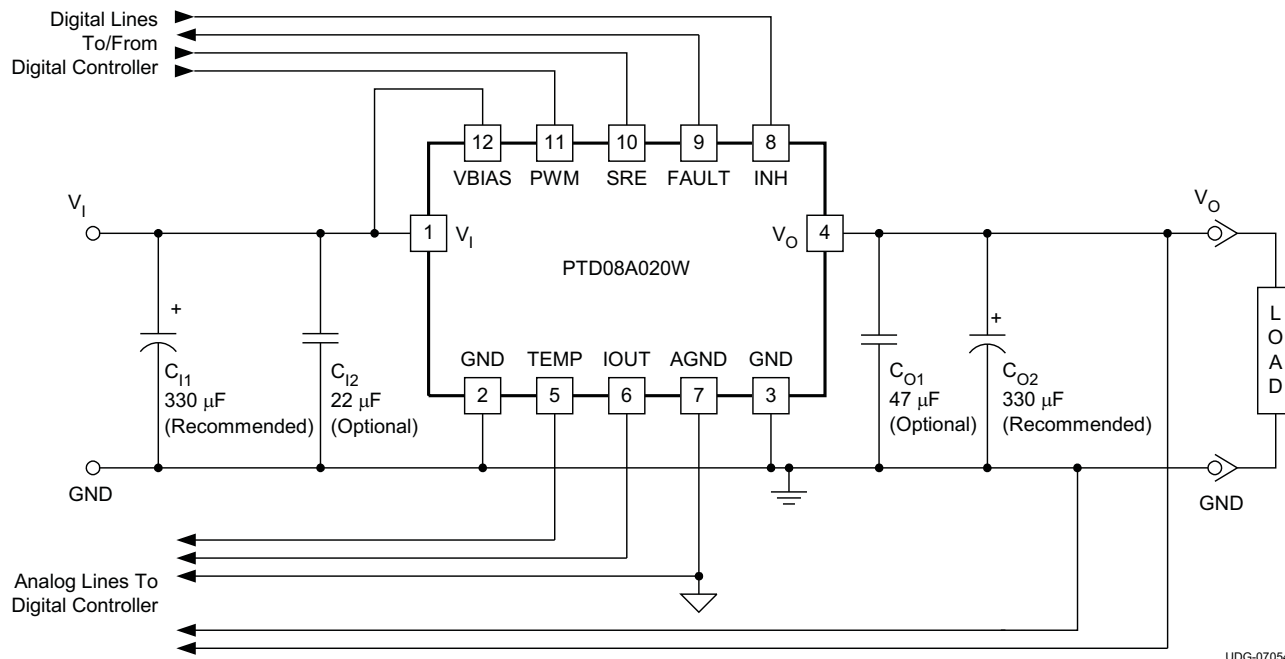
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POWERTRAIN is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Standard PTD08A020W Application



ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

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ENVIRONMENTAL AND ABSOLUTE MAXIMUM RATINGS

(Voltages are with respect to GND)

				UNIT
V_I	Input voltage		16	V
V_B	Bias voltage		16	V
T_A	Operating temperature range	Over V_I range	–40 to 85	
T_{wave}	Wave soldering temperature	Surface temperature of module body or pins for 5 seconds maximum.	260	°C
T_{stg}	Storage temperature		–55 to 125 ⁽¹⁾	
	Mechanical shock	Per Mil-STD-883D, Method 2002.3, 1msec, 1/2 sine, mounted	250	G
	Mechanical vibration	Mil-STD-883D, Method 2007.2, 20-2000 Hz	15	
	Weight		7.4	grams
MTBF	Reliability	Per Telcordia SR-332, 50% stress, $T_A = 40^\circ\text{C}$, ground benign	9.26	10 ⁶ Hr
	Flammability	Meets UL94V-O		

(1) The shipping tray or tape and reel cannot be used to bake parts at temperatures higher than 65°C.

ELECTRICAL CHARACTERISTICS

PTD08A020W

$T_A = 25^\circ\text{C}$, $F_{SW} = 350\text{kHz}$, $V_I = 12\text{ V}$, $V_O = 3.3\text{ V}$, $V_B = V_I$, $C_{I1} = 330\text{ }\mu\text{F}$, $C_{I2} = 22\text{ }\mu\text{F}$ ceramic, $C_{O1} = 47\text{ }\mu\text{F}$ ceramic, $C_{O2} = 330\text{ }\mu\text{F}$, and $I_O = I_{O(max)}$ (unless otherwise stated)

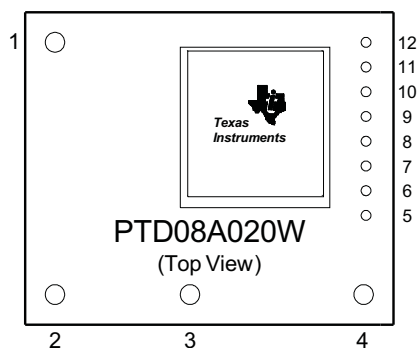
PARAMETER		TEST CONDITIONS		PTD08A010W			UNIT
				MIN	TYP	MAX	
I_O	Output current	Over V_O range	25°C , natural convection	0		20	A
V_I	Input voltage range	Over I_O range		4.75		14 ⁽¹⁾	V
V_{OAdj}	Output voltage adjust range	Over I_O range		0.7 ⁽¹⁾		3.6	V
η	Efficiency	$I_O = 20\text{ A}$, $f_s = 350\text{ kHz}$	$V_O = 3.3\text{ V}$		91%		
			$V_O = 2.5\text{ V}$		89%		
			$V_O = 1.8\text{ V}$		86%		
			$V_O = 1.5\text{ V}$		84%		
			$V_O = 1.2\text{ V}$		83%		
			$V_O = 1.0\text{ V}$		80%		
V_{OPP}	V_O Ripple (peak-to-peak)	20-MHz bandwidth			20		mV _{PP}
V_B	Bias voltage			4.75		14	V
V_B $UVLO$	Bias voltage under voltage lockout	V_B increasing		4.25	4.5	4.75	V
		V_B decreasing		4.0	4.25	4.5	
I_B	Bias current	Inhibit (pin 8) to AGND	Standby		5		mA
			Switching		42		
V_{IH}	High-level input voltage	SRE, INH, & PWM input levels		2.0		5.5	V
V_{IL}	Low-level input voltage					0.8	
	PWM input	Frequency range		300		500	kHz
		Pulse width limits		130			
	TEMP output	Range		-40		125	$^\circ\text{C}$
		Accuracy, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		-4.0		+6.0	$^\circ\text{C}$
		Slope			10		mV/ $^\circ\text{C}$
		Offset, $T_A = 0^\circ\text{C}$			500		mV
V_{OH}	FAULT output	High-level output voltage, $I_{FAULT} = 4\text{ mA}$		2.7	3.3		V
V_{OL}		Low-level output voltage, $I_{FAULT} = 4\text{ mA}$			0	0.6	
I_{LIM}		Overcurrent threshold; Reset, followed by auto-recovery			30		A
	IOUT output	Range		0.15		3.5	V
		Gain		46	66	86	mV/A
		Offset		0.44	0.6	0.76	V
		Output Impedance		10	15	20	k Ω
C_I	External input capacitance	Nonceramic		330 ⁽²⁾			μF
		Ceramic		22 ⁽²⁾			
C_O	External output capacitance	Capacitance Value	Nonceramic	330 ⁽³⁾	10,000 ⁽⁴⁾		μF
			Ceramic	47 ⁽³⁾		⁽³⁾	
		Equivalent series resistance (non-ceramic)		1 ⁽⁵⁾			m Ω

- (1) The maximum input voltage is duty cycle limited to $(V_O/(130\text{ns} \times F_{SW}))$ or 14 V, whichever is less. The maximum allowable input voltage is a function of switching frequency.
- (2) A 22 μF ceramic input capacitor is recommended for operation. An additional 330 μF bulk capacitor rated for a minimum of 500mA rms of ripple current is recommended. Refer to the UCD9240 controller datasheet and user interface for application specific capacitor specifications.
- (3) A 47 μF ceramic output capacitor is recommended for operation. An additional 330 μF bulk capacitor is recommended for improved transient response. See the related Application Information section for further guidance. Refer to the UCD9240 controller datasheet and user interface for application specific capacitor specifications.
- (4) 10,000 μF is the calculated maximum output capacitance given a 1V/msec output voltage rise time. Additional capacitance or increasing the output voltage rise rate may trigger the overcurrent threshold at start-up.
- (5) This is the minimum ESR for all non-ceramic output capacitance. Refer to the UCD9240 controller datasheet and user interface for application specific capacitor specifications.

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
V _I	1	The positive input voltage power node to the module, which is referenced to common GND.
GND	2	This is the common ground connection for the V _I and V _O power connections.
	3	
V _O	4	The regulated positive power output with respect to GND.
TEMP	5	Temperature sense output. The voltage level on this pin represents the temperature of the module.
IOUT	6	Current sense output. The voltage level on this pin represents the average output current of the module.
AGND	7	Analog ground return. It is the 0 V _{dc} reference for the control inputs.
INH ⁽¹⁾	8	The inhibit pin is a negative logic input that is referenced to AGND. Applying a low-level signal to this pin disables the module and turns off the output voltage. A 10 kΩ pull-up to 3.3 V or 5 V is required if the INH signal is not used.
FAULT	9	Current limit flag. The Fault signal is a 3.3 V digital output which is latched high after an over-current condition. The Fault is reset after two complete PWM cycles without an over-current condition (third rising edge of the PWM).
SRE	10	Synchronized Rectifier Enable. This pin is a high impedance digital input. A 3.3 V or 5 V logic level signals is used to enable the synchronous rectifier switch. When this signal is high, the module will source and sink output current. When this signal is low, the module will only source current.
PWM	11	This is the PWM input pin. It is a high impedance digital input that accepts 3.3 V or 5 V logic level signals up to 500 MHz.
VBIAS	12	Bias voltage supply required to power internal circuitry. For optimal performance connect VBIAS to V _I .

(1) Denotes negative logic: Open = Normal operation, Ground = Function active



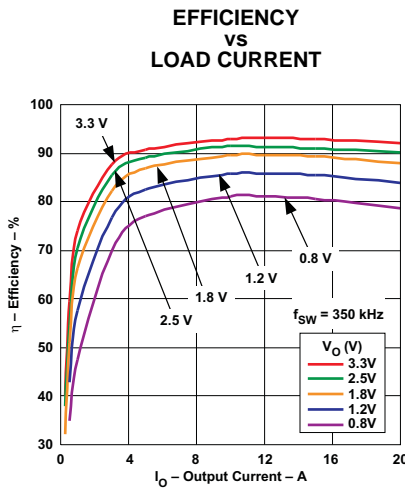
TYPICAL CHARACTERISTICS⁽¹⁾⁽²⁾CHARACTERISTIC DATA ($V_I = 12\text{ V}$)

Figure 1.

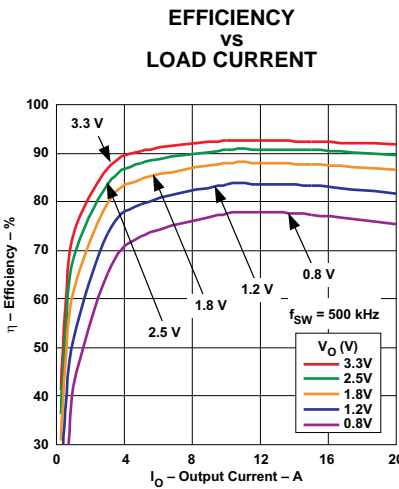


Figure 2.

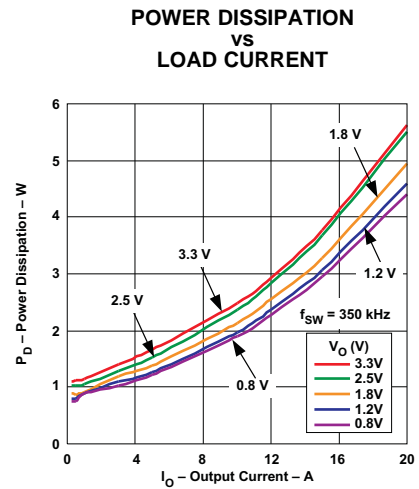


Figure 3. Safe Operating Area

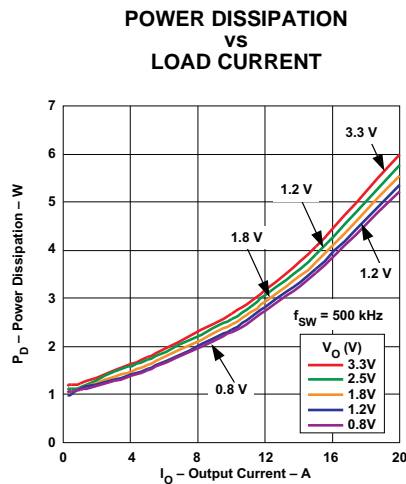


Figure 4.

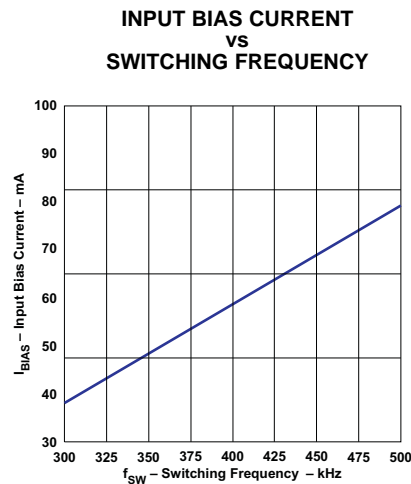


Figure 5.

- (1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to [Figure 1](#) thru [Figure 5](#).
- (2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm double-sided PCB with 2 oz. copper. For surface mount packages (AS and AZ suffix), multiple vias must be utilized. Please refer to the mechanical specification for more information. Applies to [Figure 6](#) thru [Figure 9](#).

TYPICAL CHARACTERISTICS⁽³⁾⁽⁴⁾ (continued)

CHARACTERISTIC DATA ($V_I = 12\text{ V}$) Safe Operating Area

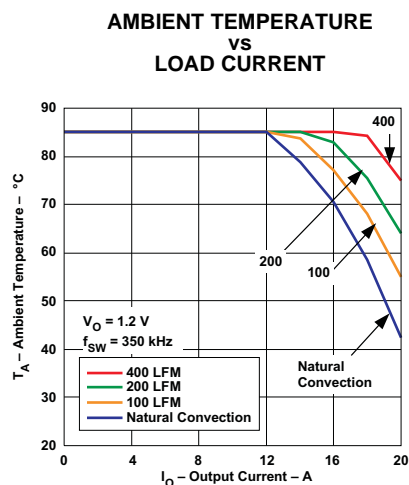


Figure 6. Safe Operating Area

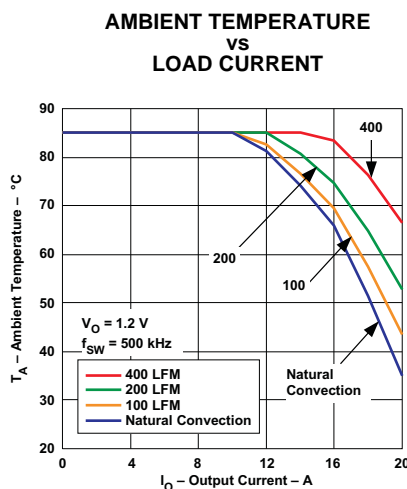


Figure 7. Safe Operating Area

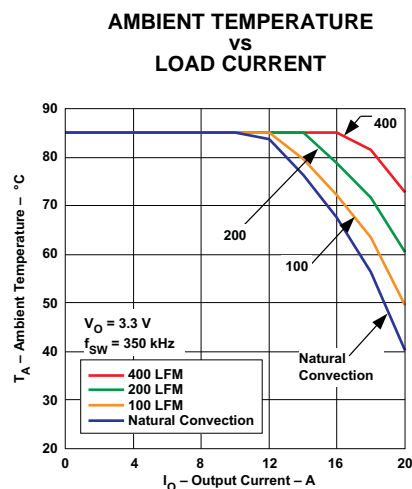


Figure 8.

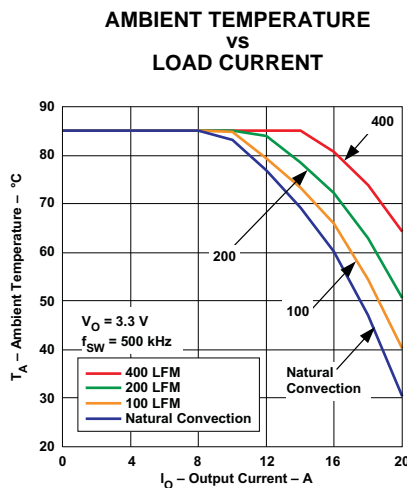


Figure 9.

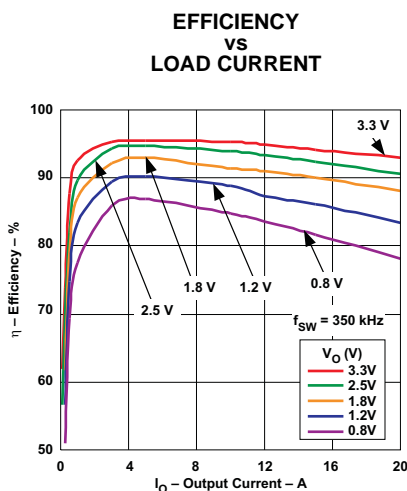
TYPICAL CHARACTERISTICS⁽¹⁾⁽²⁾CHARACTERISTIC DATA ($V_I = 5\text{ V}$)

Figure 10.

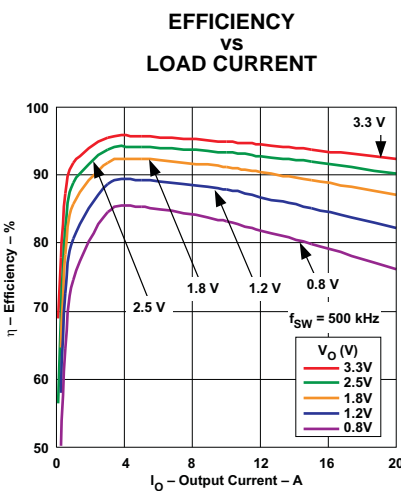


Figure 11.

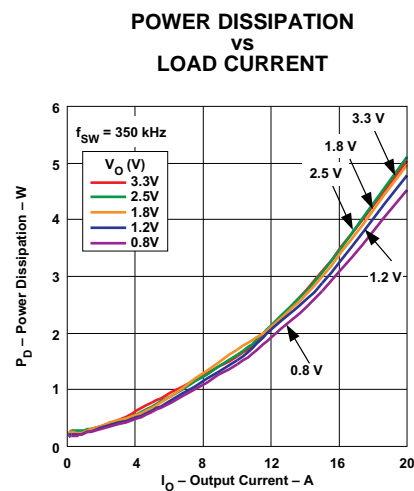


Figure 12.

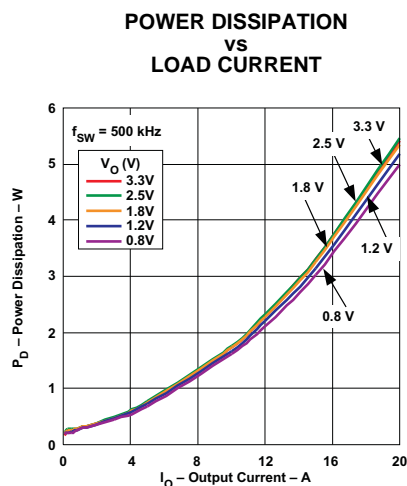


Figure 13.

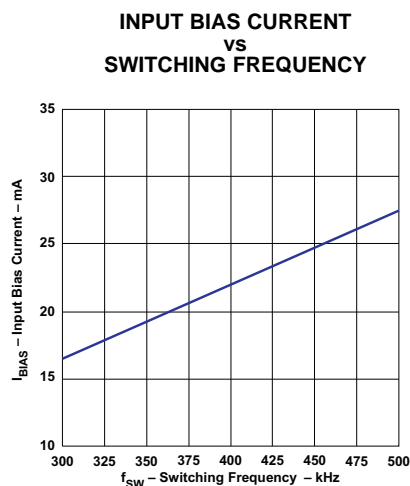


Figure 14.

- (1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 10 thru Figure 14.
- (2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm double-sided PCB with 2 oz. copper. For surface mount packages (AS and AZ suffix), multiple vias must be utilized. Please refer to the mechanical specification for more information. Applies to Figure 15 thru Figure 18.

TYPICAL CHARACTERISTICS⁽³⁾⁽⁴⁾ (continued)

CHARACTERISTIC DATA ($V_I = 5\text{ V}$) Safe Operating Area

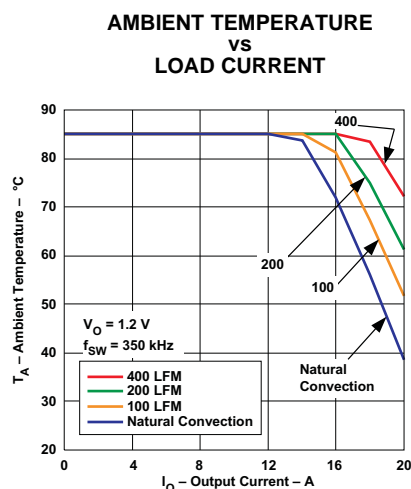


Figure 15. Safe Operating Area

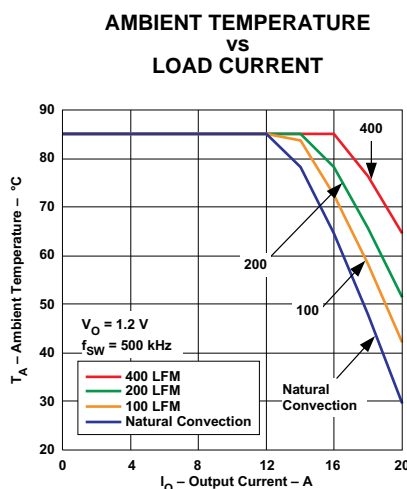


Figure 16.

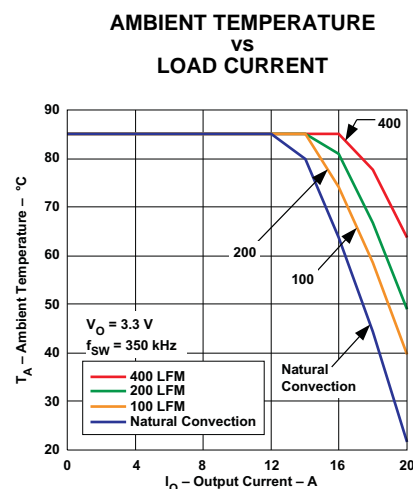


Figure 17.

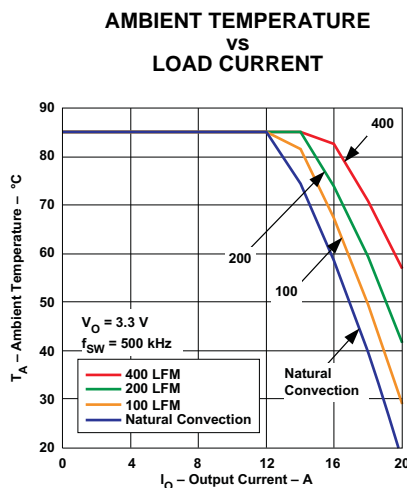


Figure 18.

APPLICATION INFORMATION

Digital Power

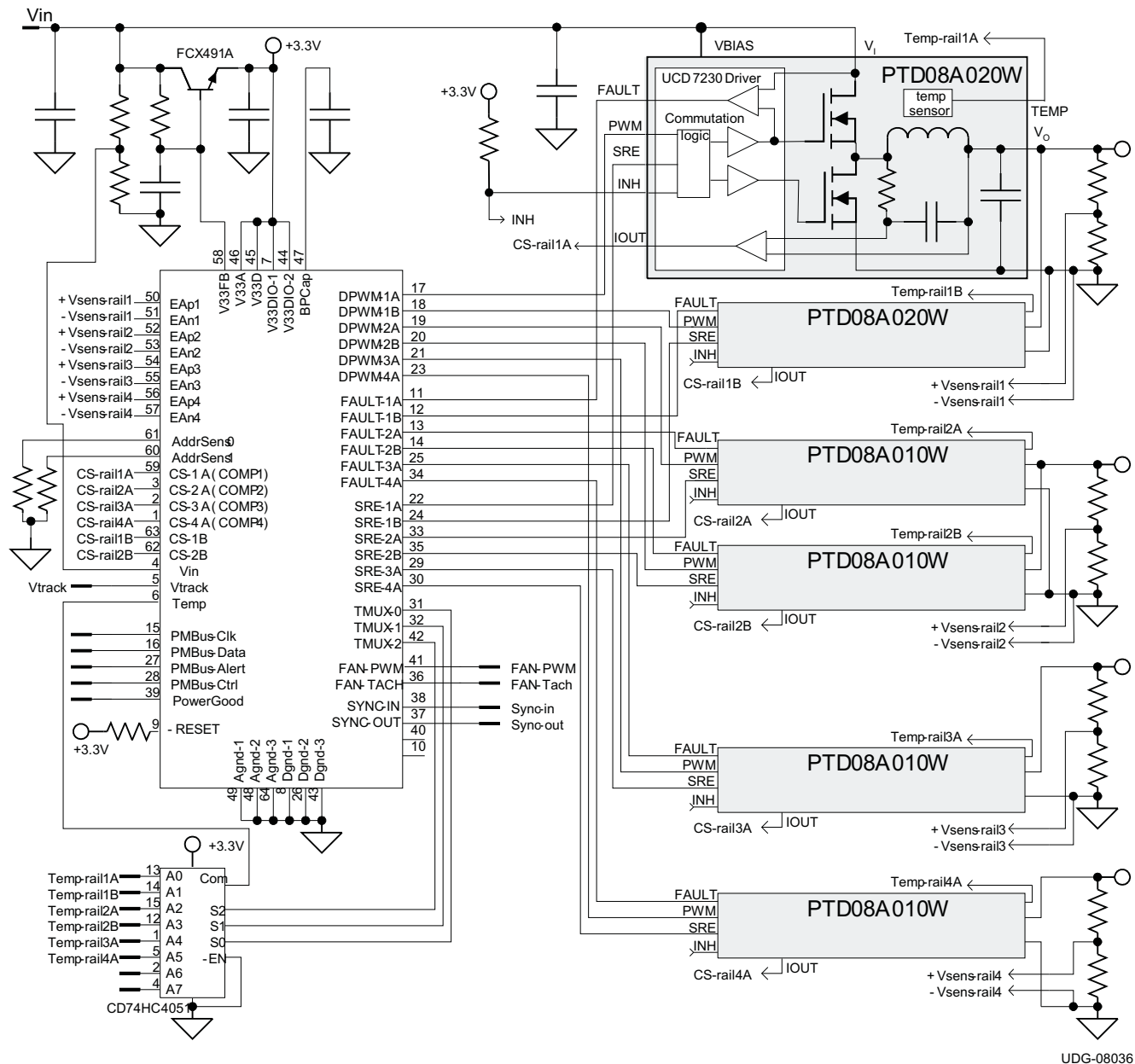


Figure 19. Typical Application Schematic

Figure 19 shows the UCD9240 power supply controller working in a system which requires the regulation of four independent power supplies. The loop for each power supply is created by the respective voltage outputs feeding into the Error ADC differential inputs, and completed by DPWM outputs feeding into the UCD7230 drivers which are shown on the PTD08A010W and PTD08A020W modules.

UCD9240 Graphical User Interface (GUI)

When using the UCD9240 digital controller along with digital PowerTrain modules to design a digital power system, several internal parameters of the modules are required to run the Fusion Digital Power Designer GUI. See the plant parameters below for the PTD08A010W and PTD08A020W digital PowerTrain modules.

PTD08A010W Plant Parameters

PTD08A010W Plant Parameters			
L (μH)	DCR (mΩ)	Rds-on-hi (mΩ)	Rds-on-lo (mΩ)
0.90	2.2	3.6	3.6

PTD08A020W Plant Parameters

PTD08A020W Plant Parameters			
L (μH)	DCR (mΩ)	Rds-on-hi (mΩ)	Rds-on-lo (mΩ)
1.0	1.5	5.0	2.5

Internal output capacitance is present on the digital PowerTrain modules themselves. When using the GUI interface this capacitance information must be included along with any additional external capacitance. See the capacitor parameters below for the PTD08A010W and PTD08A020W digital PowerTrain modules.

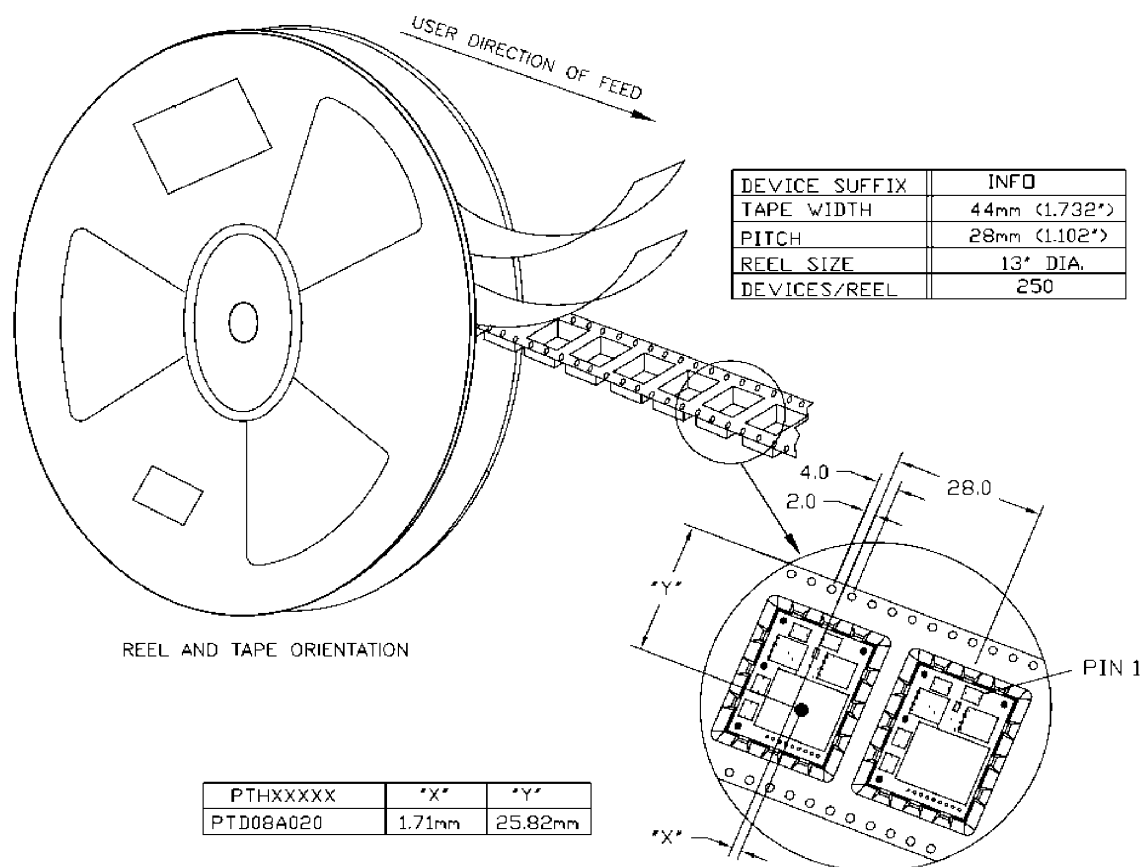
PTD08A010W Capacitor Parameters

PTD08A010W Capacitor Parameters			
C (μF)	ESR (mΩ)	ESL (nH)	Quantity
47	1.5	2.5	1

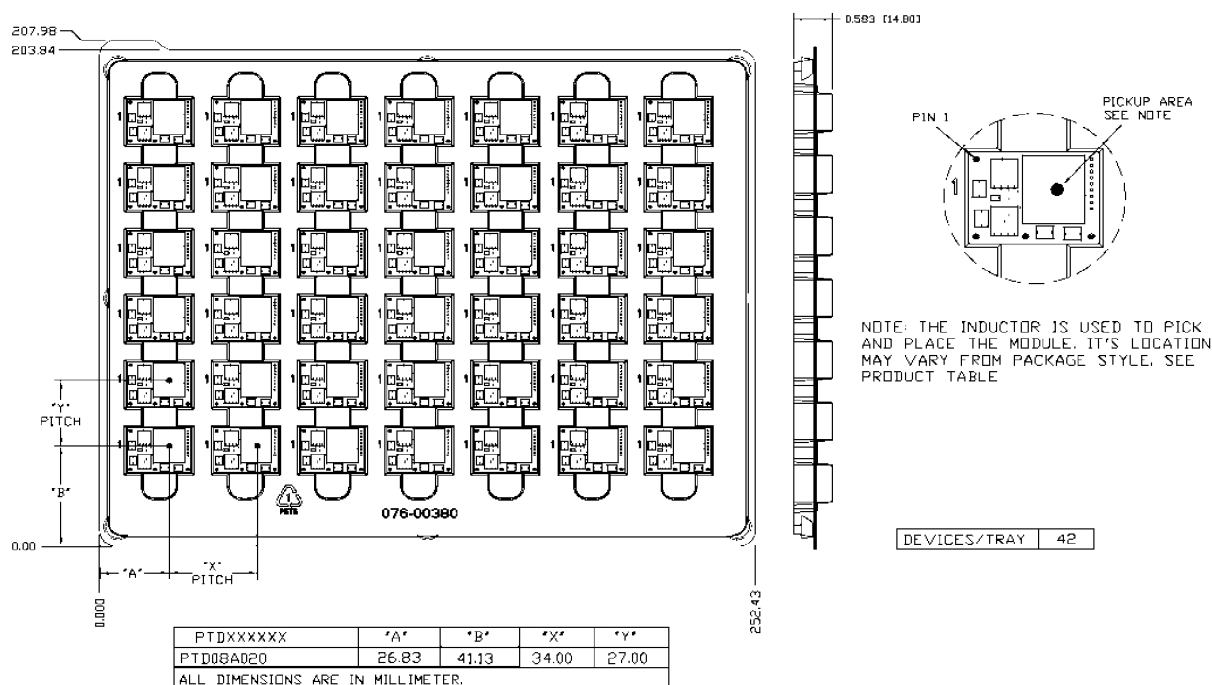
PTD08A020W Capacitor Parameters

PTD08A020W Capacitor Parameters			
C (μF)	ESR (mΩ)	ESL (nH)	Quantity
47	1.5	2.5	2

TAPE AND REEL



TRAY



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
PTD08A020WAD	ACTIVE	DIP MOD ULE-TH	EGP	12	42	TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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