

To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

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HAT2108R

Silicon N Channel Power MOS FET
High Speed Power Switching

RENESAS

ADE-208-1574C (Z)

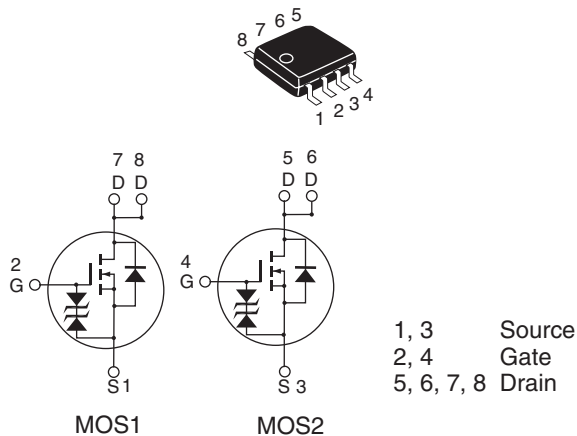
4th. Edition
Aug. 2002

Features

- Low on-resistance
- Capable of 2.5 V gate drive
- Low drive current
- High density mounting

Outline

SOP-8



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	28	V
Gate to source voltage	V_{GSS}	±12	V
Drain current	I_D	11	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	88	A
Body–drain diode reverse drain current	I_{DR}	11	A
Channel dissipation	P_{ch} ^{Note2}	2	W
Channel dissipation	P_{ch} ^{Note3}	3	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

- Notes:
- 1. $PW \leq 10 \mu s$, duty cycle $\leq 1 \%$
 - 2. 1 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10s$
 - 3. 2 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10s$

Electrical Characteristics

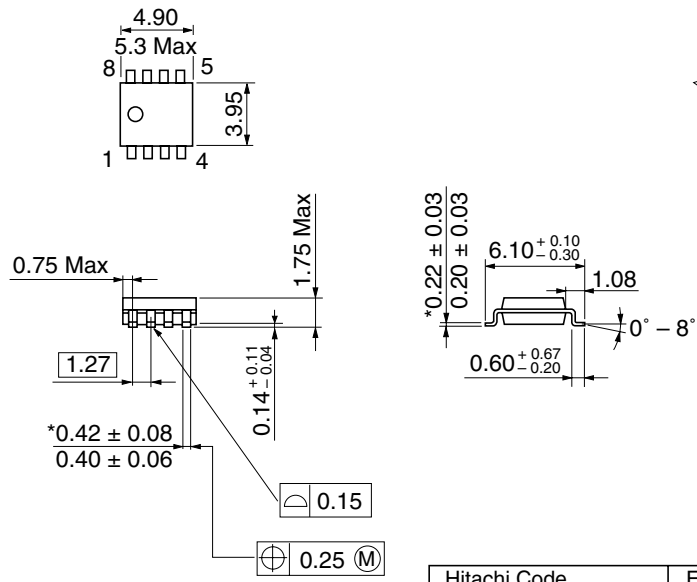
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	28	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 12	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 10 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 28 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	0.4	—	1.4	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	12	15	$\text{m}\Omega$	$I_D = 5.5 \text{ A}$, $V_{GS} = 4 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	15	22	$\text{m}\Omega$	$I_D = 5.5 \text{ A}$, $V_{GS} = 2.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	17	28	—	S	$I_D = 5.5 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	Ciss	—	2200	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	Coss	—	400	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	240	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Qg	—	16	—	nc	$V_{DD} = 10 \text{ V}$
Gate to source charge	Qgs	—	5.2	—	nc	$V_{GS} = 4 \text{ V}$
Gate to drain charge	Qgd	—	4.8	—	nc	$I_D = 11 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	30	—	ns	$V_{GS} = 4 \text{ A}$, $I_D = 5.5 \text{ A}$
Rise time	t_r	—	35	—	ns	$V_{DD} \cong 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	70	—	ns	$R_L = 1.81 \text{ }\Omega$
Fall time	t_f	—	25	—	ns	$R_g = 4.7 \text{ }\Omega$
Body-drain diode forward voltage	V_{DF}	—	0.85	1.11	V	$I_F = 11 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	40	—	ns	$I_F = 11 \text{ A}$, $V_{GS} = 0$ $diF/dt = 50 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

Package Dimensions

As of January, 2002
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-8DA
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.085 g

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Sales Offices

HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: (03) 3270-2111 Fax: (03) 3270-5109

URL <http://www.hitachisemiconductor.com/>

For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1> (408) 433-0223

Hitachi Europe Ltd.
Electronic Components Group
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585200

Hitachi Europe GmbH
Electronic Components Group
Dornacher Straße 3
D-85622 Feldkirchen
Postfach 201, D-85619 Feldkirchen
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Asia Ltd.
Hitachi Tower
16 Collyer Quay #20-00
Singapore 049318
Tel: <65>-6538-6533/6538-8577
Fax: <65>-6538-6933/6538-3877
URL: <http://semiconductor.hitachi.com.sg>

Hitachi Asia Ltd.
(Taipei Branch Office)
4/F, No. 167, Tun Hwa North Road
Hung-Kuo Building
Taipei (105), Taiwan
Tel: <886>-(2)-2718-3666
Fax: <886>-(2)-2718-8180
Telex: 23222 HAS-TP
URL: <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon Hong Kong
Tel: <852>-2735-9218
Fax: <852>-2730-0281
URL: <http://semiconductor.hitachi.com.hk>

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