S75WS-P based MCP/POP Products

1.8 Volt-only x16 Simultaneous Read/Write, Burst Mode Flash (NOR Interface) S30MS-P (NAND Interface) ORNAND™ Flash pSRAM Type 2

Data Sheet *(Advance Information)*

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

Publication Number S75WS-P_00 **Revision** 02 **Issue Date** September 6, 2006

Notice On Data Sheet Designations

Spansion Inc. issues data sheets with Advance Information or Preliminary designations to advise readers of product information or intended specifications throughout the product life cycle, including development, qualification, initial production, and full production. In all cases, however, readers are encouraged to verify that they have the latest information before finalizing their design. The following descriptions of Spansion data sheet designations are presented here to highlight their presence and definitions.

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The Advance Information designation indicates that Spansion Inc. is developing one or more specific products, but has not committed any design to production. Information presented in a document with this designation is likely to change, and in some cases, development on the product may discontinue. Spansion Inc. therefore places the following conditions upon Advance Information content:

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Preliminary

The Preliminary designation indicates that the product development has progressed such that a commitment to production has taken place. This designation covers several aspects of the product life cycle, including product qualification, initial production, and the subsequent phases in the manufacturing process that occur before full production is achieved. Changes to the technical specifications presented in a Preliminary document should be expected while keeping these aspects of production under consideration. Spansion places the following conditions upon Preliminary content:

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Combination

Some data sheets contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document distinguishes these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion Inc. applies the following conditions to documents in this category:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion Inc. deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur."

Questions regarding these document designations may be directed to your local AMD or Fujitsu sales office.

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Data Sheet *(Advance Information)*

Features

- **Power supply voltage of 1.7 to 1.95V**
- **Flash access time: 80 ns (NOR), 25 ns (ORNAND)**
- **Flash burst frequencies: 66 MHz, 80 MHz, 108 MHz**
- **pSRAM Access time: 70 ns, 20 ns (Page)**
- **pSRAM burst frequency: 66 MHz, 80 MHz, 104 MHz**
- **Package:**
  - 12 x 12 mm PoP
  - 9 x 12 mm, 115-ball MCP
- **Operating Temperature**
  - –25°C to +85°C (wireless)

The S75WS series is a product line of MCPs or POPs, and consists of:

- One S29WS-P NOR flash memory die
- One or more S30MS-P NAND interface ORNAND flash memory die
- pSRAM Type 2

For detailed specifications, please refer to the individual data sheets

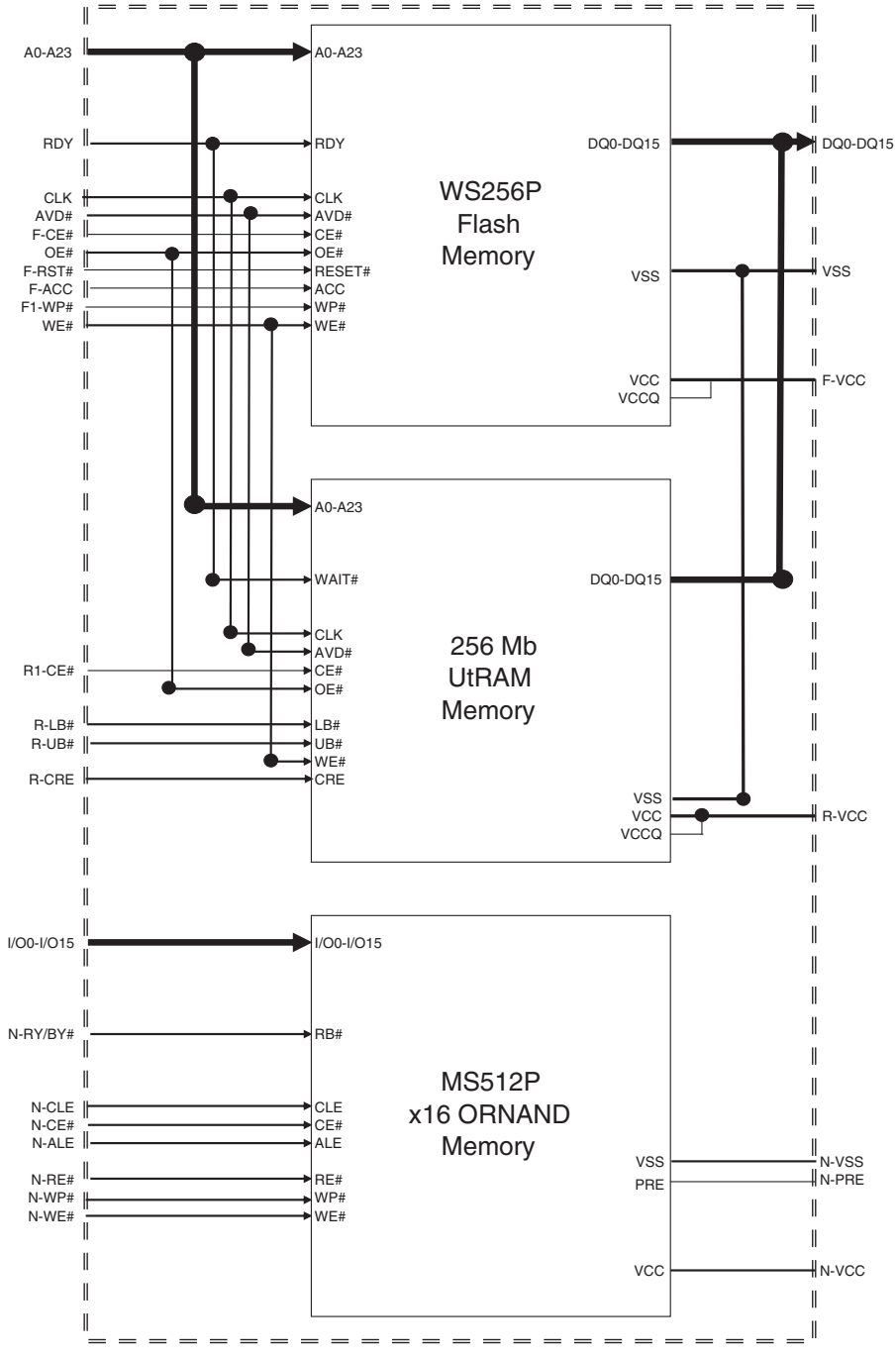
Document	Publication Identification Number (PID)
S29WS-P	S29WS-P_00
256Mb pSRAM Type 2	psram_24
S30MS-P	S30MS-P_00

Publication Number S75WS-P_00 **Revision 02** **Issue Date** September 6, 2006

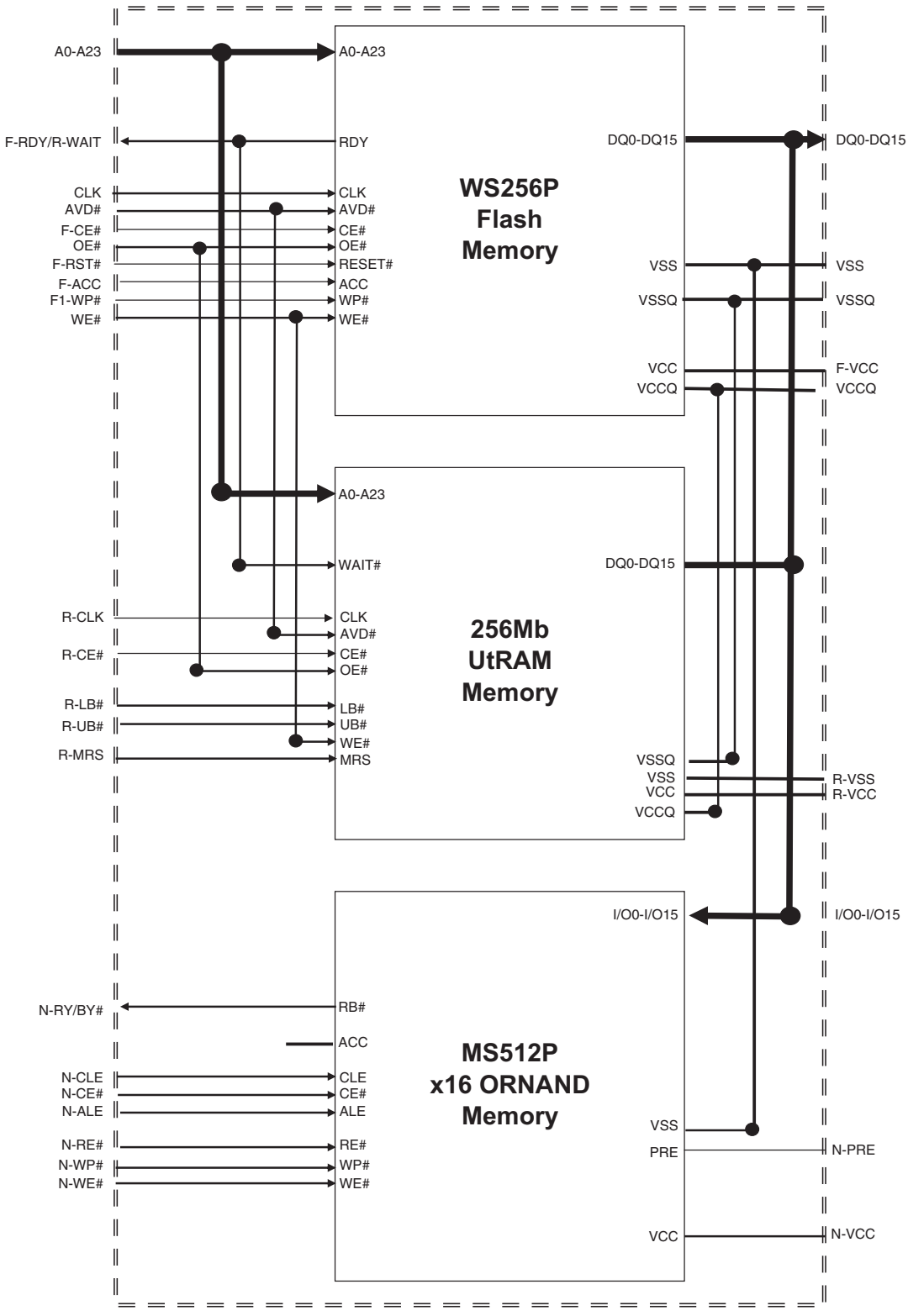
1. Product Selector Guide

Device	Model Number	Flash Density (Mb)	pSRAM Density (Mb)	ORNAND Density (Mb)	Flash Speed (MHz)	pSRAM Speed (MHz)	pSRAM Supplier	Package
S75WS256PEFKFF	LW	256	256	512	66	104	Type 2	AMB128: POP 12 x12 x 1.15 mm
S75WS256PEFJF5	VS				80			FMC115: MCP 12 x 9 mm

2. MCP Block Diagram

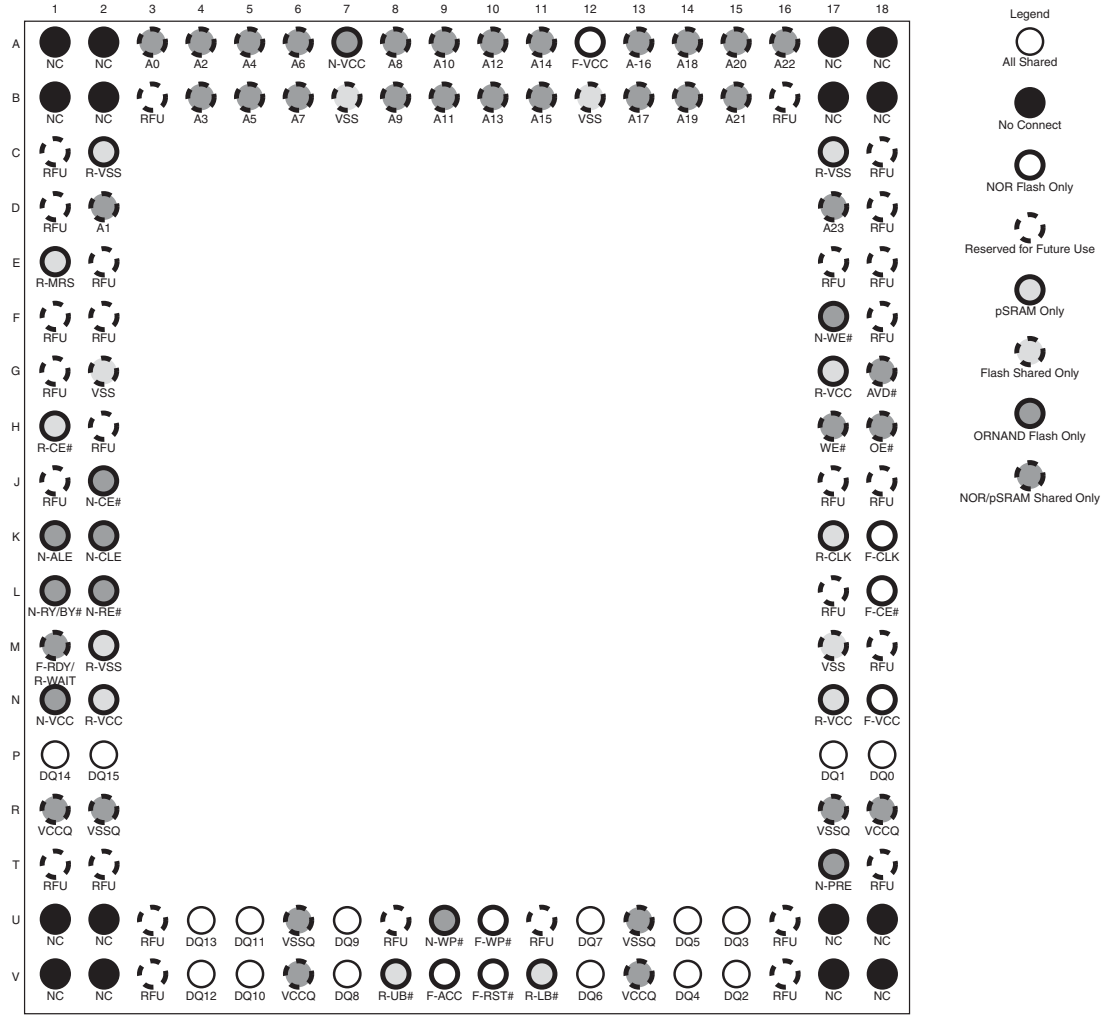


3. POP Block Diagram

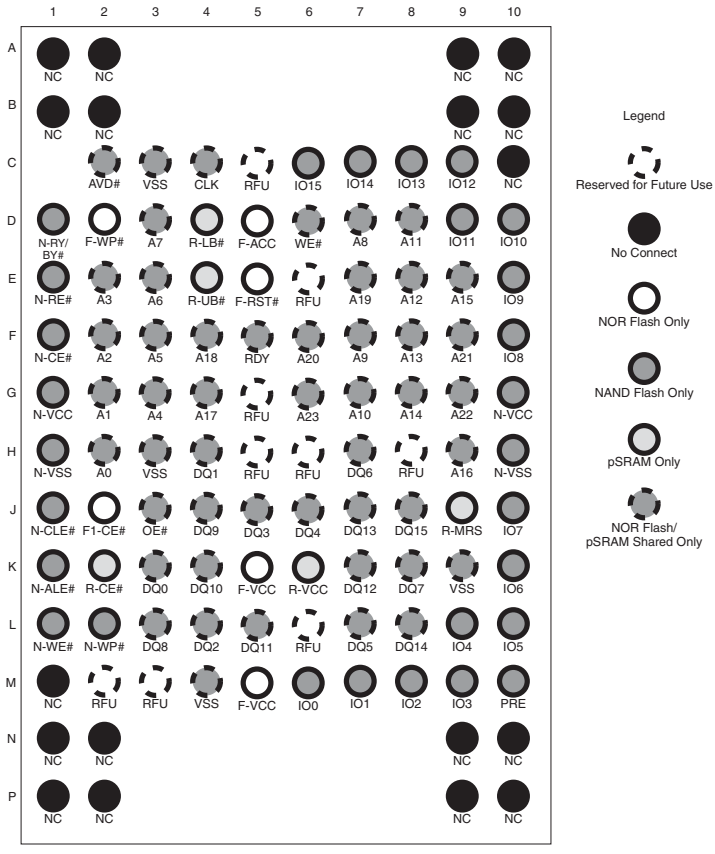


4. Connection Diagrams

4.1 12 x 12 mm PoP



4.2 9 x 12 mm, 115-ball MCP

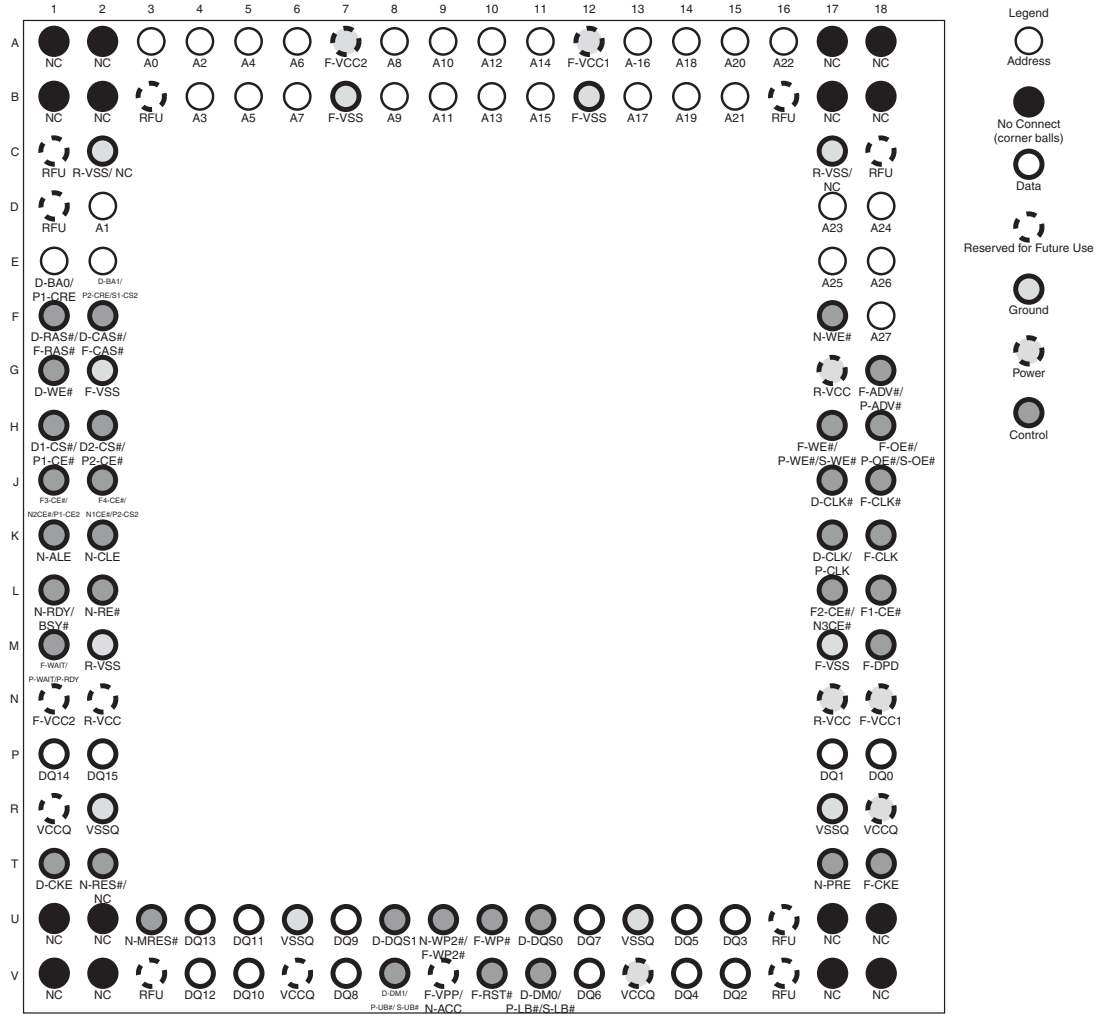


4.3 Special Handling Instructions For FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150×C for prolonged periods of time.

4.4 Look-ahead Ballout for Future Designs



5. Input/Output Descriptions

Table 5.1 identifies the input and output package connections provided on the device.

Table 5.1 Input/Output Descriptions (Sheet 1 of 2)

Symbol	Signal Type	Description	WS (NOR)	pSRAM	MS (ORNAND)
Amax-A0	Input	NOR Flash Address inputs	X	X	
DQ15-DQ0	I/O	Flash Data input/output, shared between NOR and ORNAND Flash; shared with IO15-IO0 for ORNAND	X	X	X
F-CE#	Input	NOR Flash Chip-enable input #1. Asynchronous relative to CLK for Burst Mode.	X		
OE#	Output	Output Enable input. Asynchronous relative to CLK for Burst mode.	X	X	
WE#	Input	Write Enable input.	X	X	
F-V_{CC}	Power	NOR Flash device power supply (1.7 V - 1.95V).	X		
F-V_{CCQ}	Power	Input/Output Buffer power supply.	X		
V_{SS}	Ground	Ground	X	X	X
RFU	—	Reserved for Future Use			
RDY	Output	Flash ready output. Indicates the status of the Burst read. V_{OL} = data valid. The Flash RDY pin is shared with the WAIT pin of the pSRAM.	X	X	
CLK	Input	NOR Flash Clock, shared with CLK of burst-mode pSRAM. The first rising edge of CLK in conjunction with AVD# low latches the address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access.	X	X	
AVD#	Input	NOR Flash Address Valid input. Shared with AVD# of burst-mode pSRAM. Indicates to device that the valid address is present on the address inputs. V_{IL} = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. V_{IH}= device ignores address inputs	X	X	
F-RST#	Input	NOR Flash hardware reset input. V_{IL}= device resets and returns to reading array data	X		
F-WP#	Input	NOR Flash hardware write protect input. V_{IL} = disables program and erase functions in the four outermost sectors.	X		
F-ACC	Input	NOR Flash accelerated input. At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables all program and erase functions. Should be at V_{IH} for all other conditions.	X		
R-CE#	Input	Chip-enable input for pSRAM		X	
R-MRS	Input	Mode Select Register (pSRAM). For Type 2 only.		X	
R-V_{CC}	Power	pSRAM Power Supply		X	
R-UB#	Input	Upper Byte Control (pSRAM)		X	
R-LB#	Input	Lower Byte Control (pSRAM)		X	
DNU	—	Do Not Use			
N-CLE	Input	Command Latch Enable: The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the WE# signal while CE# is low and CLE is High.			X
N-ALE	Input	Address Latch Enable: The ALE signal is used to control loading of either address information or input data into the internal address/data register. Address information is latched on the rising edge of WE# if CE# is low and ALE is High. Input data is latched if CE# is low and ALE is Low.			X

Table 5.1 Input/Output Descriptions (Sheet 2 of 2)

Symbol	Signal Type	Description	WS (NOR)	pSRAM	MS (ORNAND)
N-CE#	Input	Chip Enable: The device enters a low-power Standby mode when the device is in Ready mode. The CE# signal is ignored when the device is in a Busy state (RY/BY# = L), such as during a Page Buffer Load or Erase operation, and will not enter Standby mode even if the CE# input goes high. The CE# signal may be inactive during the Page Buffer write and Page Buffer load of the array data.			X
N-WE#	Input	Write Enable: The WE# signal is used to control the acquisition of data from the I/O port.			X
N-RE#	Output	Read Enable: The RE# signal controls serial data output. Data is available t_{REA} after the falling edge of RE#. The internal column address counter is also incremented (Address = Address + 1) on this falling edge.			X
N-WP#	Input	Write Protect: The WP# signal is used to protect the device from accidental programming or erasing. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.			X

6. Ordering Information

The order number is formed by a valid combinations of the following:

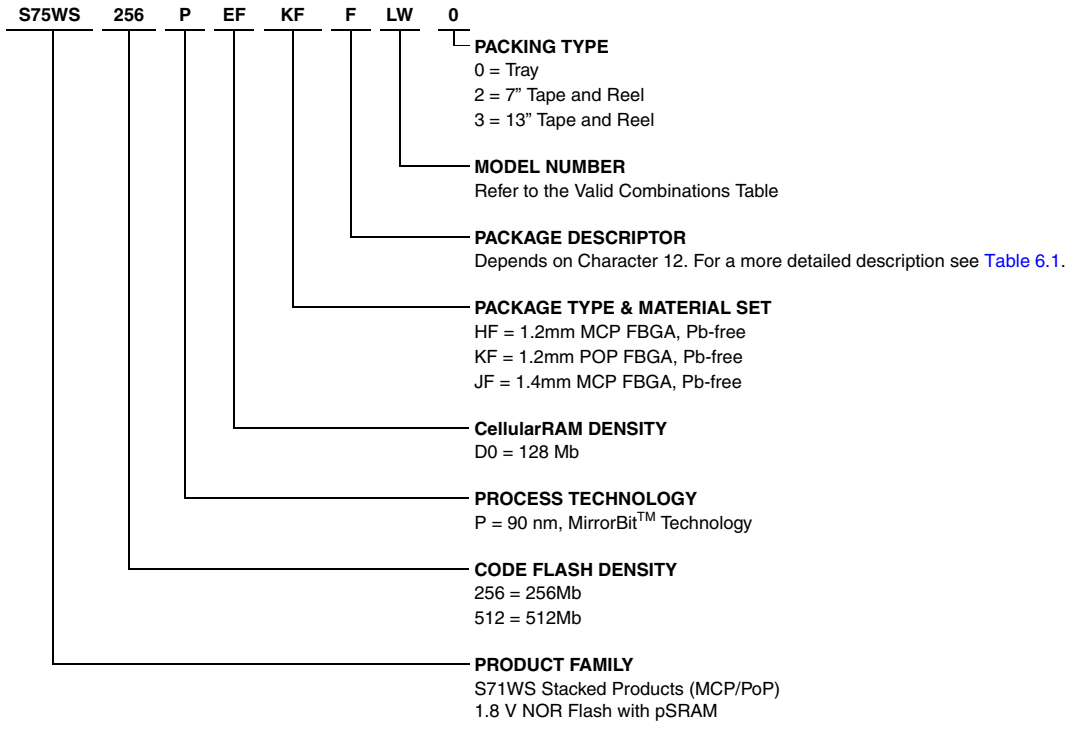


Table 6.1 Character Position Descriptions

Character 12	Character 14	Character 14 Description		
		Package Area	Package Ball Count	Raw Ball Size
H, J, or G	0	7x9 mm	56	0.35 mm
	1	7x9 mm	80	
	2	8x11.6 mm	64	
	3	8x11.6 mm	84	
	4	9x12 mm	84	
	5	9x12 mm	115	
	6	9x12 mm	137	
	7	11x13 mm	84	
	8	11x13 mm	115	
	9	11x13 mm	137	
K	A	11x11 mm	112	0.45 mm
	B	11x11 mm	112	0.50 mm
	D	12x12 mm	128	0.45 mm
	F	12x12 mm	128	0.50 mm
	G	14x14 mm	152	0.45 mm
	H	14x14 mm	152	0.50 mm
	J	15x15 mm	160	0.45 mm
	K	15x15 mm	160	0.50 mm
	L	17x17 mm	192	0.45 mm
	M	17x17 mm	192	0.50 mm

6.1 Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

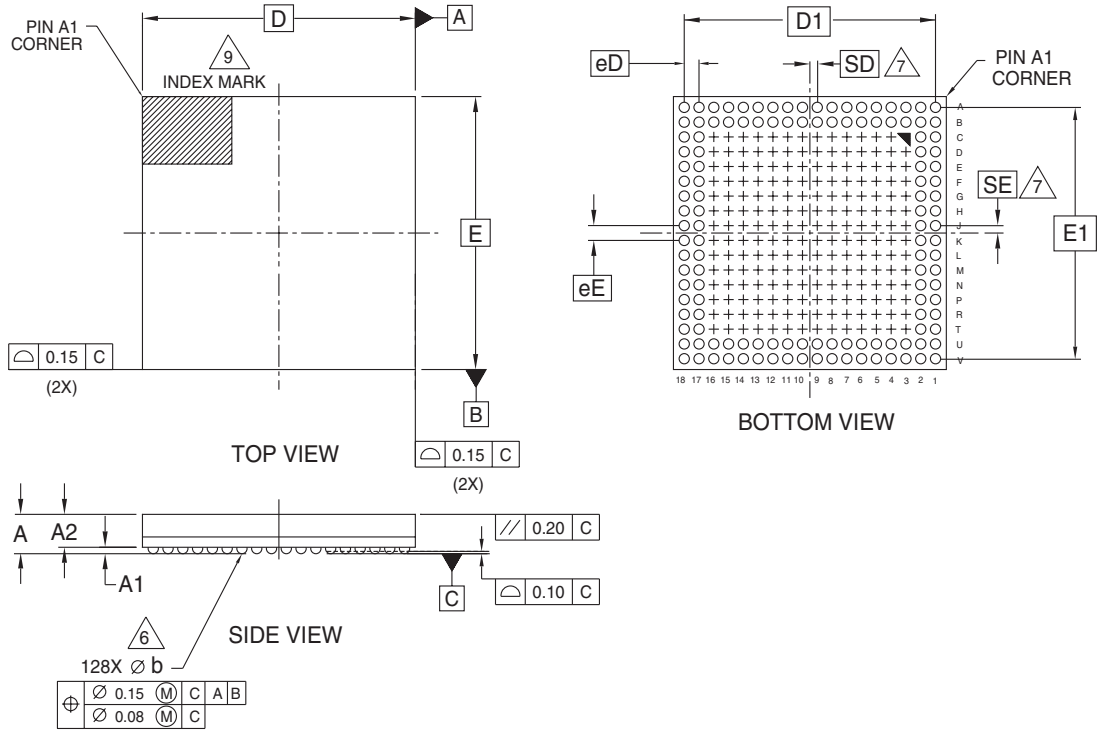
S75WS-P Valid Combinations					NOR Flash Speed (MHz)	pSRAM Speed (MHz)	pSRAM Supplier	Package Type	Package Markings
Device	Package & Material Set	Package Descriptor	Model Number	Packing Type					
S75WS256PEF	KF	F	LW	0, 2, 3 (Note 1)s	66	104	Type 2	12 x 12 mm	(Note 2)
	JF	5	VS		80	104	Type 2	9 x 12 mm	

Notes:

1. *Packing Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading* S *and packing type designator from ordering part number.*

7. Physical Dimensions

7.1 AMB128— 128-ball 12 x 12 mm Package-on-Package



PACKAGE	AMB 128			
JEDEC	N/A			
D x E	12.00 mm x 12.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.15	PROFILE
A1	0.39	---	---	BALL HEIGHT
A2	0.55	---	0.70	BODY THICKNESS
D		12.00 BSC		BODY SIZE
E		12.00 BSC		BODY SIZE
D1		11.05 BSC		MATRIX FOOTPRINT
E1		11.05 BSC		MATRIX FOOTPRINT
MD		18		MATRIX SIZE D DIRECTION
ME		18		MATRIX SIZE E DIRECTION
n		128		BALL COUNT
N		128		MAXIMUM NUMBER OF BALLS
R		2		NUMBER OF LAND PERIMETERS
Øb	0.45	0.50	0.55	BALL DIAMETER
eE		0.65 BSC		BALL PITCH
eD		0.65 BSC		BALL PITCH
SD SE		0.325 BSC		SOLDER BALL PLACEMENT
	C3~C16, D3~D16, E3~E16, F3~F16 G3~G16, H3~H16, J3~J16, K3~K16 L3~L16, M3~M16, N3~N16, P3~P16 R3~R16, T3~T16			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3.0, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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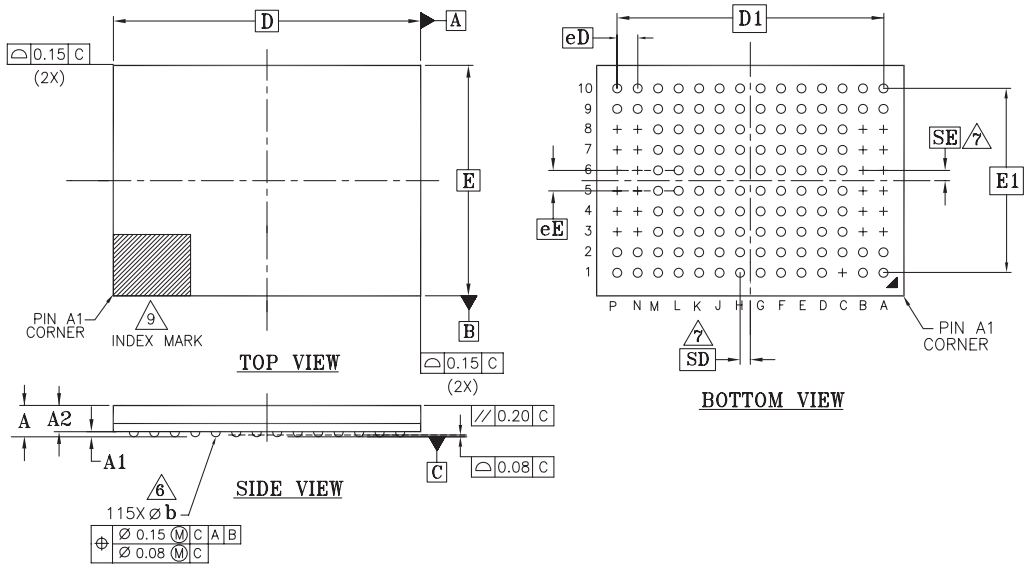
7.2 FMC115 — 115-ball 12 x 9 mm MCP



PACKAGE	FMC 115			
JEDEC	N/A			
D x E	12.00 mm x 9.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.40	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.96	---	1.11	BODY THICKNESS
D		12.00 BSC.		BODY SIZE
E		9.00 BSC.		BODY SIZE
D1		10.4 BSC.		MATRIX FOOTPRINT
E1		7.20 BSC.		MATRIX FOOTPRINT
MD		14		MATRIX SIZE D DIRECTION
ME		10		MATRIX SIZE E DIRECTION
n		115		BALL COUNT
Øb	0.35	0.40	0.45	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD SE		0.40 BSC.		SOLDER BALL PLACEMENT
	A3,A4,A5,A6,A7,A8 B3,B4,B5,B6,B7,B8,C1 N3,N4,N5,N6,N7,N8 P3,P4,P5,P6,P7,P8			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3603 \ 16-038.19 \ 9.6.6

8. Revision History

8.1 Revision 01 (May 5, 2006)

Initial release.

8.2 Revision 02 (September 6, 2006)

Added the MCP S75WS256PEF

Colophon

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