



## STL60NH3LL

N-channel 30 V - 0.0065  $\Omega$  - 30 A - PowerFLAT™ (6x5)  
ultra low gate charge STripFET™ Power MOSFET

### Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub> (max)	I <sub>D</sub>
STL60NH3LL	30V	<0.0085 $\Omega$	16A

- Improved die-to-footprint ratio
- Very low profile package (1mm max)
- Very low thermal resistance
- Very low gate charge
- Low threshold device

### Application

- Switching applications

### Description

This application specific Power MOSFET is the latest generation of STMicroelectronics unique “STripFET™” technology. The resulting transistor is optimized for low on-resistance and minimal gate charge. The Chip-scaled PowerFLAT™ package allows a significant board space saving, still boosting the performance.

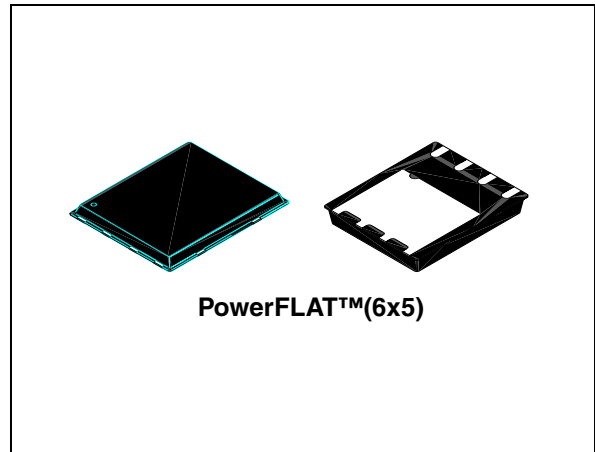


Figure 1. Internal schematic diagram

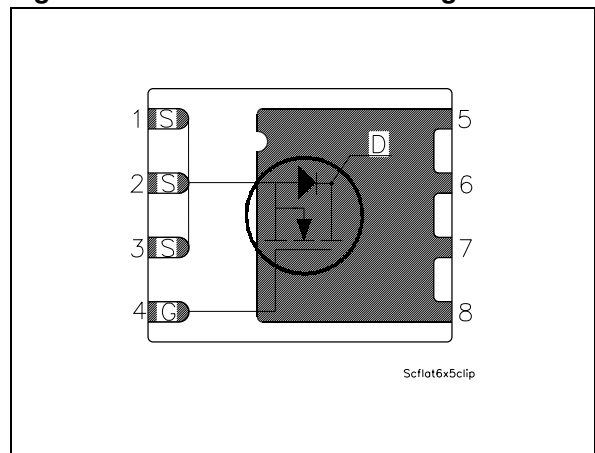


Table 1. Device summary

Order code	Marking	Package	Packaging
STL60NH3LL	L60NH3LL	PowerFLAT™ (6 x 5)	Tape & reel

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	30	V
$V_{GS}$	Gate-source voltage	$\pm 16$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	30	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	30	A
$I_D^{(2)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	16	A
$I_{DM}^{(3)}$	Drain current (pulsed)	64	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25^\circ\text{C}$	60	W
$P_{TOT}^{(2)}$	Total dissipation at $T_C = 25^\circ\text{C}$	4	W
	Derating factor	0.03	W/ $^\circ\text{C}$
$T_j$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. The value is rated according  $R_{thj-C}$  and is limited by wire bonding.
2. This value is according  $R_{thj-pcb}$
3. Pulse width limited by safe operating area

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (drain) Max	2.08	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb Max	31.3	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2 oz. Cu.,  $t < 10\text{sec}$

**Table 4. Avalanche data**

Symbol	Parameter	Value	Unit
$I_{AV}$	Not-repetitive avalanche current	7.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$ , $I_d = I_{AV}$ )	150	mJ

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}\text{C}$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0$	30			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ , $V_{DS} = \text{Max rating}$ , @ $125^{\circ}\text{C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{DS} = \pm 16\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 8\text{ A}$ $V_{GS} = 4.5\text{ V}$ , $I_D = 8\text{ A}$		0.0065 0.0075	0.0085 0.0105	$\Omega$ $\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS}=25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS}=0$		1810 565 41		pF pF pF
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 15\text{ V}$ , $I_D = 16\text{ A}$ , $V_{GS} = 4.5\text{ V}$ (see Figure 16)		18 4.8 5.3	24	nC nC nC
$R_G$	Gate input resistance	$f=1\text{ MHz}$ gate DC bias = 0 test signal level = 20 mV open drain	0.5	1.5	3	$\Omega$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Rise time	$V_{DD} = 15\text{ V}$ , $I_D = 8\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ , (see Figure 15)		8 65		ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time Fall time	$V_{DD} = 15\text{ V}$ , $I_D = 8\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ , (see Figure 15)		30 20		ns ns

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$I_{SD}$	Source-drain current				16	A
$I_{SDM}$	Source-drain current (pulsed)				64	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 16\text{ A}$ , $V_{GS} = 0$			1.3	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 16\text{ V}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 20\text{ V}$ , $T_j = 25^\circ\text{C}$ (see Figure 17)		22 32 1.9		ns nC A

1. Pulsed: Pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

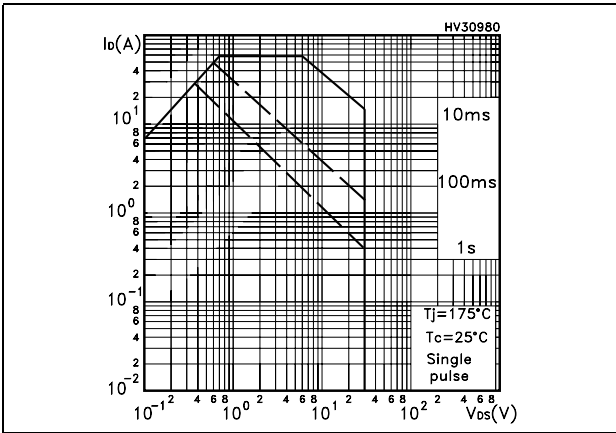


Figure 3. Thermal impedance

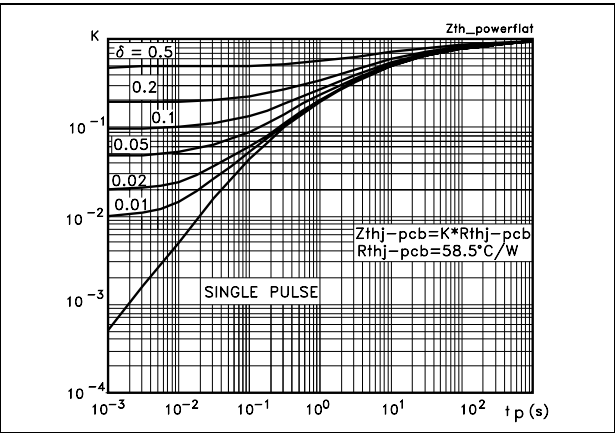


Figure 4. Output characteristics

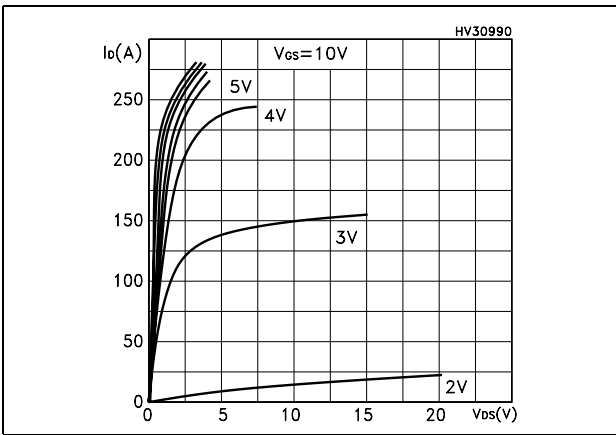


Figure 5. Transfer characteristics

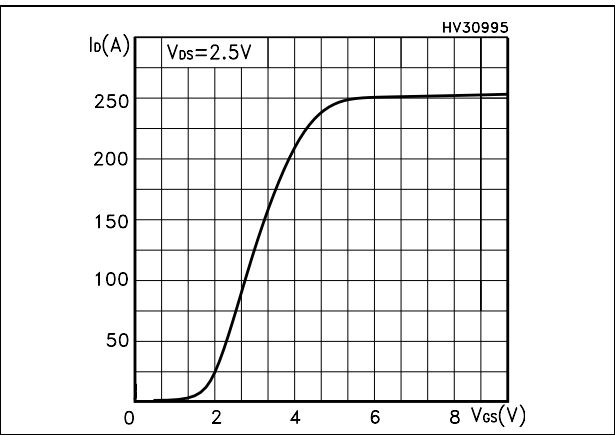


Figure 6. Normalized  $B_{V_{DSS}}$  vs. temperature

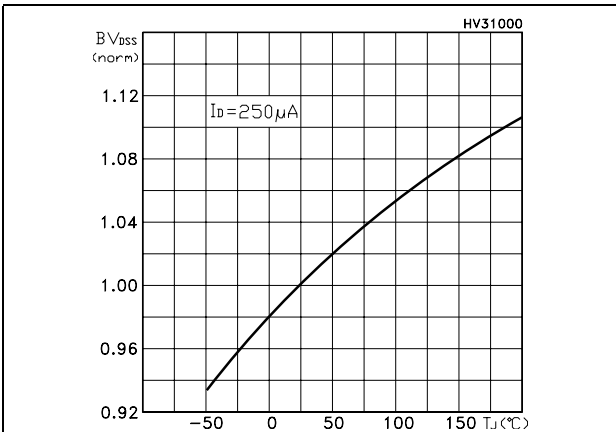


Figure 7. Static drain-source on resistance

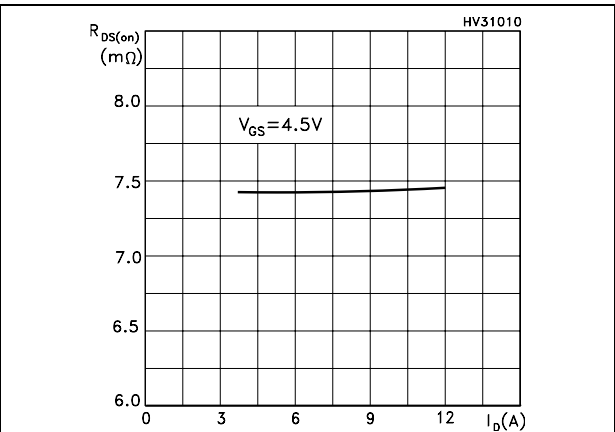


Figure 8. Gate charge vs. gate-source voltage Figure 9. Capacitance variations

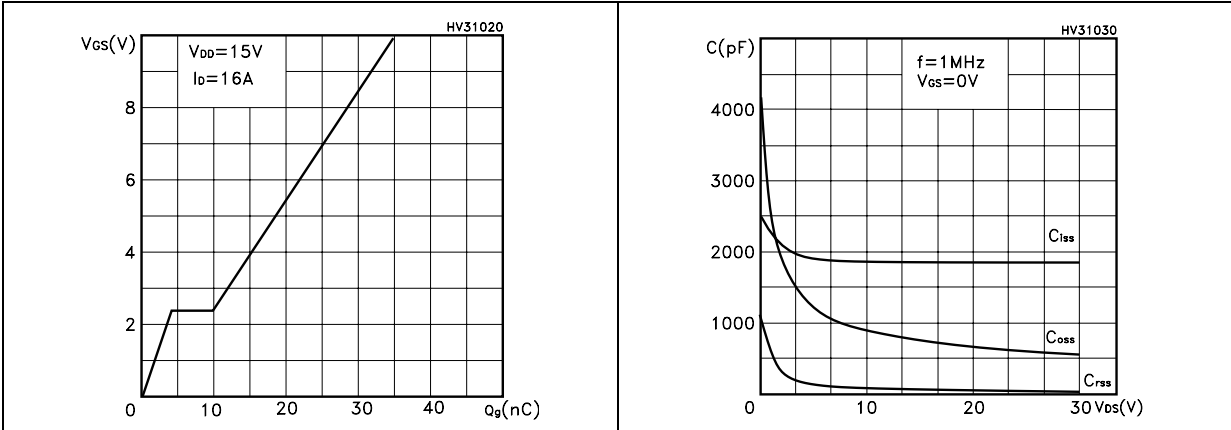


Figure 10. Normalized gate threshold voltage vs. temperature Figure 11. Normalized on resistance vs. temperature

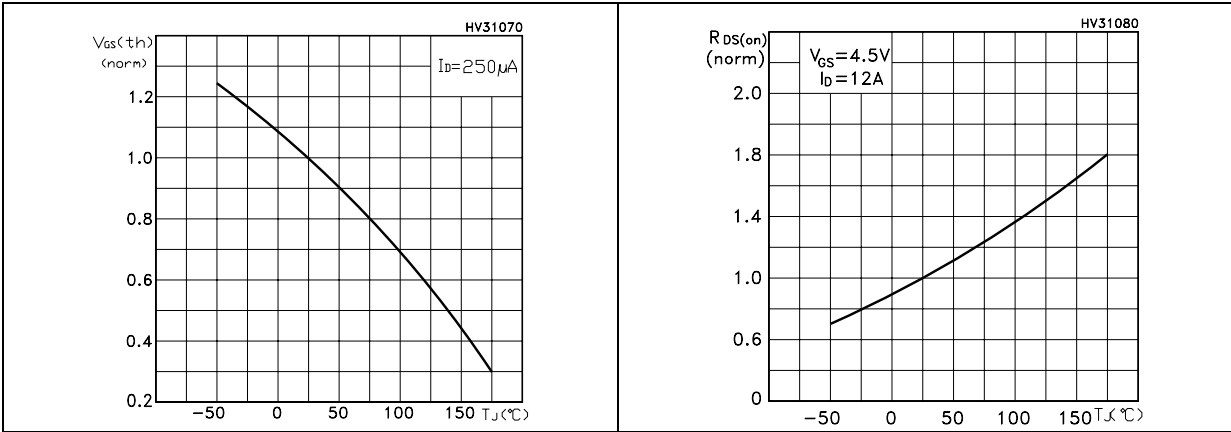


Figure 12. Source-drain diode forward characteristics

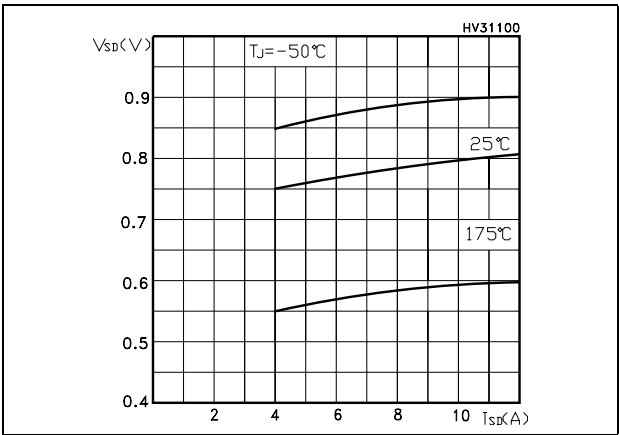
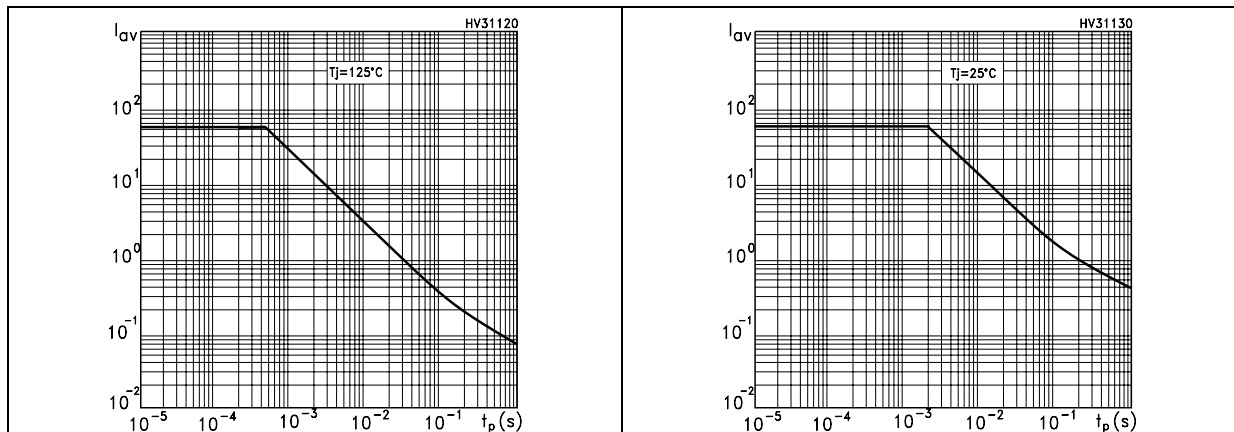


Figure 13. Allowable  $I_{AV}$  vs Time in Avalanche Figure 14. Allowable  $I_{AV}$  vs Time in Avalanche

The previous curve gives the single pulse safe operating area for unclamped inductive loads under the following conditions:

$$P_{D(AVE)} = 0.5 \cdot (1.3 \cdot BV_{DSS} \cdot I_{AV})$$

$$E_{AS(AR)} = P_{D(AVE)} \cdot t_{AV}$$

Where:

$I_{AV}$  is the allowable current in avalanche

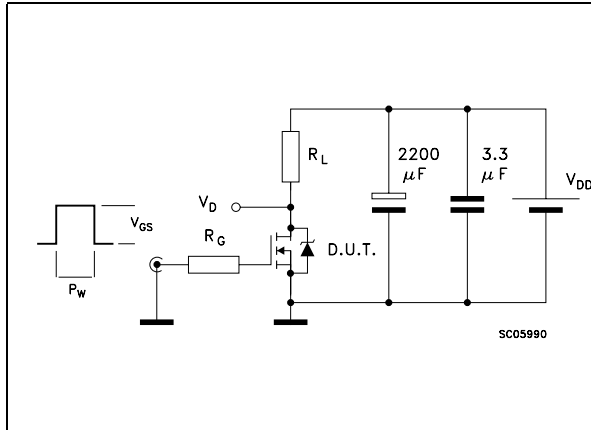
$P_{D(AVE)}$  is the average power dissipation in avalanche (single pulse)

$t_{AV}$  is the time in avalanche

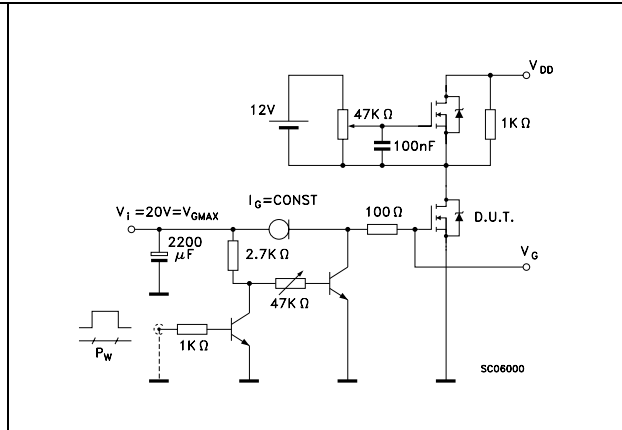


### 3 Test circuit

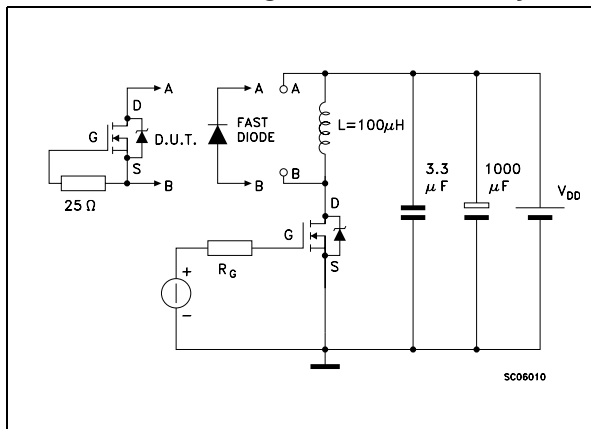
**Figure 15. Switching times test circuit for resistive load**



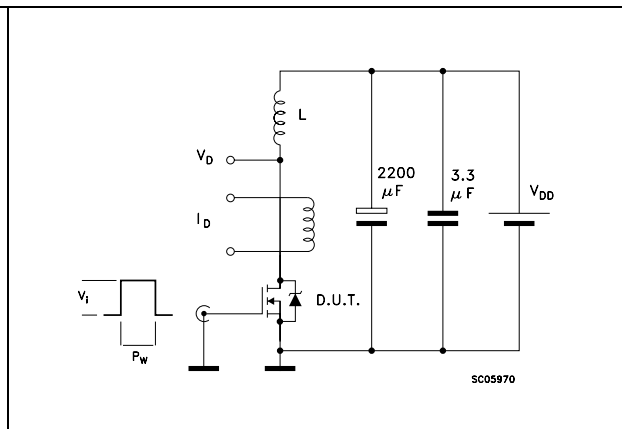
**Figure 16. Gate charge test circuit**



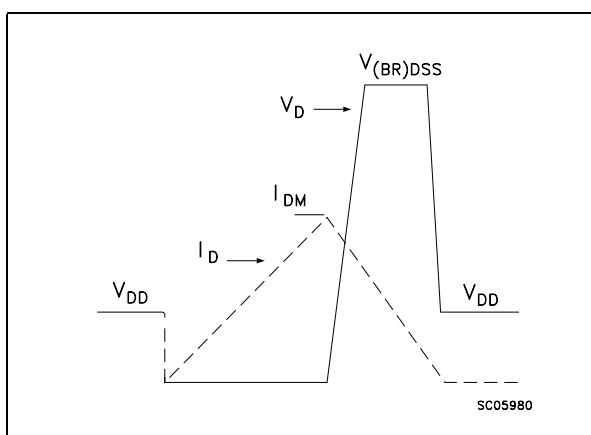
**Figure 17. Test circuit for inductive load switching and diode recovery times**



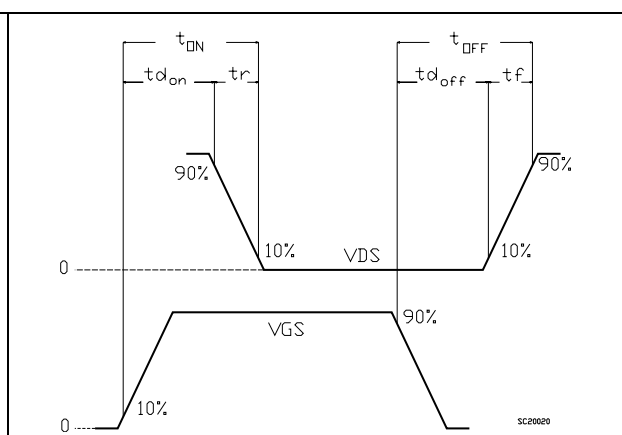
**Figure 18. Unclamped inductive load test circuit**



**Figure 19. Unclamped inductive waveform**



**Figure 20. Switching time waveform**

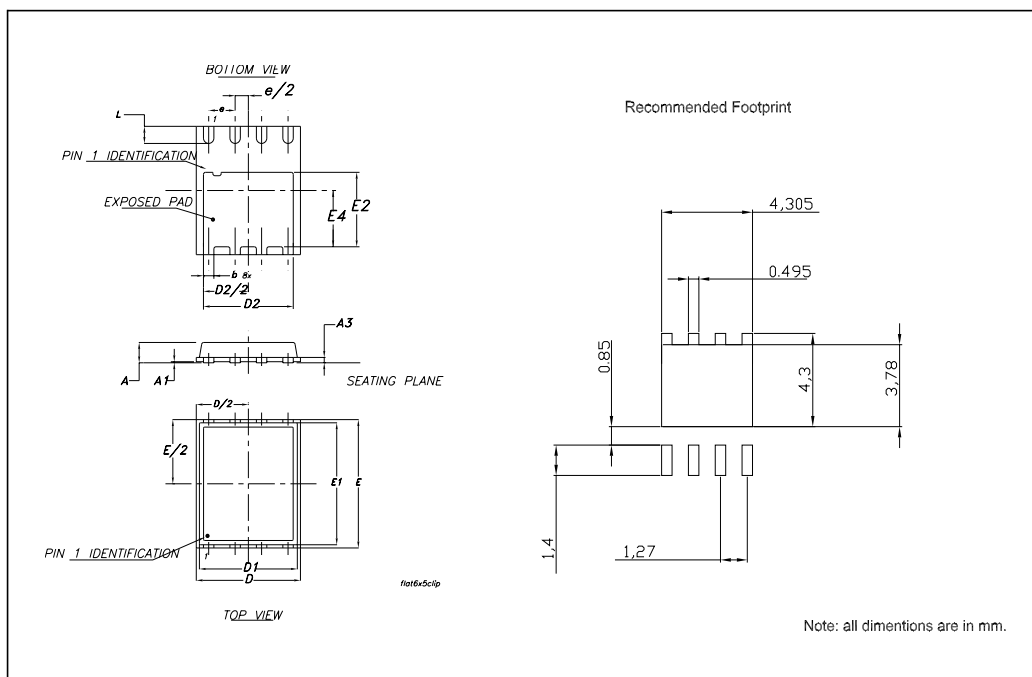


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

## PowerFLAT™ (6x5) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80	0.83	0.93	0.031	0.032	0.036
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.007	
b	0.35	0.40	0.47	0.013	0.015	0.018
D		5.00			0.196	
D1		4.75			0.187	
D2	4.15	4.20	4.25	0.163	0.165	0.167
E		6.00			0.236	
E1		5.75			0.226	
E2	3.43	3.48	3.53	0.135	0.137	0.139
E4	2.58	2.63	2.68		0.103	0.105
e		1.27			0.050	
L	0.70	0.80	0.90	0.027	0.031	0.035



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
10-Jan-2006	1	First release
14-Apr-2006	2	New footprint
03-Jul-2006	3	New Ecopack label
01-Aug-2006	4	Modified <i>Figure 2.</i> and <i>Figure 3.</i>
05-Sep-2006	5	New template, no content change
11-Dec-2007	6	Added <i>Table 4: Avalanche data</i>

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