



FLASH-ROM MODULE 16MByte (4M x 32Bit), 72-Pin SIMM, 5V
Part No. HMF4M32M8G

GENERAL DESCRIPTION

The HMF4M32M8G is a high-speed flash read only memory (FROM) module containing 8,388,608 words organized in a x32bit configuration. The module consists of eight 2M x 8bit FROM mounted on a 72 -pin, double-sided, FR4-printed circuit board. Commands are written to the command register using standard microprocessor write timings.

Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0V flash or EPROM devices.

Eight chip enable inputs, (/CE_UU1, /CE_UM1, /CE_LM1, /CE_LL1, /CE_UU2, /CE_UM2, /CE_LM2, CE_LL2) are used to enable the module's 4 bytes independently. Outputs enable (/OE) and write enable (/WE) can set the memory input and output. When FROM module is disable condition the module is becoming power standby mode, system designer can get low - power design. All module components may be powered from a single +5V DC power supply and all inputs and outputs are TTL-compatible.

FEATURES

w Part Identifications

HMF4M32M8G : 16Mbyte, 72-pin SIMM, Gold

HMF4M32M8 : 16Mbyte, 72-pin SIMM, Solder

w Access time : 75, 90 and 120ns

w High-density 16MByte design

w High-reliability, low-power design

w Single + 5V $\pm$ 0.5V power supply

w Easy memory expansion

w All inputs and outputs are TTL-compatible

w FR4-PCB design

w Low profile 72-pin SIMM

w Minimum 1,000,000 write/erase cycle

w Sectors erase architecture

w Sector group protection

w Temporary sector group unprotection

w The used device is Am29F016B or MBM29F016-90PFTN

PIN ASSIGNMENT

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	25	A20	49	DQ17
2	A3	26	DQ8	50	DQ18
3	A2	27	DQ9	51	DQ22
4	A1	28	DQ10	52	DQ21
5	A0	29	/CE-LM2	53	DQ20
6	Vcc	30	Vcc	54	DQ19
7	A11	31	/CE-LM1	55	A19
8	/OE	32	DQ15	56	A15
9	A10	33	DQ14	57	A12
10	/RESET	34	DQ13	58	A7
11	/CE-LL2	35	DQ12	59	Vcc
12	/CE-LL1	36	DQ11	60	A8
13	DQ7	37	A18	61	A9
14	DQ0	38	A16	62	DQ24
15	DQ1	39	Vss	63	DQ25
16	DQ2	40	A6	64	DQ26
17	DQ6	41	/RY_BY	65	/CE-UU2
18	DQ5	42	A5	66	/CE-UU1
19	DQ4	43	A4	67	DQ31
20	DQ3	44	Vcc	68	DQ30
21	/WE	45	/CE-UM2	69	DQ29
22	A17	46	/CE-UM1	70	DQ28
23	A14	47	DQ23	71	DQ27
24	A13	48	DQ16	72	Vss

OPTIONS

MARKING

w Timing

75ns access -75

90ns access -90

120ns access -120

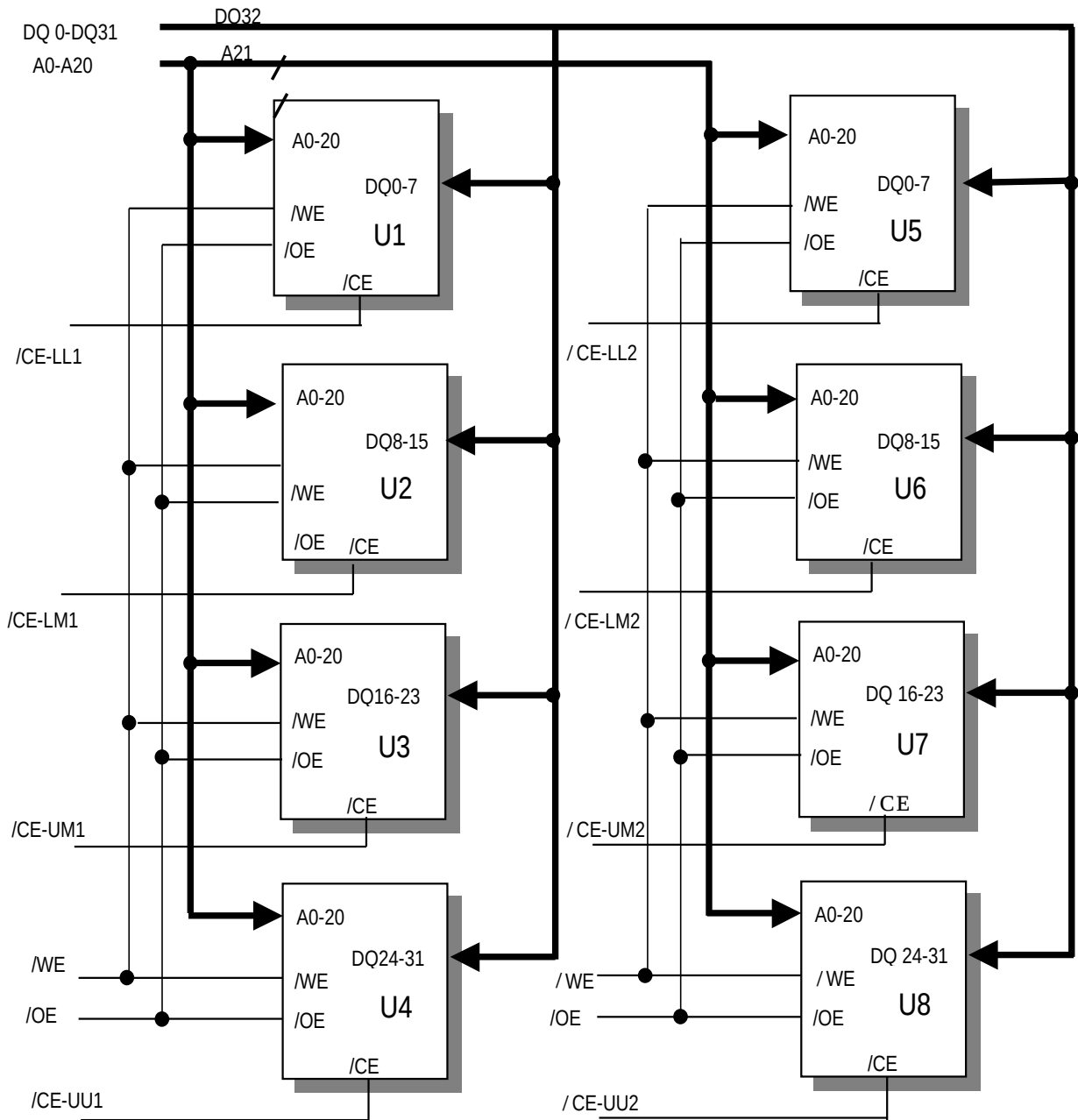
w Packages

72-pin SIMM M

72-PIN SIMM

TOP VIEW

Functional Block Diagram



TRUTH TABLE

MODE	/OE	/CE	/WE	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
READ	L	L	H	Q	ACTIVE
WRITE or ERASE	X	L	L	D	ACTIVE

NOTE: X means don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage with respect to ground all other pins	$V_{IN,OUT}$	-2.0V to +7.0V
Voltage with respect to ground V_{CC}	V_{CC}	-2.0V to +7.0V
Storage Temperature	T_{STG}	-65°C to +125°C
Operating Temperature	T_A	-55°C to +125°C

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP.	MAX
V_{CC} for $\pm 10\%$ device Supply Voltages	V_{CC}	4.5V		5.5V
Ground	V_{SS}	0	0	0

DC AND OPERATING CHARACTERISTICS ($0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$; $V_{CC} = 5V \pm 0.5V$)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNITS
Input Leakage Current	$V_{CC}=V_{CC\text{ max}}, V_{IN}= \text{GND to } V_{CC}$	I_{L1}		± 1.0	μA
Output Leakage Current	$V_{CC}=V_{CC\text{ max}}, V_{OUT}= \text{GND to } V_{CC}$	I_{L0}		± 1.0	μA
Output High Voltage	$I_{OH} = -2.5\text{mA}, V_{CC} = V_{CC\text{ min}}$	V_{OH}	2.4		V
Output Low Voltage	$I_{OL} = 12\text{mA}, V_{CC} = V_{CC\text{ min}}$	V_{OL}		0.45	V
V_{CC} Active Current for Read(1)	$/CE = V_{IL}, /OE = V_{IH}$	I_{CC1}		40	mA
V_{CC} Active Current for Program or Erase(2)	$/CE = V_{IL}, /OE = V_{IH}$	I_{CC2}		60	mA
V_{CC} Standby Current	$/CE = V_{IH}$	I_{CC3}		1.0	mA
Low V_{CC} Lock-Out Voltage		V_{LKO}	3.2	4.2	V

Notes:

1. The I_{CC} current listed is typically less than 2mA/MHz, with $/OE$ at V_{IH} .
2. I_{CC} active while embedded algorithm (program or erase) is in progress
3. Maximum I_{CC} current specifications are tested with $V_{CC}=V_{CC\text{ max}}$

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	LIMITS			UNIT	COMMENTS
	MIN.	TYP.	MAX.		
Sector Erase Time	-	1	8	sec	Excludes 00H programming prior to erasure
Byte Programming Time	-	7	300	μs	Excludes system-level overhead
Chip Programming Time	-	14.4	43.2	sec	Excludes system-level overhead

TSOP CAPACITANCE

PARAMETER SYMBOL	PARAMETER DESCRIPTION	TEST SETUP	MIN	MAX	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0	6	7.5	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0	8.5	12	pF
C _{IN2}	Control Pin Capacitance	V _{IN} = 0	7.5	9	pF

Notes : Test conditions T_A = 25° C, f=1.0 MHz.

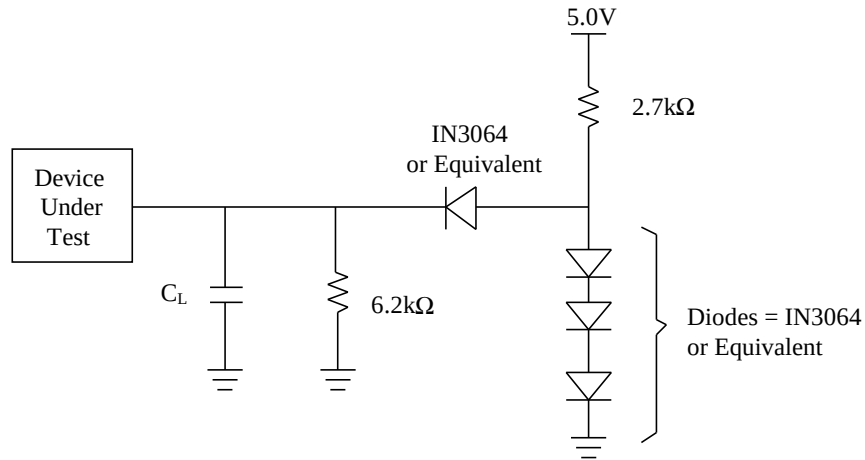
AC CHARACTERISTICS**u Read Only Operations Characteristics**

PARAMETER SYMBOLS		DESCRIPTION	TEST SETUP		-75	-90	UNIT
JEDEC	STANDARD						
t _{AVAV}	t _{RC}	Read Cycle Time		Min	70	90	ns
t _{AVQV}	t _{ACC}	Address to Output Delay	/CE = V _{IL} /OE = V _{IL}	Max	70	90	ns
t _{ELOV}	t _{CE}	Chip Enable to Output Delay	/OE = V _{IL}	Max	70	90	ns
t _{GLOV}	t _{OE}	Chip Enable to Output Delay		Max	40	40	ns
t _{EHQZ}	t _{DF}	Chip Enable to Output High-Z		Max	20	20	ns
t _{GHQZ}	t _{DF}	Output Enable to Output High-Z		Max	20	20	ns
t _{AXQX}	t _{QH}	Output Hold Time From Addresses, /CE or /OE, Whichever Occurs First		Min	0	0	ns

TEST SPECIFICATIONS

TEST CONDITION	ALL SPEED OPTIONS	UNIT
Output load	1TTL gate	

Output load capacitance, C_L (Including jig capacitance)	100	pF
Input rise and fall times	20	ns
Input pulse levels	0.45-2.4	V
Input timing measurement reference levels	0.8	V
Output timing measurement reference levels	2.0	V



Note : C_L = 100pF including jig capacitance

u Erase/Program Operations

PARAMETER SYMBOLS		DESCRIPTION		-75	-90	UNIT
JEDEC	STANDARD					
t_{AVAV}	t_{WC}	Write Cycle Time	Min	70	90	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	40	45	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	40	45	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0	0	ns
	t_{OES}	Output Enable Setup Time	Min	0	0	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write	Min	0	0	ns
t_{ELWL}	t_{CS}	/CE Setup Time	Min	0	0	ns
t_{WHEH}	t_{CH}	/CE Hold Time	Min	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	40	45	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Typ	7	7	μs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note1)	Typ	1	1	sec

	t_{VCS}	Vcc set up time	Min	50	50	μs
--	-----------	-----------------	-----	----	----	---------

Notes :

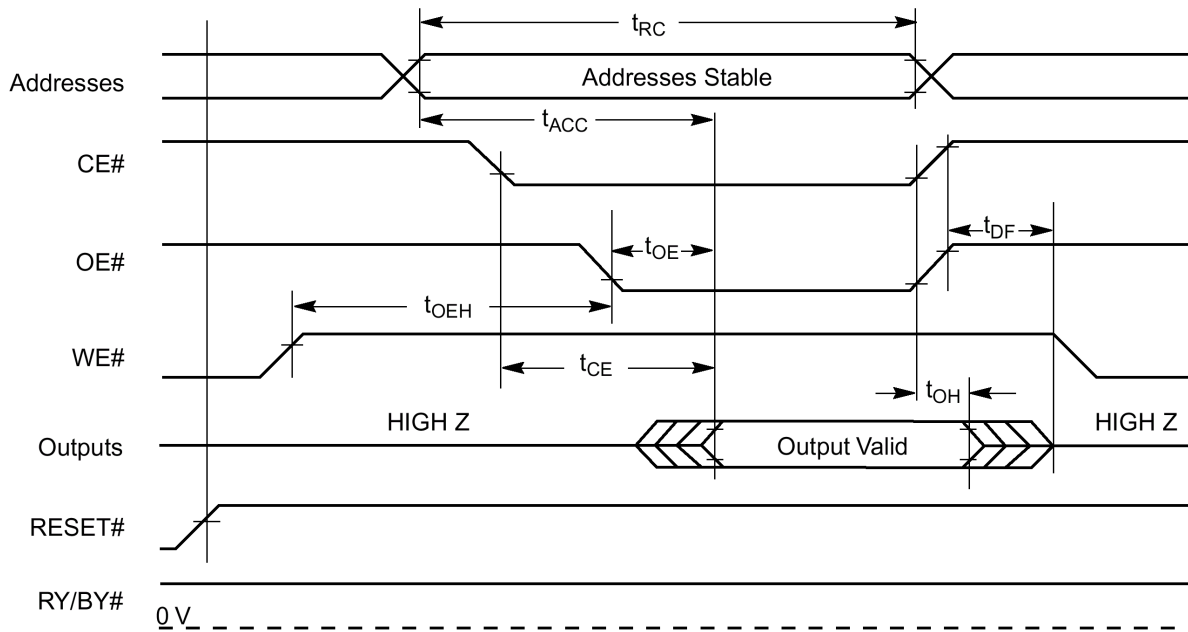
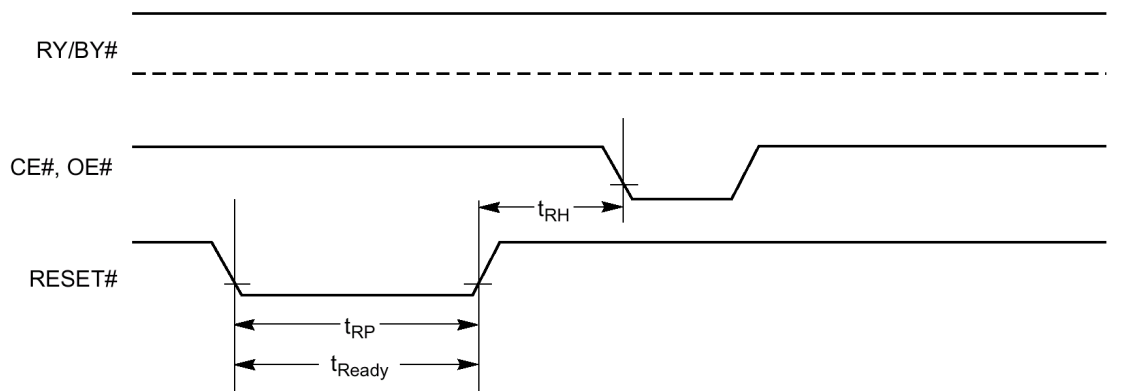
1. This does not include the preprogramming time
2. This timing is only for Sector Protect operations

u Erase/Program Operations**Alternate /CE Controlled Writes**

PARAMETER SYMBOLS		DESCRIPTION		-75	-90	UNIT
JEDEC	STANDARD					
t_{AVAV}	t_{WC}	Write Cycle Time	Min	70	90	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	40	45	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	40	45	ns
t_{WHDx}	t_{DH}	Data Hold Time	Min	0	0	ns
	t_{OES}	Output Enable Setup Time	Min	0	0	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write	Min	0	0	ns
t_{ELWL}	t_{CS}	/CE Setup Time	Min	0	0	ns
t_{WHEH}	t_{CH}	/CE Hold Time	Min	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	40	45	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Typ	7	7	μs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note1)	Typ	1	1	sec

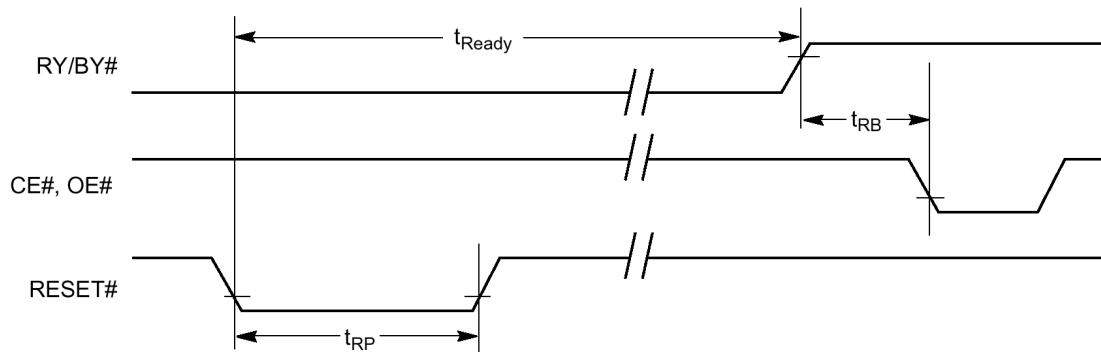
Notes :

1. This does not include the preprogramming time
2. This timing is only for Sector Protect operations

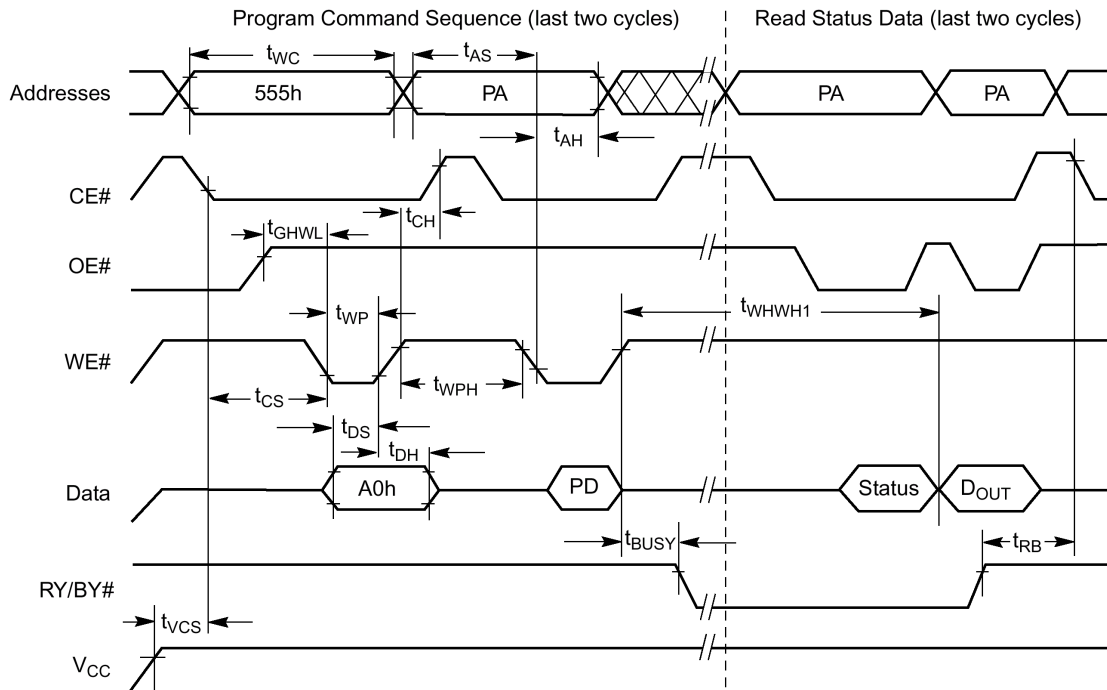
u READ OPERATIONS TIMING**u RESET TIMING**

Reset Timings NOT during Embedded Algorithms

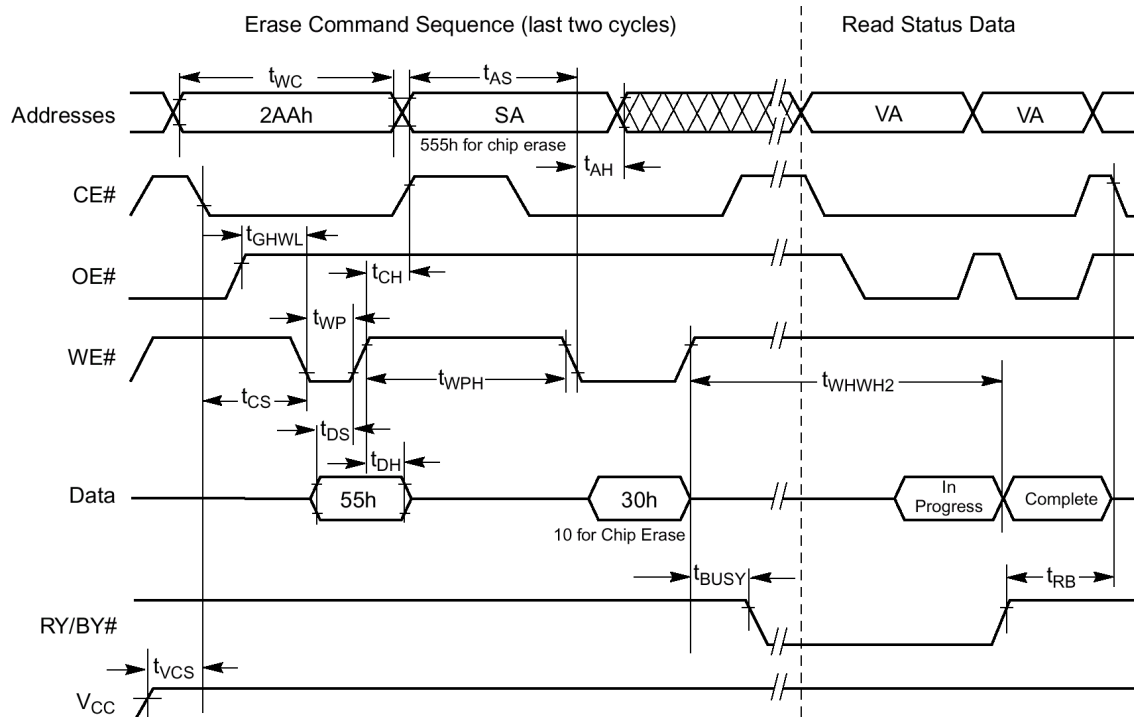
Reset Timings during Embedded Algorithms

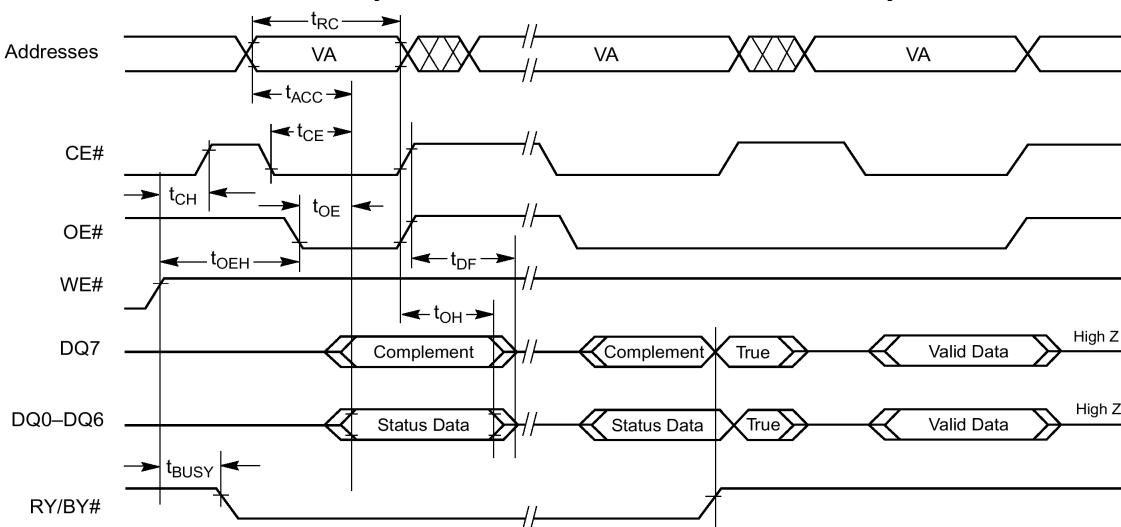
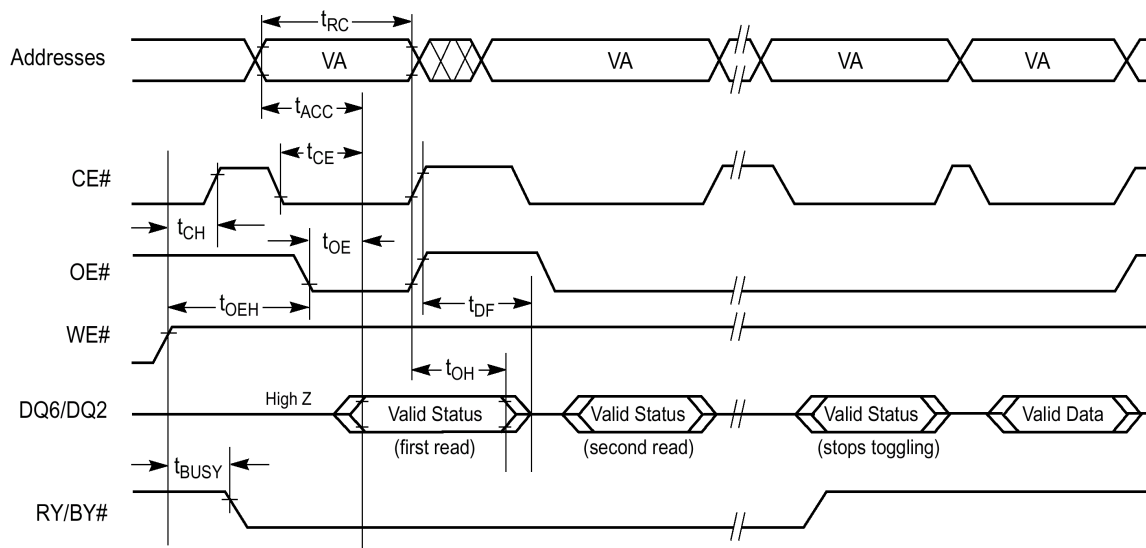


u PROGRAM OPERATIONS TIMING



u CHIP/SECTOR ERASE OPERATION TIMINGS



u DATA# POLLING TIMES(DURING EMBEDDED ALGORITHMS)**u TOGGLE# BIT TIMINGS (DURING EMBEDDED ALGORITHMS)**

The timing diagram illustrates the sequence of signals for Sector Protect/Unprotect and Verify operations. The signals shown are RESET#, SA, A6, A1, A0, Data, CE#, WE#, and OE#.

- RESET#**: A horizontal line at V_{IH} level, with a dashed line at V_{IP} level.
- SA, A6, A1, A0**: Address signals. The diagram shows a transition from a low state to a high state labeled "Valid*".
- Data**: Data bus signals. The diagram shows a transition from a low state to a high state labeled "60h".
- CE#**: Chip Enable signal. A pulse width of $1\ \mu s$ is indicated. The diagram shows a transition from a high state to a low state.
- WE#**: Write Enable signal. The diagram shows a transition from a high state to a low state.
- OE#**: Output Enable signal. The diagram shows a transition from a high state to a low state.

The diagram is divided into two main sections:

- Sector Protect/Unprotect**: This section shows the data bus being set to "60h" and the CE# signal being pulsed low for $1\ \mu s$. The WE# signal is also pulsed low.
- Verify**: This section shows the data bus being set to "40h" and the CE# signal being pulsed low. The WE# signal is also pulsed low. The status of the operation is indicated by the "Status" signal.

Timing specifications for the Verify operation are provided:

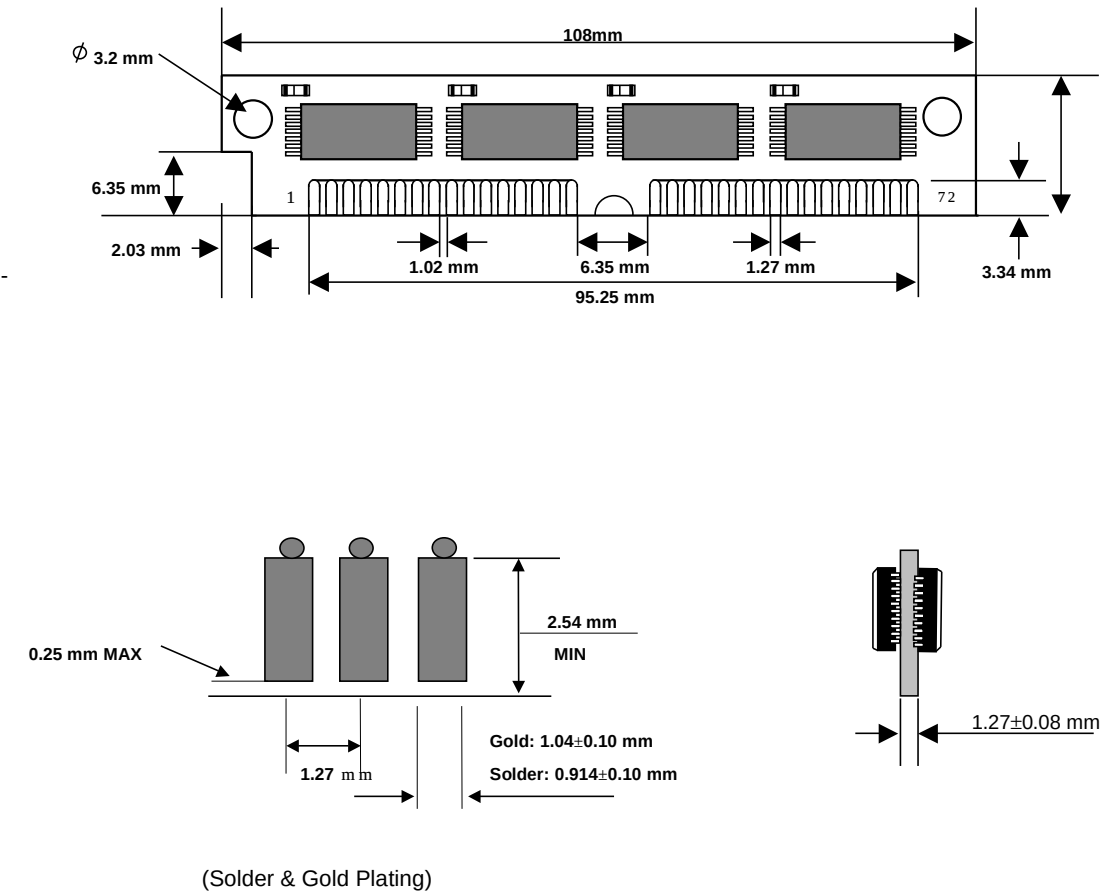
- Sector Protect: $150\ \mu s$
- Sector Unprotect: $15\ ms$

The timing diagram illustrates the sequence of operations for the 28C64 EPROM. It includes the following signals and parameters:

- Addresses:** Shows the address bus with specific points for program (55), sector erase (PA), and chip erase (55). Timing parameters t_{WC} , t_{AS} , and t_{AH} are indicated.
- WE# (Write Enable):** Shows the pulse width t_{WH} and the time t_{GHEL} from the start of the address to the start of the data output.
- OE# (Output Enable):** Shows the pulse width $t_{WHWH1 \text{ or } 2}$.
- CE# (Chip Enable):** Shows the pulse width t_{WS} and the time t_{CPH} from the start of the address to the start of the data output.
- Data:** Shows the data bus with the time t_{DS} from the start of the address to the start of the data output, and the time t_{DH} from the start of the address to the start of the data output. The data output is shown as $DQ7\#$ and D_{OUT} .
- RESET#:** Shows the reset signal.
- RY/BY#:** Shows the read/write/byte select signal.

Additional labels include "Data# Polling" and "PA" (Program Address).

PACKAGE DIMENSIONS



ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	SPEED
HMF4M32M8G-75	16MByte	4MX 32bit	72 Pin-SIMM	8EA	5V	70ns
HMF4M32M8G-90	16MByte	4MX 32bit	72 Pin-SIMM	8EA	5V	90ns
HMF4M32M8G-120	16MByte	4MX 32bit	72 Pin-SIMM	8EA	5V	120ns