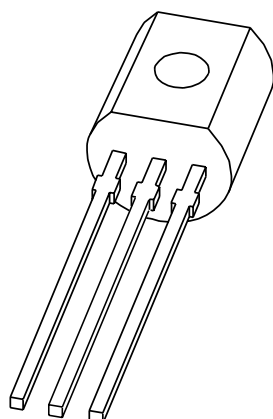


DATA SHEET



BSN254; BSN254A N-channel enhancement mode vertical D-MOS transistor

Product specification
Supersedes data of 1997 Jun 23

2002 Feb 19

N-channel enhancement mode vertical D-MOS transistor

BSN254; BSN254A

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown
- Low $R_{DS(on)}$

APPLICATIONS

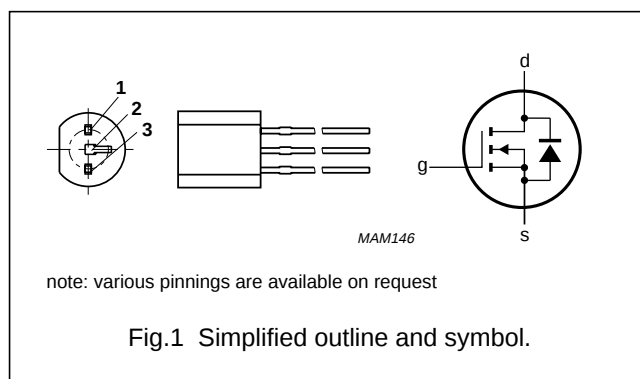
- Line current interruptor in telephone sets
- Relay, high-speed and line transformer drivers.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT54 (TO-92) variant package.

PINNING - SOT54 variant

PIN	DESCRIPTION	
	BSN254	BSN254A
1	gate	source
2	drain	gate
3	source	drain



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		—	250	V
I_D	drain current (DC)		—	310	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$	—	1	W
$R_{DS(on)}$	drain-source on-state resistance	$I_D = 300\text{ mA}; V_{GS} = 10\text{ V}$	2.8	5	Ω
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}; V_{DS} = V_{GS}$	—	2	V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		—	250	V
V_{GSO}	gate-source voltage (DC)	open drain	—	± 20	V
I_D	drain current (DC)		—	310	mA
I_{DM}	peak drain current		—	1.25	A
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}; \text{note 1}$	—	1	W
T_{stg}	storage temperature		−55	+150	°C
T_j	junction temperature		—	150	°C

Note

1. Device mounted on a printed-circuit board; maximum lead length 4 mm; mounting pad for drain lead minimum $10 \times 10\text{ mm}$.

N-channel enhancement mode vertical D-MOS transistor

BSN254; BSN254A

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient; note 1	125	K/W

Note

1. Device mounted on a printed-circuit board; maximum lead length 4 mm; mounting pad for drain lead minimum 10×10 mm.

CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\text{ }\mu\text{A}$; $V_{GS} = 0$	250	–	–	V
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 20\text{ V}$; $V_{DS} = 0$	–	–	± 100	nA
V_{GSth}	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$	0.8	–	2	V
R_{DSon}	drain-source on-state resistance	$I_D = 20\text{ mA}$; $V_{GS} = 2.4\text{ V}$	–	–	7.5	Ω
		$I_D = 300\text{ mA}$; $V_{GS} = 10\text{ V}$	–	2.8	5	Ω
I_{DSS}	drain-source leakage current	$V_{DS} = 200\text{ V}$; $V_{GS} = 0$	–	–	1	μA
$ Y_{fs} $	transfer admittance	$I_D = 300\text{ mA}$; $V_{DS} = 25\text{ V}$	200	600	–	mS
C_{iss}	input capacitance	$V_{DS} = 25\text{ V}$; $V_{GS} = 0$; $f = 1\text{ MHz}$	–	100	120	pF
C_{oss}	output capacitance	$V_{DS} = 25\text{ V}$; $V_{GS} = 0$; $f = 1\text{ MHz}$	–	21	30	pF
C_{rss}	feedback capacitance	$V_{DS} = 25\text{ V}$; $V_{GS} = 0$; $f = 1\text{ MHz}$	–	10	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$I_D = 250\text{ mA}$; $V_{DD} = 50\text{ V}$; $V_{GS} = 0$ to 10 V	–	6	10	ns
t_{off}	turn-off time	$I_D = 250\text{ mA}$; $V_{DD} = 50\text{ V}$; $V_{GS} = 10$ to 0 V	–	47	60	ns

N-channel enhancement mode
vertical D-MOS transistor

BSN254; BSN254A

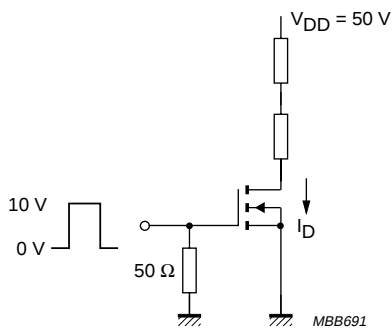


Fig.2 Switching times test circuit.

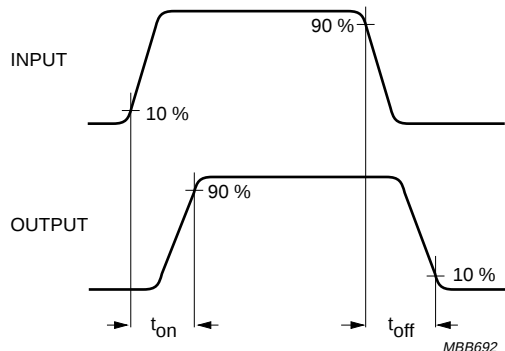


Fig.3 Input and output waveforms.

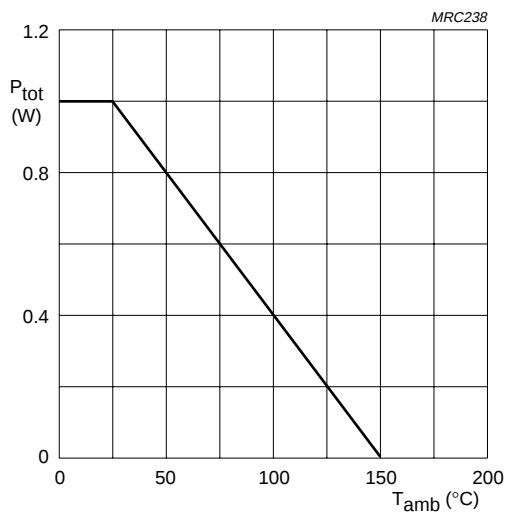
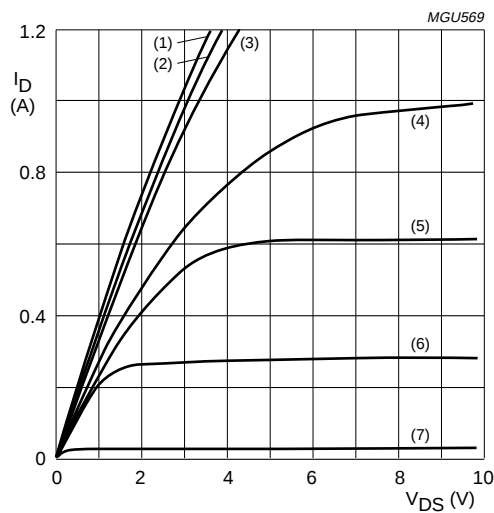


Fig.4 Power derating curve.



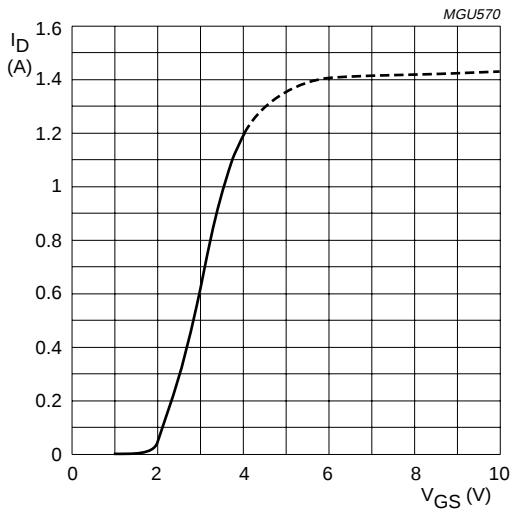
$T_j = 25\text{ }^{\circ}\text{C}$.

(1) $V_{GS} = 10\text{ V}$.	(4) $V_{GS} = 3.5\text{ V}$.	(7) $V_{GS} = 2\text{ V}$.
(2) $V_{GS} = 5\text{ V}$.	(5) $V_{GS} = 3\text{ V}$.	
(3) $V_{GS} = 4\text{ V}$.	(6) $V_{GS} = 2.5\text{ V}$.	

Fig.5 Typical output characteristics.

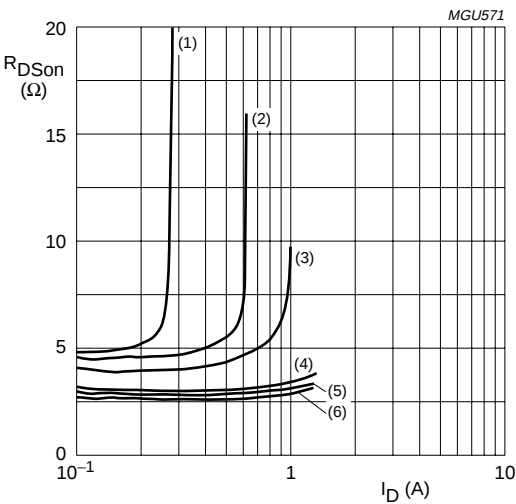
N-channel enhancement mode
vertical D-MOS transistor

BSN254; BSN254A



$V_{DS} = 10\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$.

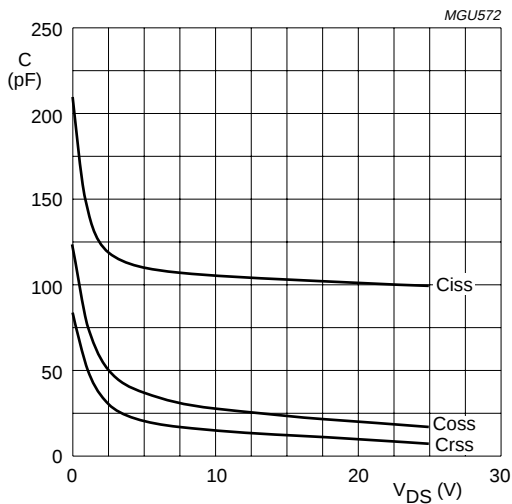
Fig.6 Typical transfer characteristics.



$T_j = 25\text{ }^\circ\text{C}$.

- | | | |
|-------------------------------|-------------------------------|------------------------------|
| (1) $V_{GS} = 2.5\text{ V}$. | (3) $V_{GS} = 3.5\text{ V}$. | (5) $V_{GS} = 5\text{ V}$. |
| (2) $V_{GS} = 3\text{ V}$. | (4) $V_{GS} = 4\text{ V}$. | (6) $V_{GS} = 10\text{ V}$. |

Fig.7 Drain-source on-state resistance as a function of drain current; typical values.

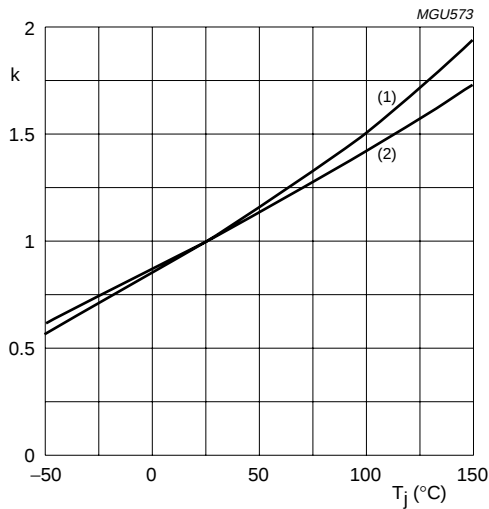


$V_{GS} = 0$; $f = 1\text{ MHz}$; $T_j = 25\text{ }^\circ\text{C}$.

Fig.8 Input, output and feedback capacitance as functions of drain-source voltage; typical values.

N-channel enhancement mode
vertical D-MOS transistor

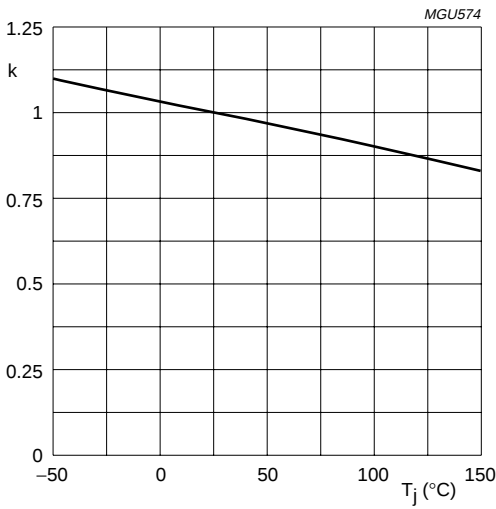
BSN254; BSN254A



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25^\circ\text{C}}$$

Typical R_{DSon} :
(1) $I_D = 250 \text{ mA}$; $V_{GS} = 10 \text{ V}$.
(2) $I_D = 20 \text{ mA}$; $V_{GS} = 2.4 \text{ V}$.

Fig.9 Temperature coefficient of drain-source on-state resistance; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25^\circ\text{C}}$$

Typical V_{GSth} at 1 mA.

Fig.10 Temperature coefficient of gate-source threshold voltage; typical values.

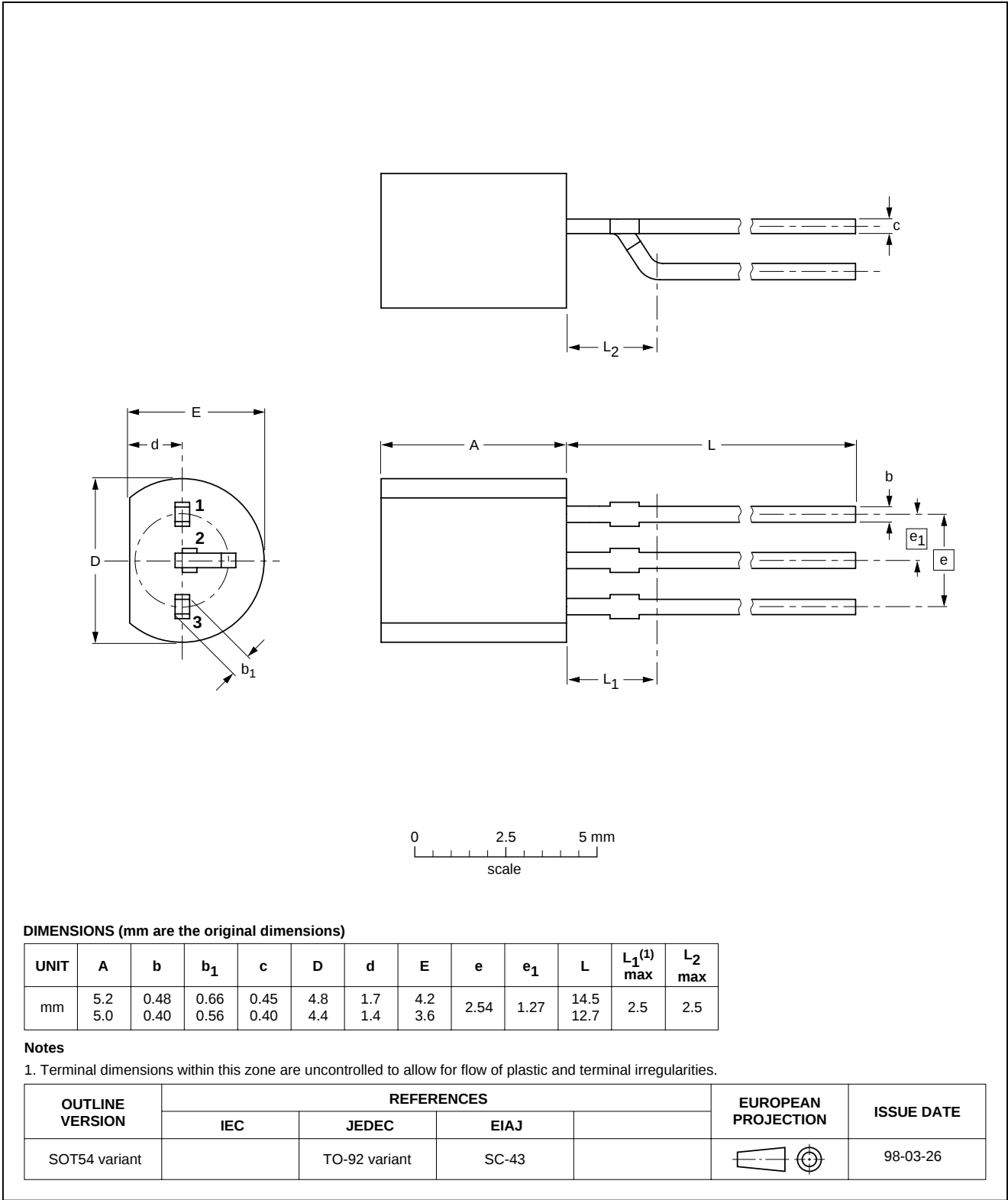
N-channel enhancement mode
vertical D-MOS transistor

BSN254; BSN254A

PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads (on-circle)

SOT54 variant



N-channel enhancement mode vertical D-MOS transistor

BSN254; BSN254A

DATA SHEET STATUS

DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

N-channel enhancement mode
vertical D-MOS transistor

BSN254; BSN254A

NOTES

N-channel enhancement mode
vertical D-MOS transistor

BSN254; BSN254A

NOTES

N-channel enhancement mode
vertical D-MOS transistor

BSN254; BSN254A

NOTES

Philips Semiconductors – a worldwide company

Contact information

For additional information please visit <http://www.semiconductors.philips.com>. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to: sales.addresses@www.semiconductors.philips.com.

© Koninklijke Philips Electronics N.V. 2002

SCA74

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

613510/03/pp12

Date of release: 2002 Feb 19

Document order number: 9397 750 09312

Let's make things better.

**Philips
Semiconductors**



PHILIPS