

PE84244

Military Operating Temperature Range

Product Description

The PE84244 MOSFET RF Switch is designed to cover a broad range of applications from DC to 3.0 GHz. This switch integrates on-board CMOS control logic with a low voltage CMOS compatible control input. Using a +3-volt nominal power supply voltage, a 1 dB compression point of +27 dBm can be achieved. The PE84244 also exhibits excellent isolation of 28 dB at 2.0 GHz and is offered in a small 8-lead MSOP package.

The PE84244 MOSFET RF Switch is manufactured in Peregrine's patented Ultra Thin Silicon (UTSi®) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

SPDT MOSFET RF Switch

Features

- Single +3.0-volt Power Supply
- Low Insertion loss: 0.70 dB up to 2.0 GHz
- High isolation of 39 dB at 1.0 GHz, 28 dB at 2.0 GHz, typical
- Typical 1 dB compression of +27 dBm
- Single-pin CMOS logic control
- Packaged in 8-lead MSOP

Figure 1. Functional Schematic Diagram

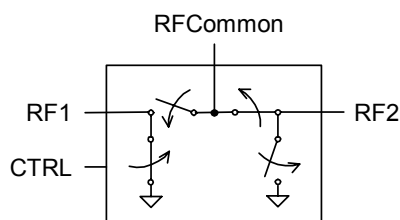


Figure 2. Package Type

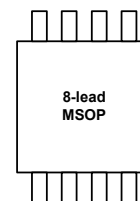
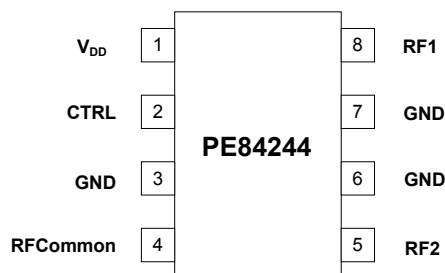


Table 1. Electrical Specifications -55 °C to +125 °C, V_{DD} = 3 V (Z_S = Z_L = 50 Ω)

| Parameter | Conditions | Minimum | Typical | Maximum | Units |
|----------------------------------|-----------------------------------|---------|---------|---------|------------------|
| Operation Frequency ¹ | | DC | | 3000 | MHz |
| Insertion Loss | 2000 MHz | | 0.7 | 0.95 | dB |
| Isolation – RFCommon to RF1/RF2 | 2000 MHz | 25 | 28 | | dB |
| Isolation – RF1 to RF2 | 2000 MHz | 24 | 27 | | dB |
| Return Loss | 2000 MHz | 18 | 25 | | dB |
| 'ON' Switching Time | CTRL to 0.1 dB final value, 2 GHz | | 200 | | ns |
| 'OFF' Switching Time | CTRL to 25 dB isolation, 2 GHz | | 90 | | ns |
| Video Feedthrough ² | | | 15 | | mV _{pp} |
| Input 1 dB Compression | 2000 MHz | 25 | 27 | | dBm |
| Input IP3 | 2000 MHz, 14dBm | 40 | 42 | | dBm |

Notes: 1. Device linearity will begin to degrade below 10 MHz.

2. The DC transient at the output of any port of the switch when the control voltage is switched from Low to High or High to Low in a 50 Ω test set-up, measured with 1ns risetime pulses and 500 MHz bandwidth.

Figure 3. Pin Configuration

Table 2. Pin Descriptions

| Pin No. | Pin Name | Description |
|---------|-----------------|---|
| 1 | V _{DD} | Nominal 3 V supply connection. A bypass capacitor (100 pF) to the ground plane should be placed as close as possible to the pin |
| 2 | CTRL | CMOS logic level: High = RFCommon to RF1 signal path Low = RFCommon to RF2 signal path |
| 3 | GND | Ground connection. Traces should be physically short and connected to ground plane for best performance. |
| 4 | RF Common | Common RF port for switch (Note 1) |
| 5 | RF2 | RF2 port (Note 1) |
| 6 | GND | Ground Connection. Traces should be physically short and connected to ground plane for best performance. |
| 7 | GND | Ground Connection. Traces should be physically short and connected to ground plane for best performance. |
| 8 | RF1 | RF1 port (Note 1) |

Note 1: All RF pins must be DC blocked with an external series capacitor or held at 0V_{DC}.

Table 3. Absolute Maximum Ratings

| Symbol | Parameter/Conditions | Min | Max | Units |
|------------------|--------------------------------|------|----------------------|-------|
| V _{DD} | Power supply voltage | -0.3 | 4.0 | V |
| V _I | Voltage on any input | -0.3 | V _{DD} +0.3 | V |
| T _{ST} | Storage temperature range | -65 | 150 | °C |
| T _{OP} | Operating temperature range | -55 | 125 | °C |
| P _{IN} | Input power (50Ω) | | 30 | dBm |
| V _{ESD} | ESD voltage (Human Body Model) | | 1500 | V |

Table 4. DC Electrical Specifications

| Parameter | Min | Typ | Max | Units |
|--|---------------------|-----|---------------------|-------|
| V _{DD} Power Supply Voltage | 2.7 | 3.0 | 3.3 | V |
| I _{DD} Power Supply Current V _{DD} = 3V, V _{CTRL} = 3V | | 250 | 500 | nA |
| Control Voltage High | 0.7xV _{DD} | | | V |
| Control Voltage Low | | | 0.3xV _{DD} | V |

Table 5. Control Logic Truth Table

| Control Voltage | Signal Path |
|------------------|-----------------|
| CTRL = CMOS High | RFCommon to RF1 |
| CTRL = CMOS Low | RFCommon to RF2 |

Electrostatic Discharge (ESD) Precautions

When handling this UTSi device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

Latch-Up Avoidance

Unlike conventional CMOS devices, UTSi CMOS devices are immune to latch-up.

Typical Performance Data -55 °C to +125 °C (Unless Otherwise Noted)

Figure 4. Insertion Loss – RFC to RF1

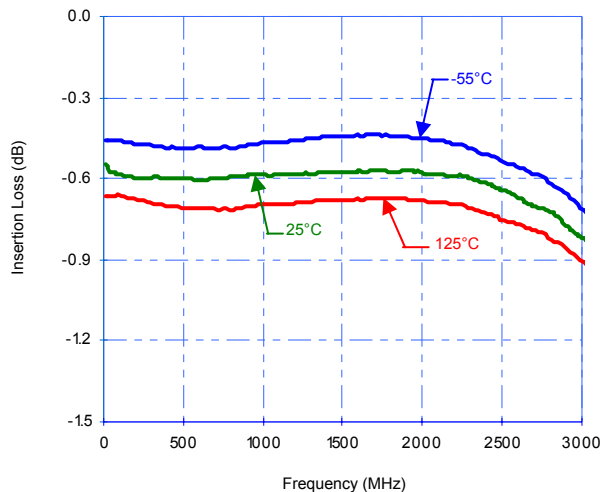


Figure 5. Input 1 dB Compression Point & IIP3

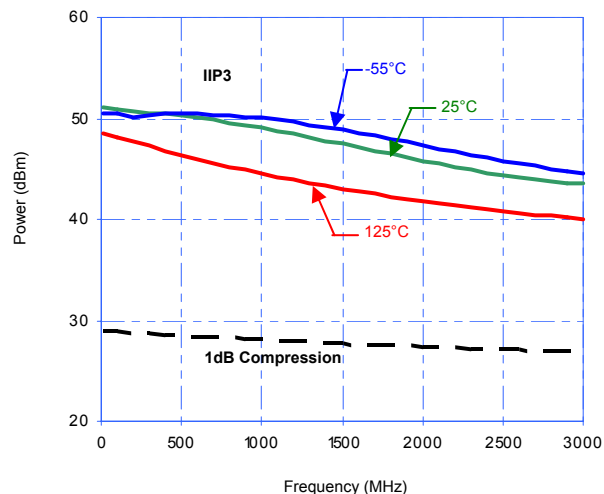


Figure 6. Insertion Loss – RFC to RF2

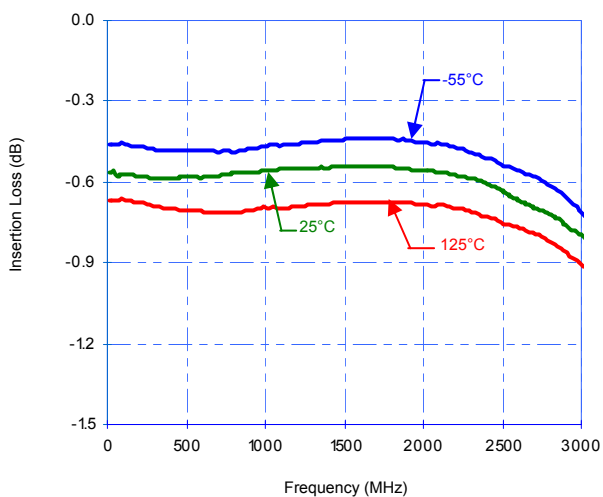
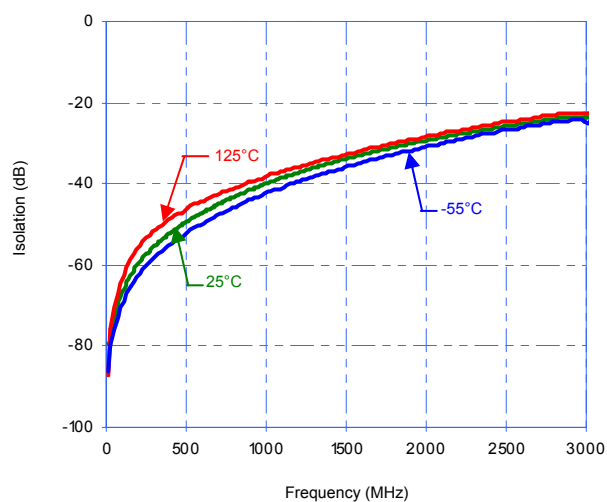


Figure 7. Isolation – RFC to RF1



Typical Performance Data -55 °C to +125 °C (Unless Otherwise Noted)

Figure 8. Isolation – RFC to RF2

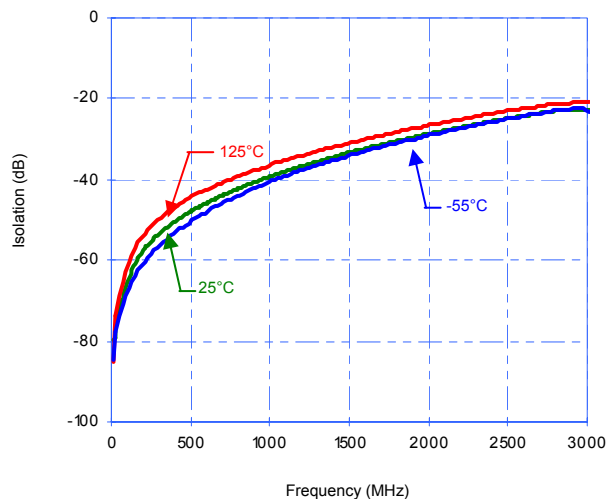


Figure 9. Isolation – RF1 to RF2, RF2 to RF1

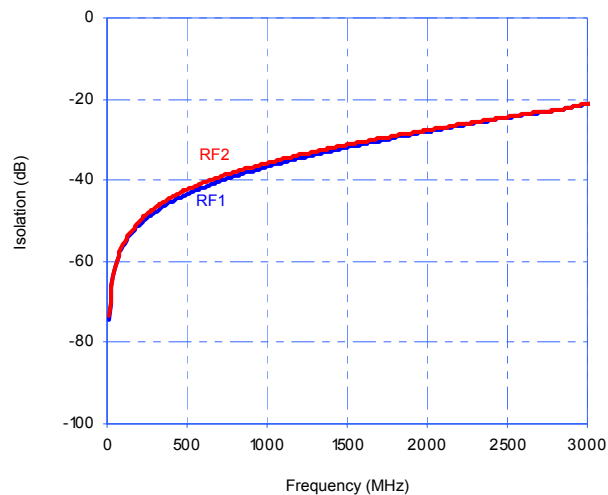


Figure 10. Return Loss – RFC to RF1, RF2

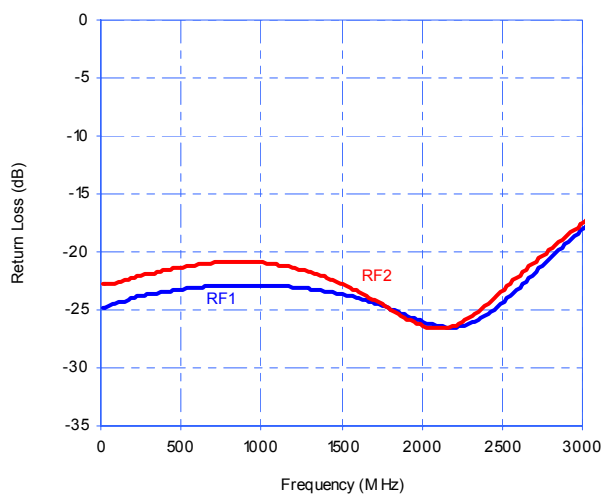
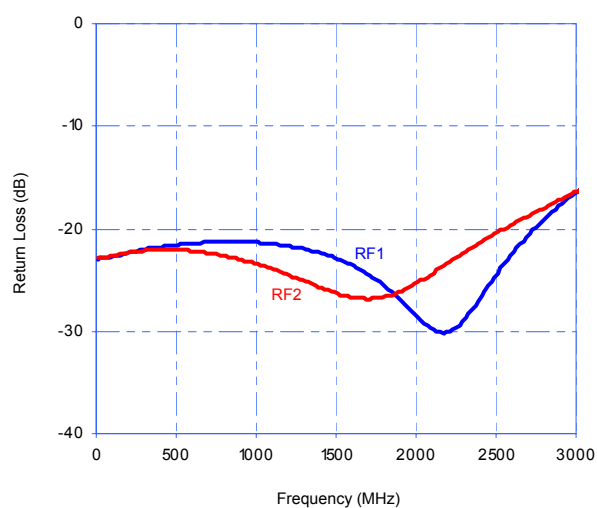


Figure 11. Return Loss – RF1, RF2



Evaluation Kit Information

Evaluation Kit

The SPDT Switch Evaluation Kit board was designed to ease customer evaluation of the PE84244 SPDT switch. The RF common port is connected through a 50 Ω transmission line to the top left SMA connector, J1. Port 1 and Port 2 are connected through 50 Ω transmission lines to the top two SMA connectors on the right side of the board, J3 and J4. A through transmission line connects SMA connectors J6 and J8. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.030", trace gaps of 0.007", dielectric thickness of 0.028", metal thickness of 0.0014" and ϵ_r of 4.4.

J2 provides a means for controlling DC and digital inputs to the device. Starting from the lower left pin, the second pin to the right (J2-3) is connected to the device CNTL input. The fourth pin to the right (J2-7) is connected to the device V_{DD} input. A decoupling capacitor (100 pF) is provided on both CNTL and V_{DD} traces. It is the responsibility of the customer to determine proper supply decoupling for their design application. Removing these components from the evaluation board has not been shown to degrade RF performance.

Figure 12. Evaluation Board Layouts

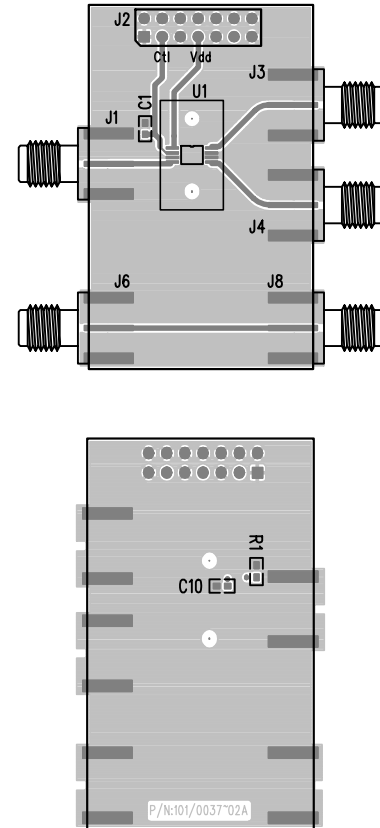


Figure 13. Evaluation Board Schematic

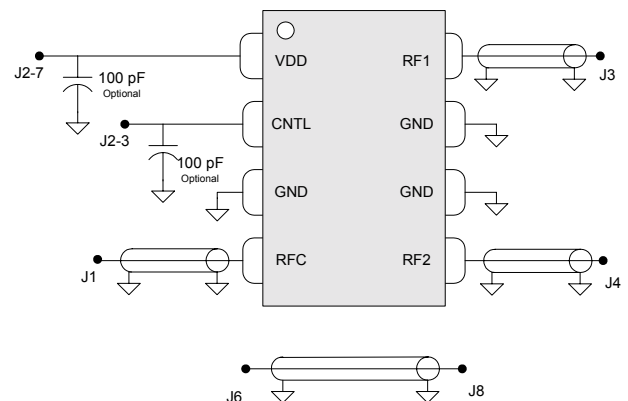


Figure 14. Package Drawing

8-lead MSOP

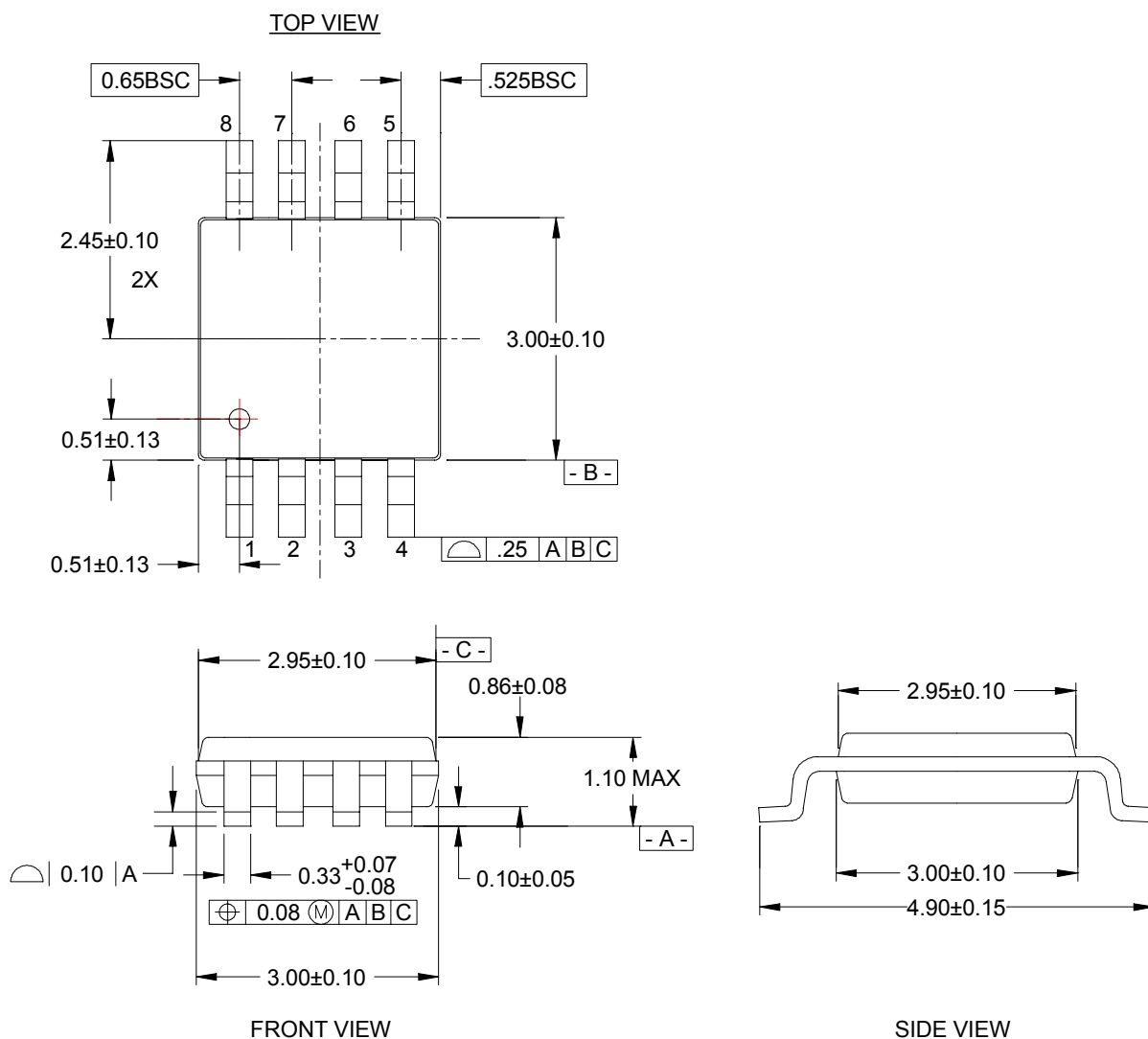


Table 6. Ordering Information

| Order Code | Part Marking | Description | Package | Shipping Method |
|------------|--------------|----------------------|----------------|------------------|
| 84244-01 | 84244 | PE84244-08MSOP-50A | 8-lead MSOP | 50 units / Tube |
| 84244-02 | 84244 | PE84244-08MSOP-2000C | 8-lead MSOP | 2000 units / T&R |
| 84244-00 | PE84244-EK | PE84244-08MSOP-EK | Evaluation Kit | 1 / Box |