PCKEP14

2.5 V/3.3 V 1:5 differential ECL/PECL/HSTL clock driver

Rev. 01 — 30 October 2002 **Product data**

1. Description

The PCKEP14 is a low skew 1-to-5 differential driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The ECL/PECL input signals can be either differential or single-ended (if the V_{BB} output is used). HSTL inputs can be used when the PCKEP14 is operating under PECL conditions.

The PCKEP14 specifically guarantees low output-to-output skew. Optimal design, layout, and processing minimize skew within a device, and from device to device.

To ensure that the tight skew specification is realized, both sides of any differential output need to be terminated identically into 50 Ω resistors, even if only one output is being used. If an output pair is unused, both outputs may be left open (unterminated) without affecting skew.

The common enable ($\overline{EN}$) is synchronous, outputs are enabled/disabled in the LOW state. This avoids a runt clock pulse when the device is enabled/disabled, as can happen with an asynchronous control. The internal flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

The PCKEP14, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the PCKEP14 to be used for high performance clock distribution in +3.3 V or +2.5 V systems.

2. Features

- 100 ps device-to-device skew
- 25 ps within device skew
- 400 ps typical propagation delay
- Maximum frequency > 2 GHz (typical)
- Contains temperature compensation
- PECL and HSTL mode: V_{CC} = 2.375 V to 3.8 V with V_{EE} = 0 V
- NECL mode: V_{CC} = 0 V with V_{EE} = –2.375 V to –3.8 V
- LVDS input compatible
- Open input default state.

3. Pinning information

3.1 Pinning

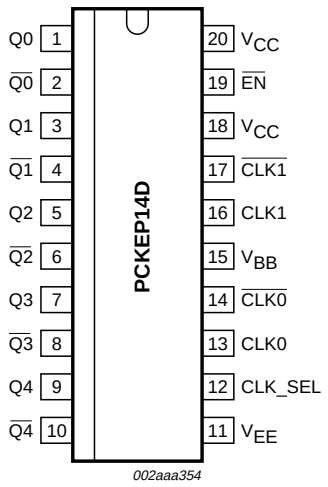


Fig 1. SO20 pin configuration.

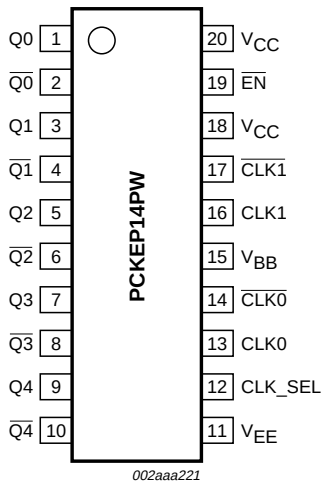


Fig 2. TSSOP20 pin configuration.

3.2 Pin description

Table 1: Pin description

Symbol	Pin	Description
Q0-Q4	1, 3, 5, 7, 9	Positive ECL/PECL output
$\overline{Q0}$-$\overline{Q4}$	2, 4, 6, 8, 10	Negative ECL/PECL output
V_{EE}	11	Negative supply
CLK_SEL	12	ECL/PECL active clock select input. Pin will default LOW when left open.
CLK0, CLK1	13, 16	ECL/PECL/HSTL CLK input. Pins will default LOW when left open.
$\overline{CLK0}$, $\overline{CLK1}$	14, 17	ECL/PECL/HSTL CLK input. Pins will default to $V_{CC}/2$ when left open.
V_{BB}	15	Reference voltage output
V_{CC}	18, 20	Positive supply
$\overline{EN}$	19	ECL synchronous enable

3.2.1 Power supply connection

CAUTION

All V_{CC} and V_{EE} pins must be connected to power supply to guarantee proper operation.

4. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
PCKEP14D	SO20	plastic small outline package 8 leads; body width 7.5 mm	SOT163-1
PCKEP14PW	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

5. Logic diagram

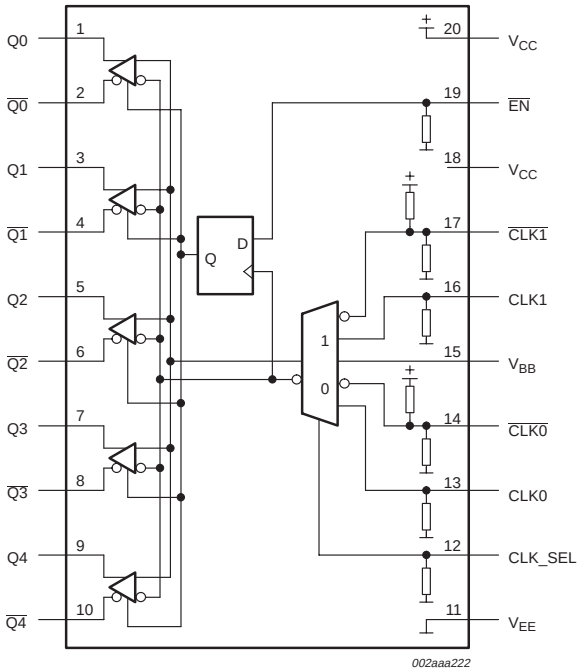


Fig 3. Logic diagram.

CAUTION

All V_{CC} and V_{EE} pins must be connected to power supply to guarantee proper operation.

6. Function table

Table 3: Function table

CLK0	CLK1	CLK_SEL	$\overline{EN}$	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L[1]

[1] On next negative transition of CLK0 or CLK1.

7. Attributes

Table 4: Attributes

Characteristic		Value
internal input pull-down resistor		75 kΩ
internal input pull-up resistor		37.5 kΩ
ESD protection	Human Body Model	> 2.5 kV
	Machine Model	> 100 V
	Charged Device Model	> 1 kV
moisture sensitivity, indefinite time out of drypack		Level 1
flammability rating		UL-94 code V-0 A 1/8”
Meets or exceeds JEDEC Specification EIA/JEDS78 IC latch-up test.		

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	PECL mode power supply	V_{EE} = 0 V	-	4.1	V
V_{EE}	NECL mode power supply	V_{CC} = 0 V	-	–4.1	V
V_I	PECL mode input voltage	V_{EE} = 0 V; $V_I \leq V_{CC}$	-	4.1	V
	NECL mode input voltage	V_{CC} = 0 V; $V_I \geq V_{EE}$	-	–4.1	V
I_{out}	output current	continuous	-	50	mA
		surge	-	100	mA
I_{BB}	V_{BB} source current		0	0.1	mA
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature range		–65	+150	°C
$R_{th(j-a)}$	thermal resistance from junction to ambient	0 LFPM	-	140	°C/W
		500 LFPM	-	100	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		23	41	°C/W
T_{sld}	soldering temperature		-	265	°C

9. Static characteristics

Table 6: PECL DC characteristics[1]

V_{CC} = 2.5 V; V_{EE} = 0 V [2]

Symbol	Parameter	Conditions	T_{amb} = –40 °C			T_{amb} = +25 °C			T_{amb} = +85 °C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	power supply current		45	60	75	45	60	75	45	60	75	mA
V_{OH}	HIGH-level output voltage	[3]	1355	1480	1605	1355	1500	1605	1355	1510	1605	mV
V_{OL}	LOW-level output voltage	[3]	555	720	805	555	700	805	555	710	805	mV
V_{IH}	HIGH-level input voltage	single-ended	1335	-	1620	1335	-	1620	1275	-	1620	mV
V_{IL}	LOW-level input voltage	single-ended	555	-	875	555	-	875	555	-	875	mV
V_{IHCMR}	HIGH-level input voltage, common mode range (differential)	[4]	1.2	-	2.5	1.2	-	2.5	1.2	-	2.5	V
I_{IH}	HIGH-level input current		-	-	150	-	-	150	-	-	150	µA
I_{IL}	LOW-level input current	CLK	0.5	-	-	0.5	-	-	0.5	-	-	µA
		$\overline{CLK}$	–150	-	-	–150	-	-	–150	-	-	µA
V_{BB}	output reference voltage		1075	1165	1265	1065	1165	1265	1085	1180	1270	mV

[1] Devices are designed to meet the DC specifications shown in this table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 LFPM is maintained.

[2] Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.125 V to –1.3 V.

[3] All loading with 50 Ω to V_{CC} – 2 V.

[4] $V_{IHCMR(min)}$ varies 1:1 with V_{EE}, $V_{IHCMR(max)}$ varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 7: PECL DC characteristics[1]

V_{CC} = 3.3 V; V_{EE} = 0 V [2]

Symbol	Parameter	Conditions	T_{amb} = −40 °C			T_{amb} = +25 °C			T_{amb} = +85 °C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	power supply current		45	60	75	45	60	75	45	60	75	mA
V_{OH}	HIGH-level output voltage	[3]	2155	2280	2405	2155	2300	2405	2155	2310	2405	mV
V_{OL}	LOW-level output voltage	[3]	1355	1515	1605	1355	1500	1605	1355	1500	1605	mV
V_{IH}	HIGH-level input voltage	single-ended	2135	-	2420	2135	-	2420	2135	-	2420	mV
V_{IL}	LOW-level input voltage	single-ended	1355	-	1675	1355	-	1675	1355	-	1675	mV
V_{BB}	output reference voltage	[4]	1875	1965	2065	1865	1965	2065	1885	1980	2070	mV
V_{IHCMR}	HIGH-level input voltage, common mode range (differential)	[5]	1.2	-	3.3	1.2	-	3.3	1.2	-	3.3	V
I_{IH}	HIGH-level input current		-	-	150	-	-	150	-	-	150	µA
I_{IL}	LOW-level input current	CLK	0.5	-	-	0.5	-	-	0.5	-	-	µA
		$\overline{CLK}$	−150	-	-	−150	-	-	−150	-	-	µA

[1] Devices are designed to meet the DC specifications shown in this table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 LFPM is maintained.

[2] Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925 V to −0.5 V.

[3] All loading with 50 Ω to V_{CC} − 2 V.

[4] Single-ended input operation is limited to $V_{CC} \geq 3.0$ V in PECL mode.

[5] $V_{IHCMR(min)}$ varies 1:1 with V_{EE}, $V_{IHCMR(max)}$ varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 8: NECL DC characteristics[1]

V_{CC} = 0 V; V_{EE} = –3.8 V to –2.375 V [2]

Symbol	Parameter	Conditions	T_{amb} = –40 °C			T_{amb} = +25 °C			T_{amb} = +85 °C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	power supply current		45	60	75	45	60	75	45	60	95	mA
V_{OH}	HIGH-level output voltage	[3]	–1145	–1020	–895	–1145	–1000	–895	–1145	–990	–895	mV
V_{OL}	LOW-level output voltage	[3]	–1945	–1785	–1695	–1945	–1800	–1695	–1945	–1800	–1695	mV
V_{IH}	HIGH-level input voltage	single-ended	–1165	-	–880	–1165	-	–880	–1165	-	–880	mV
V_{IL}	LOW-level input voltage	single-ended	–1945	-	–1625	–1945	-	–1625	–1945	-	–1625	mV
V_{BB}	output reference voltage	[4]	–1425	–1335	–1235	–1435	–1335	–1235	–1415	–1320	–1230	mV
V_{IHCMR}	HIGH-level input voltage, common mode range (differential)	[5]	V_{EE}+1.2		0	V_{EE}+1.2		0	V_{EE}+1.2		0	V
I_{IH}	HIGH-level input current		-	-	150	-	-	150	-	-	150	µA
I_{IL}	LOW-level input current	CLK	0.5	-	-	0.5	-	-	0.5	-	-	µA
		$\overline{CLK}$	–150	-	-	–150	-	-	–150	-	-	µA

[1] Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 LFPM is maintained.

[2] Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925 V to –0.5 V.

[3] All loading with 50 Ω to V_{CC} – 2 V.

[4] Single-ended input operation is limited to $V_{EE} \leq 3.0$ V in NECL mode.

[5] $V_{IHCMR(min)}$ varies 1:1 with V_{EE}, $V_{IHCMR(max)}$ varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 9: HSTL DC characteristics

V_{CC} = 2.375 V to 3.8 V; V_{EE} = 0 V.

Symbol	Parameter	Conditions	T_{amb} = –40 °C			T_{amb} = +25 °C			T_{amb} = +85 °C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	HIGH-level input voltage		1200	-	-	1200	-	-	1200	-	-	mV
V_{IL}	LOW-level input voltage		-	-	400	-	-	400	-	-	400	mV

10. Dynamic characteristics

Table 10: AC characteristics

(V_{CC} = 0 V; V_{EE} = −2.375 V to −3.8 V) or (V_{CC} = 2.375 V to 3.8 V; V_{EE} = 0 V) [1]

Symbol	Parameter	Conditions	T_{amb} = −40 °C			T_{amb} = +25 °C			T_{amb} = +85 °C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max(PECL/HSTL)}$	maximum toggle frequency	see Figure 4	-	> 2	-	-	> 2	-	-	> 2	-	GHz
t_{PLH}, t_{PHL}	propagation delay to output differential		250	345	425	275	360	475	300	430	525	ps
t_{SKEW}	skew time	within-device	-	10	25	-	15	25	-	15	25	ps
		part-to-part [2]	-	100	125	-	150	175	-	200	225	ps
t_{JITTER}	cycle-to-cycle jitter	see Figure 4	-	0.2	< 1	-	0.2	< 1	-	0.2	< 1	ps
t_{su}	$\overline{EN}$ set-up time		100	50	-	100	50	-	100	50	-	ps
t_h	$\overline{EN}$ hold time		200	140	-	200	140	-	200	140	-	ps
$V_{i(p-p)}$	minimum input swing		150	800	1200	150	800	1200	150	800	1200	mV
t_r/t_f	output rise/fall times	(20% - 80%)	125	205	250	125	200	250	125	200	275	ps

[1] Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} − 2.0 V.

[2] Skew is measured between outputs under identical transitions.

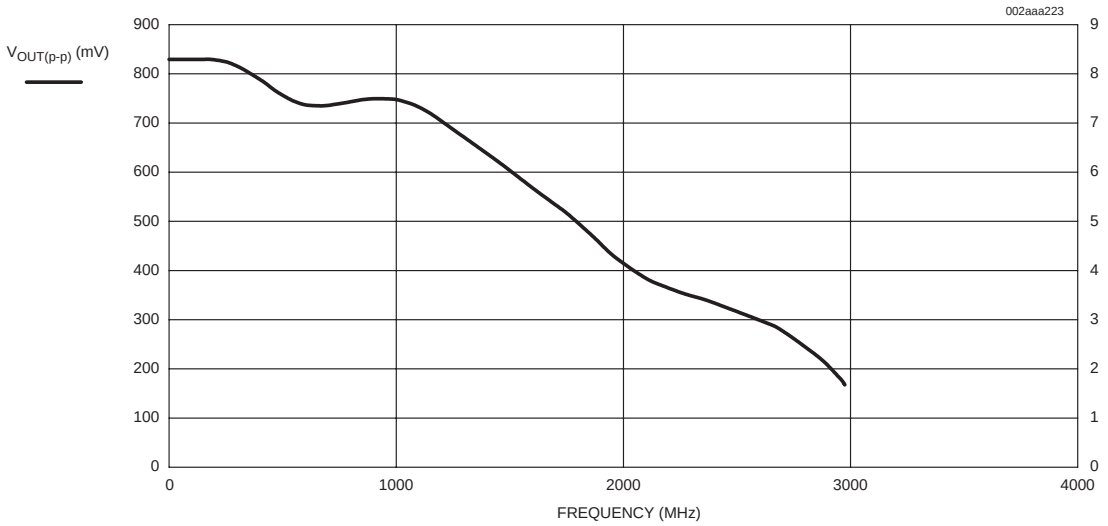
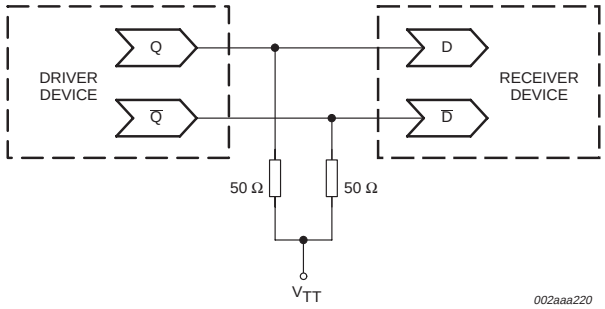


Fig 4. f_{max}.

11. Application information

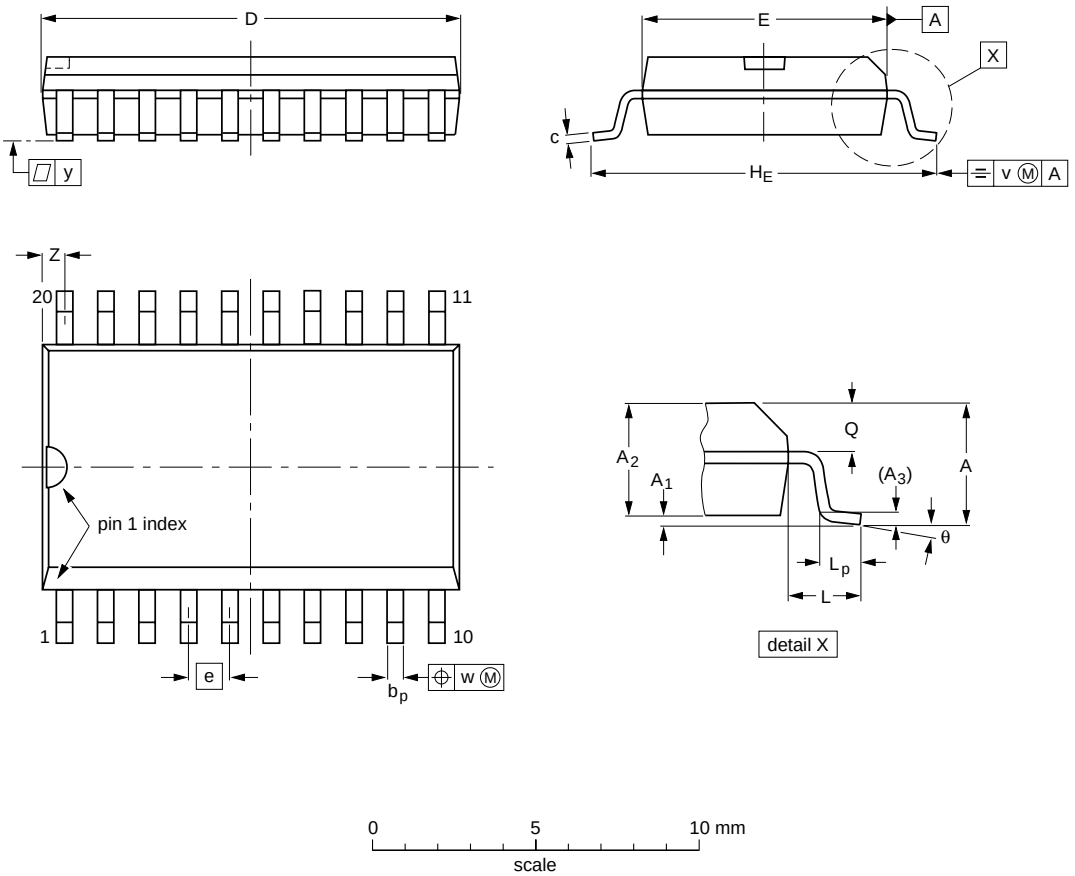


$V_{TT} = V_{CC} - 2.0$ V.

Fig 5. Typical termination for output driver and device evaluation.

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

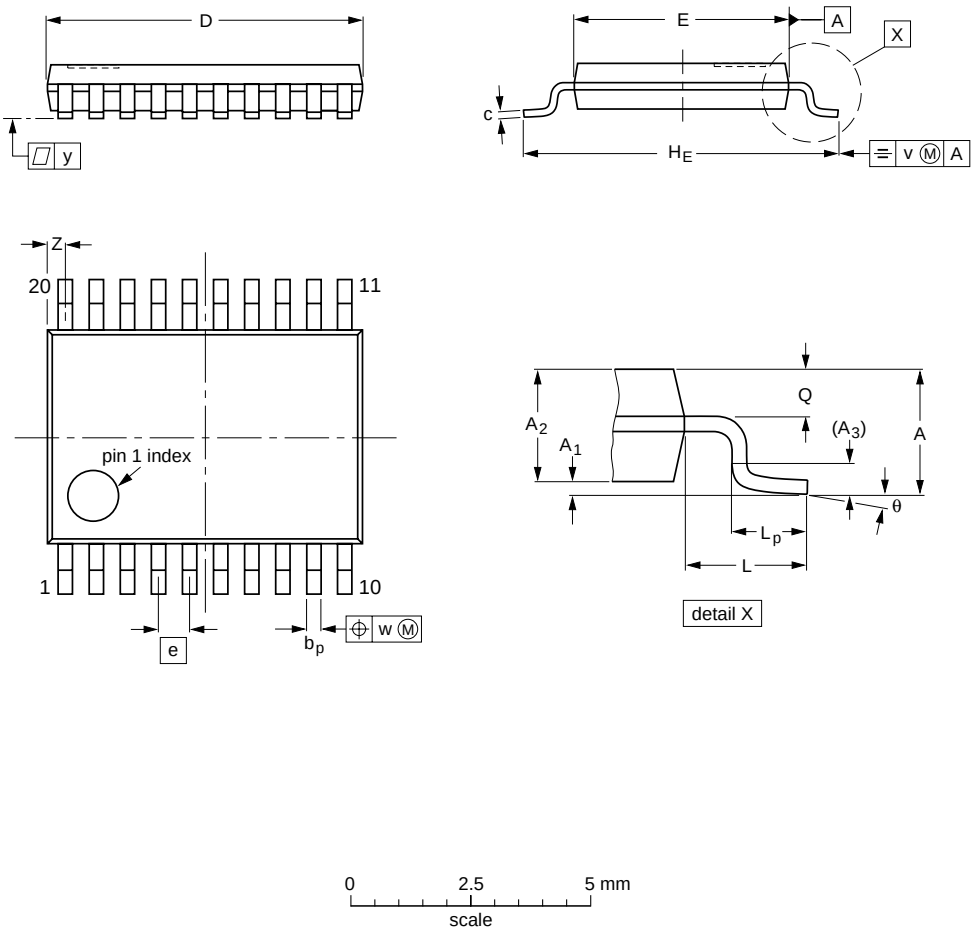
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013				~~97-05-22~~ 99-12-27

Fig 6. SO20 package outline (SOT163-1).

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153				~~95-02-04~~ 99-12-27

Fig 7. TSSOP20 package outline (SOT360-1).

13. Soldering

13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C small/thin packages.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

13.5 Package related soldering information

Table 11: Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[4] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[5] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[6] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

14. Revision history

Table 12: Revision history

Rev	Date	CPCN	Description
01	20021030	-	**Product data (9397 750 09565)**
			Engineering Change Notice 853-2373 28877 (date: 20020909)

15. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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