INTERSIL

# IM5600/IM5610
# 256 Bit Bipolar Read Only Memory

## FEATURES

- Uses Patented AIM Programming Element for
  - Superior Reliability
  - High Programming Yield
  - Fast Programming Speed < 1 sec
  - TTL Processing Compatibility
- Low Power Consumption 1.5 mW/bit
- Operating Speed
  - Address to Output — 50nS
  - Chip Enable to Output — 40nS
- Large Output Drive — 16mA @ 0.45V
- TTL Compatible Inputs & Outputs
- Two Output Designs
  - 5600 Open Collector
  - 5610 Active Pull-up
- Chip Enable Facilitates Memory Expansion and Use in Bus Organized Systems

## APPLICATIONS

- Code Conversion
- Logic Implementation
- Microprogramming
- Look-up Tables
- Control of Sequential Circuits
- Character Generation

## GENERAL DESCRIPTION

The Intersil IM5600 and IM5610 are high speed, electrically programmable, fully decoded, bipolar 256 bit read only memories organized as 32 words by 8 bits. On-chip address decoding, chip enable input and uncomitted collector or three-state outputs provide for simplified memory expansion and use in bus organized systems.

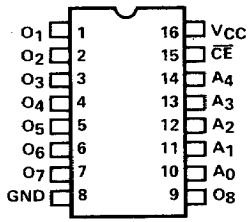
Unprogrammed AIM elements are sensed as ZERO's or low logic levels at the outputs. Programming with a commercially available programmer irreversibly converts selected elements in the array so that they are sensed as ONE's or high logic levels.

The following companies make programmers approved by Intersil:

1. Data I/O Corp., P.O. Box 1603, Bellevue, Wash. 98009
2. PRO-LOG Corp., 2411 Garden Rd., Monterey, CA 93940

Detailed programming specifications for all Intersil PROMs are presented in the Intersil BIPOLAR PROM PROGRAMMING SPECIFICATION Data Sheet.

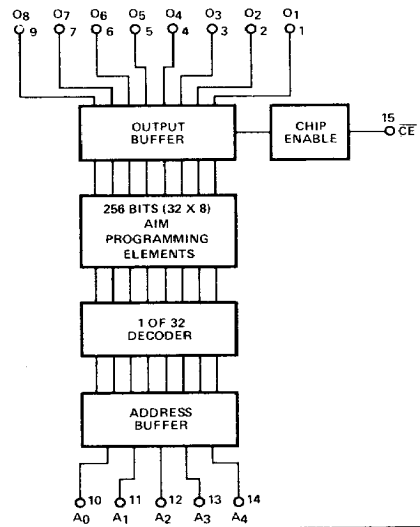
## CONNECTION DIAGRAM




TOP VIEW

**(outline dwgs JE, PE)**

## BLOCK DIAGRAM




## ORDERING INFORMATION

| PART NUMBER | PACKAGE | TEMPERATURE RANGE | ORDER NUMBER |
|---|---|---|---|
| IM5600 | 16 Pin Flatpack | 0°C to +75°C Commercial<br>−55°C to +125°C Military | IM5600CFE<br>IM5600MFE* |
| | 16 Pin Plastic DIP | 0°C to +75°C | IM5600CPE |
| | 16 Pin Cerdip DIP | 0°C to +75°C Commercial<br>−55°C to +125°C Military | IM5600CJE<br>IM5600MJE* |
| IM5610 | 16 Pin Flatpack | 0°C to +75°C Commercial<br>−55°C to +125°C Military | IM5610CFE<br>IM5610MFE* |
| | 16 Pin Plastic DIP | 0°C to +75°C | IM5610CPE |
| | 16 Pin Cerdip DIP | 0°C to +75° C Commercial<br>−55°C to +125°C Military | IM5610CJE<br>IM5610MJE* |

* If 883B processing is desired add /883B to order number.

## TRUTH TABLE

| ADDRESS INPUTS $A_0$–$A_4$ | $\overline{CE}$ | ANY OUTPUT $O_1$–$O_8$ |
|---|---|---|
| Any one of 32 possible addresses. | L | H—if the bit uniquely associated with this output and address has been electrically programmed.<br>L—if it has not been programmed. |
| Any one of 32 possible addresses. | H | All outputs are forced to a high impedance state regardless of the address. |

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## ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +7.0V
Input Voltage Applied ..... −1.5V to +5.5V
Output Voltage Applied ..... −0.5V to +$V_{CC}$
Output Voltage Applied (Programming Only) ..... 28V
Current Into Output (Programming Only) ..... 210 mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature Range*
(IM5600C and IM5610C) ..... 0°C to +75°C
(IM5600M and IM5610M) ..... −55°C to +125°C

*Operating temperature is defined as ambient temperature for the DIP and case temperature for the flatpack. Case temperature is measured directly below the die.

## DC CHARACTERISTICS

| SYMBOL | CHARACTERISTICS | LIMITS $V_{CC}$ = 5.0V ±5% T = 0°C to +75°C MIN | TYP | MAX | LIMITS $V_{CC}$ = 5.0V ±10% T = −55°C to +125°C MIN | TYP | MAX | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| $I_{FA}$ | Address Input Load Current | | −0.63 | −1.0 | | −0.63 | −1.0 | mA | $V_A$ = 0.4V |
| $I_{FE}$ | Chip Enable Input Load Current | | −0.63 | −1.0 | | −0.63 | −1.0 | | $V_{\overline{CE}}$ = 0.4V |
| $I_{RA}$ | Address Input Leakage Current | | 5.0 | 40 | | 5.0 | 60 | μA | $V_A$ = 4.5V |
| $I_{RE}$ | Chip Enable Input Leakage Current | | 5.0 | 40 | | 5.0 | 60 | | $V_{\overline{CE}}$ = 4.5V |
| $V_{OL}$ | Output Low Voltage | | 0.3 | 0.45 | | 0.3 | 0.45 | V | $I_{OL}$ = 16 mA $V_{CE}$ = 0.4V '0' bit is addressed. |
| $V_{IL}$ | Input Low Voltage | | | 0.8 | | | 0.8 | | |
| $V_{IH}$ | Input High Voltage | 2.0 | | | 2.0 | | | | |
| $V_C$ | Input Clamp Voltage | | −0.9 | −1.5 | | −0.9 | −1.5 | | $I_{IN}$ = −10 mA |
| $BV_{IN}$ | Input Breakdown Voltage | 5.5 | 6.5 | | 5.5 | 6.5 | | | $I_{IN}$ = 1.0 mA |
| $I_{CC}$ | Power Supply Current | | 75 | 100 | | 75 | 100 | mA | Inputs Either Open or at Ground |
| $I_O$ (High R State) | Output Leakage Current | | <1.0 | 40 | | <1.0 | 100 | μA | $V_O$ = 5.5V, $V_{CE}$ = 2.4V |
| $I_O$ (High R State) | Output Leakage Current | | <−1.0 | −40 | | <−1.0 | −100 | | $V_O$ = 0.4V, $V_{CE}$ = 2.4V |
| $C_{IN}$ | Input Capacitance | | 5.0 | | | 5.0 | | pF | $V_{IN}$ = 2.0V, $V_{CC}$ = 0V |
| $C_{OUT}$ | Output Capacitance | | 7.0 | | | 7.0 | | | $V_O$ = 2.0V, $V_{CC}$ = 0V |

The following are guaranteed characteristics of the output high level state when the chip is enabled ($\overline{CE}$ = 0.4V) and a programmed bit is addressed. These characteristics cannot be tested prior to programming but are guaranteed by design.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $I_{OLK}$ | Output Leakage Current | | <1.0 | 100 | | <1.0 | 100 | μA | $V_O$ = 5.5V, $V_{\overline{CE}}$ = 0.4V |
| $V_{OH}$ (IM5610) | Output High Voltage | 2.4 | 3.2 | | 2.4 | 3.2 | | V | $I_{OH}$ = −1.0 mA (IM5610M) $I_{OH}$ = −2.4 mA (IM5610C) |
| $I_{SC}$ (IM5610) | Output Short Circuit | −15 | −30 | −60 | −15 | −30 | −60 | mA | $V_O$ = 0V |

**NOTE 1:** Typical characteristics are for $V_{CC}$ = 5.0V, $T_A$ = 25°C.

## SWITCHING CHARACTERISTICS

| SYMBOL | CHARACTERISTIC | LIMITS $V_{CC}$ = 5V $T_A$ = 25°C | | LIMITS $V_{CC}$ = 5V ±5% $T_A$ = 0°C to +75°C | | LIMITS $V_{CC}$ = 5V ±10% $T_A$ = −55°C to +125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{aa}$ | Address Access Time | 20 | 50 | 20 | 65 | 20 | 75 | ns |
| $t_{dis}$ | Output Disable Time* | 10 | 40 | 10 | 50 | 10 | 60 | |
| $t_{en}$ | Output Enable Time* | 5 | 40 | 5 | 50 | 5 | 60 | |

* Output disable time is the time taken for the output to reach a high resistance state when the chip enable is taken high. Output enable time is the time taken for the output to become active when the chip enable is taken low. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

## SWITCHING WAVEFORMS

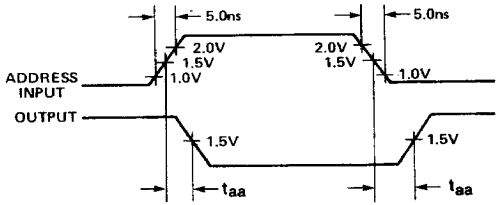


**FIGURE 1:** Access Time Via Address Input

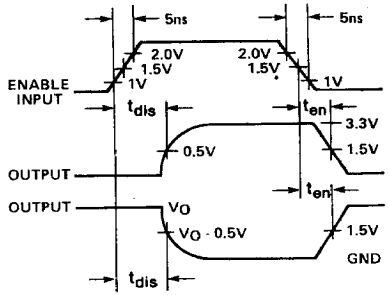


**FIGURE 2:** Output Disable And Enable Time

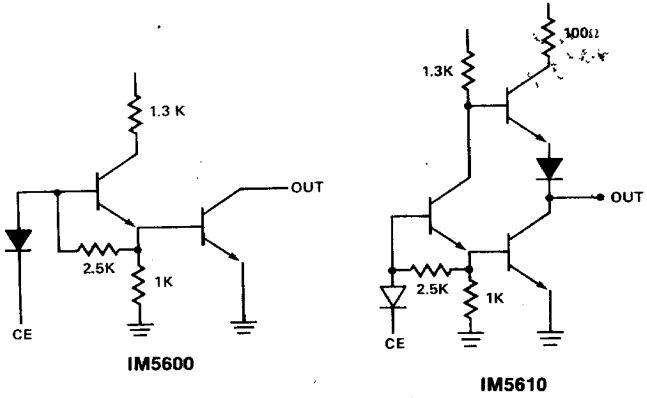


**FIGURE 3:** Output Stage Schematics

## SWITCHING TIME TEST CONDITIONS

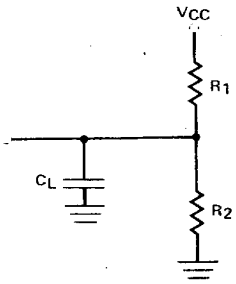


**FIGURE 4:** Output Load Circuit

| SWITCHING PARAMETER | IM5600 $R_1$ | IM5600 $R_2$ | IM5600 $C_L$ | IM5610 $R_1$ | IM5610 $R_2$ | IM5610 $C_L$ |
|---|---|---|---|---|---|---|
| $t_{aa}$ | 300Ω | 600Ω | 30 pF | 300Ω | 600Ω | 30 pF |
| $t_{dis}$ '1' | ∞ | 3.3 KΩ | 10 pF | ∞ | 600Ω | 10 pF |
| $t_{dis}$ '0' | 300Ω | 600Ω | 10 pF | 300Ω | 600Ω | 10 pF |
| $t_{en}$ '1' | ∞ | 3.3 KΩ | 30 pF | ∞ | 600Ω | 30 pF |
| $t_{en}$ '0' | 300Ω | 600Ω | 30 pF | 300Ω | 600Ω | 30 pF |

### INPUT CONDITIONS

Amplitude — 0V to 3V
Rise and Fall Time — 5 ns From 1V to 2V
Frequency — 1 MHz