International
IOR Rectifier

PRELIMINARY

IRS2136D/IRS21362D/IRS21363D/IRS21365D/ IRS21366D/IRS21367D/IRS21368D (J&S) PBF

3-PHASE BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V (IRS2136D/ IRS21368D), 11.5 V to 20 V (IRS21362D), or 12 V to 20 V (IRS21363D/IRS21365D/IRS21366D/IRS21367D
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent 3 half-bridge drivers
- Matched propagation delay for all channels
- Cross-conduction prevention logic
- Integrated bootstrap diode function
- Low side output out of phase with inputs. High side outputs out of phase (IRS213(6,63, 65, 66, 67, 68)D), or in phase (IRS21362D) with inputs
- 3.3 V logic compatible
- Lower di/dt gate drive for better noise immunity
- Externally programmable delay for automatic fault clear
- All parts are LEAD-FREE

Packages


28-Lead SOIC


28-Lead PDIP


44-Lead PLCC w/o 12 Leads

Applications:

*Motor Control
*Air Conditioners/ Washing Machines
*General Purpose Inverters
*Micro/Mini Inverter Drives

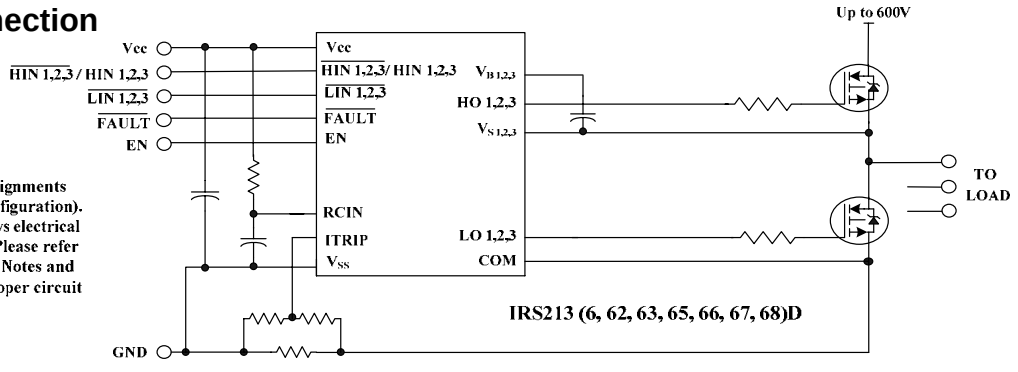
Description

The IRS2136xD (J&S) are high voltage, high speed power MOSFET and IGBT driver with three independent high side and low side referenced output channels for 3-phase applications. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3 V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. An enable function is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that an overcurrent or undervoltage shutdown has occurred. Overcurrent fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 V.

Feature Comparison:
IRS2136xD

Part	IRS2136D	IRS21362D	IRS21363D	IRS21365D	IRS21366D	IRS21367D	IRS21368D
Input Logic	$\overline{HIN}$, $\overline{LIN}$	HIN, $\overline{LIN}$	$\overline{HIN}$, $\overline{LIN}$	$\overline{HIN}$, $\overline{LIN}$	$\overline{HIN}$, $\overline{LIN}$	$\overline{HIN}$, $\overline{LIN}$	$\overline{HIN}$, $\overline{LIN}$
t_{on} (typ.)	530 ns	530 ns	530 ns	530 ns	200 ns	200 ns	530 ns
t_{off} (typ.)	530 ns	530 ns	530 ns	530 ns	200 ns	200 ns	530 ns
V_{IH} (min.)	2.5 V	2.5 V	2.5 V	2.5 V	2.5 V	2.5 V	2.5 V
V_{IL} (max.)	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V
V_{ITRIP+}	0.46 V	0.46 V	0.46 V	4.3 V	0.46 V	4.3 V	4.3 V
V_{CCUV+}/ V_{BSUV+}	8.9 V	10.4 V	11.1 V	11.1 V	11.1 V	11.1 V	8.9 V
V_{CCUV-}/ V_{BSUV-}	8.2 V	9.4 V	10.9 V	10.9 V	10.9 V	10.9 V	8.2 V

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This diagram shows electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_S	High side offset voltage		$V_{B\,1,2,3}$ - 20	$V_{B\,1,2,3}$ + 0.3	V
V_B	High side floating supply voltage		-0.3	620	
$V_{HO1,2,3}$	High side floating output voltage		$V_{S1,2,3}$ - 0.3	$V_{B\,1,2,3}$ + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	20	
V_{SS}	Logic ground		V_{CC} - 20	V_{CC} + 0.3	
$V_{LO1,2,3}$	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Input voltage $\overline{LIN}$, $\overline{HIN}$, ITRIP, EN, RCIN		V_{SS} -0.3	V_{CC} + 0.3	
V_{FLT}	$\overline{FAULT}$ output voltage		V_{SS} -0.3	V_{CC} + 0.3	
dV/dt	Allowable offset voltage slew rate		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25$ °C	(28 lead PDIP)	—	1.5	W
		(28 lead SOIC)	—	1.6	
		(44 lead PLCC)	—	2.0	
Rth_{JA}	Thermal resistance, junction to ambient	(28 lead PDIP)	—	83	°C/W
		(28 lead SOIC)	—	78	
		(44 lead PLCC)	—	63	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic-timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute referenced to COM. The V_S & V_{SS} offset ratings are tested with all supplies biased at a 15 V differential.

Symbol	Definition		Min.	Max.	Units
$V_{B1,2,3}$	High side floating supply voltage	IRS213(6,68)D	$V_{S1,2,3}$ +10	$V_{S1,2,3}$ + 20	V
		IRS21362D	$V_{S1,2,3}$ +11.5	$V_{S1,2,3}$ + 20	
		IRS213(6,63,65,66,67)D	$V_{S1,2,3}$ +12	$V_{S1,2,3}$ + 20	
$V_{S\,1,2,3}$	High side floating supply voltage		Note 1	600	
V_{CC}	Low side supply voltage	IRS213(6,68)D	10	20	
		IRS21362D	11.5	20	
		IRS213(6,63,65,66,67)D	12	20	
$V_{HO\,1,2,3}$	High side output voltage		$V_{S1,2,3}$	$V_{B1,2,3}$	
$V_{LO1,2,3}$	Low side output voltage		0	V_{CC}	
V_{SS}	Logic ground		-5	5	
V_{FLT}	$\overline{FAULT}$ output voltage		V_{SS}	V_{CC}	
V_{RCIN}	RCIN input voltage		V_{SS}	V_{CC}	

Note 1: Logic operational for V_S of (COM - 8 V) to (COM + 600 V). Logic state held for V_S of (COM - 8 V) to (COM – V_{BS}). (Please refer to the Design Tip DT97-3 for more details).

Recommended Operating Conditions - (Continued)

The input/output logic-timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute referenced to COM. The V_S & V_{SS} offset ratings are tested with all supplies biased at a 15 V differential.

Symbol	Definition	Min.	Max.	Units
V_{ITRIP}	ITRIP input voltage	V_{SS}	V_{SS} + 5	V
V_{IN}	Logic input voltage $\overline{LIN}$, $\overline{HIN}$ (IRS213(6,63,65,66,67,68)D), $\overline{LIN}$, HIN (IRS21362D), EN	V_{SS}	V_{SS} + 5	
T_A	Ambient temperature	-40	125	°C

Note 1: HIN, LIN, EN and the ITRIP pin are internally clamped with a 5.2 V zener diode.

Static Electrical Characteristics

V_{BIAS} (V_{CC},$V_{BS1,2,3}$) = 15 V unless otherwise specified. The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels ($\overline{HIN}$1,2,3/HIN1,2,3 and $\overline{LIN}$1,2,3). The V_O and I_O parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: LO1,2,3 and HO1,2,3.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “0” input voltage $\overline{LIN}$1,2,3, $\overline{HIN}$1,2,3 IRS213(6,63,65)D Logic “1” input voltage HIN1,2,3 IRS21362D	2.5	—	—	V	
	Logic “0” input voltage $\overline{LIN}$1,2,3, $\overline{HIN}$1,2,3 IRS213(66,67,68)D	2.5	—	—		
V_{IL}	Logic “1” input voltage $\overline{LIN}$1,2,3, $\overline{HIN}$1,2,3 IRS213(6,63,65)D Logic “0” input voltage HIN1,2,3 IRS21362D	—	—	0.8		
	Logic “0” input voltage $\overline{LIN}$1,2,3, $\overline{HIN}$1,2,3 IRS213(66,67,68)D					
$V_{IN,TH+}$	Input positive going threshold	—	1.9	—		
$V_{IN,TH-}$	Input negative going threshold	—	1	—		
$V_{EN,TH+}$	Enable positive going threshold	—	—	2.5		
$V_{EN,TH-}$	Enable negative going threshold	0.8	—	—		
$V_{IT,TH+}$ (6,62,63,66)	ITRIP positive going threshold	0.37	0.46	0.55		
$V_{IT,HYS}$ (6,62,63,66)	ITRIP hysteresis	—	0.07	—		
$V_{IT,TH+}$ (65,67,68)	ITRIP positive going threshold	3.85	4.3	4.75		
$V_{IT,HYS}$ (65,67,68)	ITRIP hysteresis	—	0.15	—		
$V_{RCIN,\ TH+}$	RCIN positive going threshold	—	8	—		
$V_{RCIN,\ HYS}$	RCIN hysteresis	—	3	—		
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	0.9	1.4		Io = 20 mA
V_{OL}	Low level output voltage, V_O	—	0.4	0.6		
V_{CCUV+} (6,68)	V_{CC} supply undervoltage positive going threshold	8	8.9	9.8		
V_{CCUV-} (6,68)	V_{CC} supply undervoltage negative going threshold	7.4	8.2	9		
V_{CCUVHY} (6,68)	V_{CC} supply undervoltage hysteresis	0.3	0.7	—		
V_{BSUV+} (6,68)	V_{BS} supply undervoltage positive going threshold	8	8.9	9.8		

Static Electrical Characteristics - (Continued)

V_{BIAS} (V_{CC},$V_{BS1,2,3}$) = 15 V unless otherwise specified. The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels ($\overline{HIN1,2,3}$/ HIN1,2,3 and LIN1,2,3). The V_O and I_O parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: LO1,2,3 and HO1,2,3.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{BSUV-} (6,68)	V_{BS} supply undervoltage negative going threshold	7.4	8.2	9	V	
V_{BSUVHY} (6,68)	V_{BS} supply undervoltage hysteresis	0.3	0.7	—		
V_{CCUV+} (62)	V_{CC} supply undervoltage positive going threshold	9.6	10.4	11.2		
V_{CCUV-} (62)	V_{CC} supply undervoltage negative going threshold	8.6	9.4	10.2		
V_{CCUVHY} (62)	V_{CC} supply undervoltage hysteresis	0.5	1	—		
V_{BSUV+} (62)	V_{BS} supply undervoltage positive going threshold	9.6	10.4	11.2		
V_{BSUV-} (62)	V_{BS} supply undervoltage negative going threshold	8.6	9.4	10.2		
V_{BSUVHY} (62)	V_{BS} supply undervoltage hysteresis	0.5	1	—		
V_{CCUV+} (63,65,66,67)	V_{CC} supply undervoltage positive going threshold	10.4	11.1	11.6		
V_{CCUV-} (63,65,66,67)	V_{CC} supply undervoltage negative going threshold	10.2	10.9	11.4		
V_{CCUVHY} (63,65,66,67)	V_{CC} supply undervoltage hysteresis	—	0.2	—		
V_{BSUV+} (63,65,66,67)	V_{BS} supply undervoltage positive going threshold	10.4	11.1	11.6		
V_{BSUV-} (63,65,66,67)	V_{BS} supply undervoltage negative going threshold	10.2	10.9	11.4		
V_{BSUVHY} (63,65,66,67)	V_{BS} supply undervoltage hysteresis	—	0.2	—		
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B=V_S= 600 V
I_{QBS}	Quiescent V_{BS} supply current	—	70	120		all inputs @ logic 0 value
I_{QCC}	Quiescent V_{CC} supply current	—	3	4	mA	
$V_{IN,CLAMP}$	Input clamp voltage (HIN, LIN, ITRIP and EN)	4.8	5.2	5.65	V	I_{IN}=100 µA
I_{LIN+} (6,62,63,65)	Input bias current (LOUT = HI)	—	110	150	µA	V_{IN}=4 V
I_{LIN-} (6,62,63,65)	Input bias current (LOUT = LO)	—	150	200		V_{IN}=0 V
I_{LIN+} (66,67,68)	Input bias current (LOUT = HI)	—	—	3		V_{IN}=4 V
I_{LIN-} (66,67,68)	Input bias current (LOUT = LO)	—	—	3		V_{IN}=0 V
I_{HIN+} (6,63,65)	Input bias current (HOUT = HI)	—	110	150		V_{IN}=4 V
I_{HIN-} (6,63,65)	Input bias current (HOUT = LO)	—	150	200		V_{IN}=0 V
I_{HIN+} (62)	Input bias current (HOUT = HI)	—	5	20		V_{IN}=4 V
I_{HIN-} (62)	Input bias current (HOUT = LO)	—	—	3		V_{IN}=0 V
I_{HIN+} (66,67,68)	Input bias current (HOUT = HI)	—	—	3		V_{IN}=4 V
I_{HIN-} (66,67,68)	Input bias current (HOUT = LO)	—	—	3		V_{IN}=0 V
I_{ITRIP+}	“High” ITRIP input bias current	—	5	40		V_{IN}=4 V
I_{ITRIP-}	“Low” ITRIP input bias current	—	—	1		V_{IN}=0 V
I_{EN+}	“High” ENABLE input bias current	—	5	40		V_{IN}=4 V
I_{EN-}	“Low” ENABLE input bias current	—	—	1		V_{IN}=0 V

Static Electrical Characteristics - (Continued)

V_{BIAS} (V_{CC},$V_{BS1,2,3}$) = 15 V unless otherwise specified. The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels ($\overline{HIN1,2,3}$/HIN1,2,3 and LIN1,2,3). The V_O and I_O parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: LO1,2,3 and HO1,2,3.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
I_{RCIN}	RCIN input bias current	—	—	1	µA	V_{RCIN}= 0 V or 15 V
I_{O+}	Output high short circuit pulsed current	120	200	—	mA	Vo =0 V, PW ≤10 µs
I_{O-}	Output low short circuit pulsed current	250	350	—		Vo =15 V, PW ≤10 µs
R_{on_RCIN}	RCIN low on resistance	—	50	100	Ω	I= 1.5 mA
R_{on_FAULT}	$\overline{FAULT}$ low on resistance	—	50	100		
R_{BS}	Internal BS diode R_{ON}	—	200	—		

Note 1: Please refer to Feature Description section for integrated bootstrap functionality information.

Dynamic Electrical Characteristics

Dynamic Electrical Characteristics V_{CC} = V_{BS} = V_{BIAS} = 15 V, $V_{S1,2,3}$ = V_{SS} = COM, T_A = 25 °C and CL = 1000 pF unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	400	530	750	ns	V_{IN} = 0 V & 5 V
t_{off}	Turn-off propagation delay	400	530	750		
t_{on} (66,67)	Turn-on propagation delay	—	200	—		
t_{off}(66,67)	Turn-off propagation delay	—	200	—		
t_r	Turn-on rise time	—	125	190		
t_f	Turn-off fall time	—	50	75		
t_{EN}	ENABLE low to output shutdown propagation delay	350	460	650		V_{IN}, V_{EN} = 0 V or 5 V
t_{EN} (66,67)	ENABLE low to output shutdown propagation delay	—	300	—		
t_{ITRIP}	ITRIP to output shutdown propagation delay	500	750	1200		V_{ITRIP} =5 V
t_{bl}	ITRIP blanking time	—	400	—		V_{IN} = 0 V or 5 V V_{ITRIP} = 5 V
t_{FLT}	ITRIP to $\overline{FAULT}$ propagation delay	400	600	950		
t_{FILIN}	Input filter time (HIN, LIN) (IRS213(6,62,63,65,68)D only)	200	350	510		V_{IN} = 0 V & 5 V
$t_{filterEN}$	Enable input filter time (IRS213(6,62,63,65,68)D only)	100	200	—		
DT	Deadtime	190	290	420		V_{IN} = 0 V & 5 V external dead time
MT	t_{on}, t_{off} matching time (on all six channels)	—	—	50		External dead time >420 ns
MDT	DT matching (Hi->Lo & Lo->Hi on all channels)	—	—	60		External dead time 0 s
PM	Pulse width distortion (pwin-pwout)	—	—	75		PW input=10 µs
t_{FLTCLR}	$\overline{FAULT}$ clear time RCIN: R = 2 MΩ, C = 1 nF	1.3	1.65	2	ms	V_{IN} = 0 V or 5 V V_{ITRIP} = 0 V

Note 2: For high side PWM, HIN pulse width must be ≥ 500 ns.

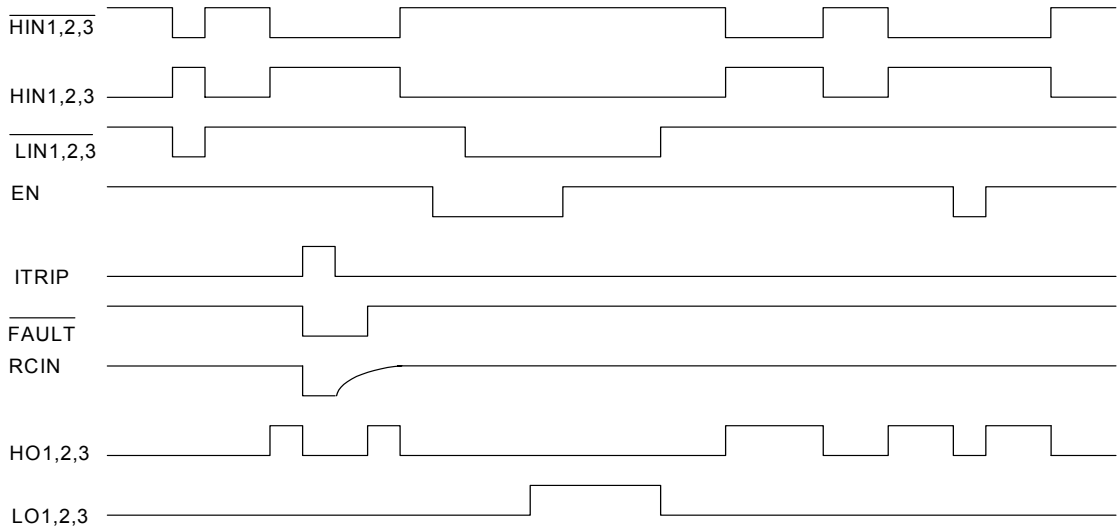


Fig. 1. Input/Output Timing Diagram

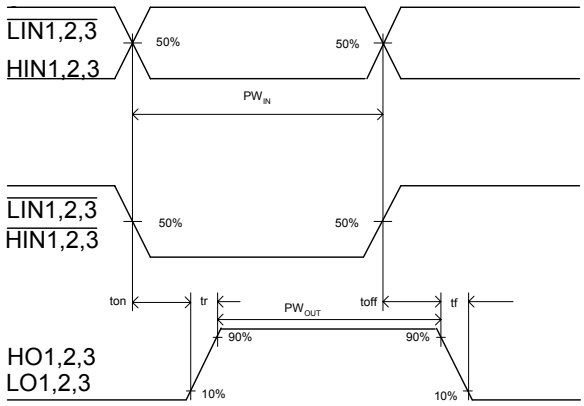


Fig. 2. Switching Time Waveforms

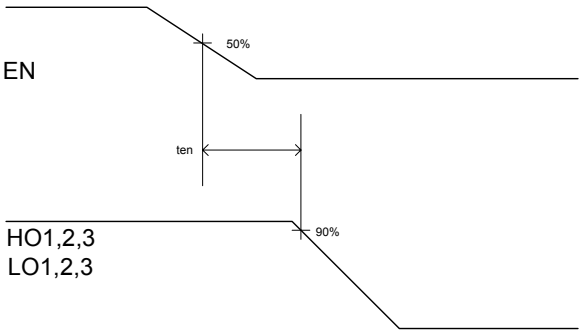


Fig. 3. Output Enable Timing Waveform

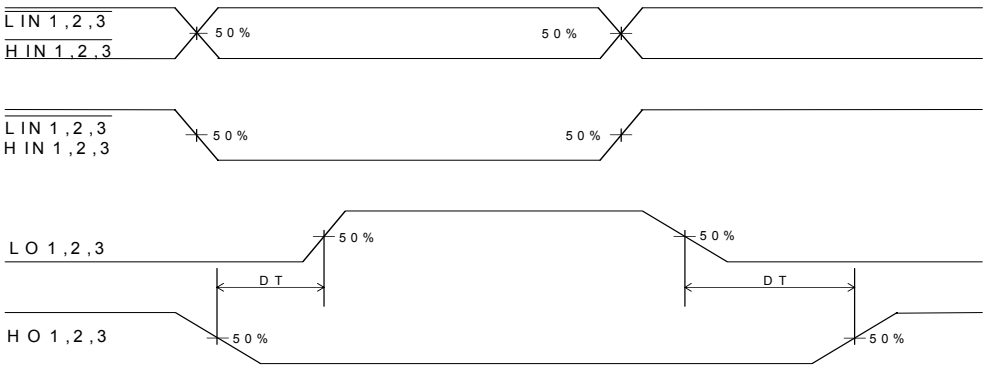


Fig. 4. Internal Deadtime Timing Waveforms

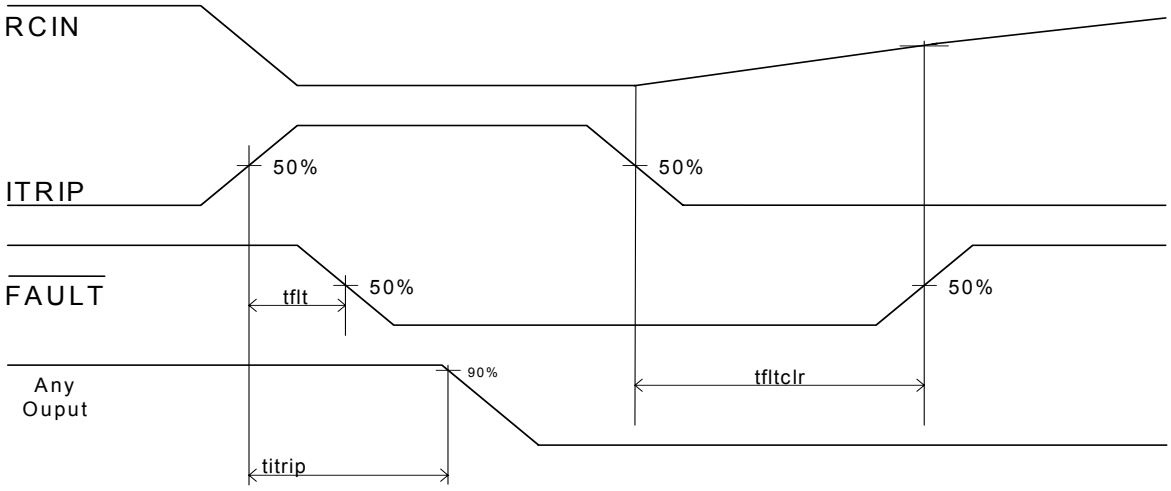


Fig. 5. ITRIP/RCIN Timing Waveforms

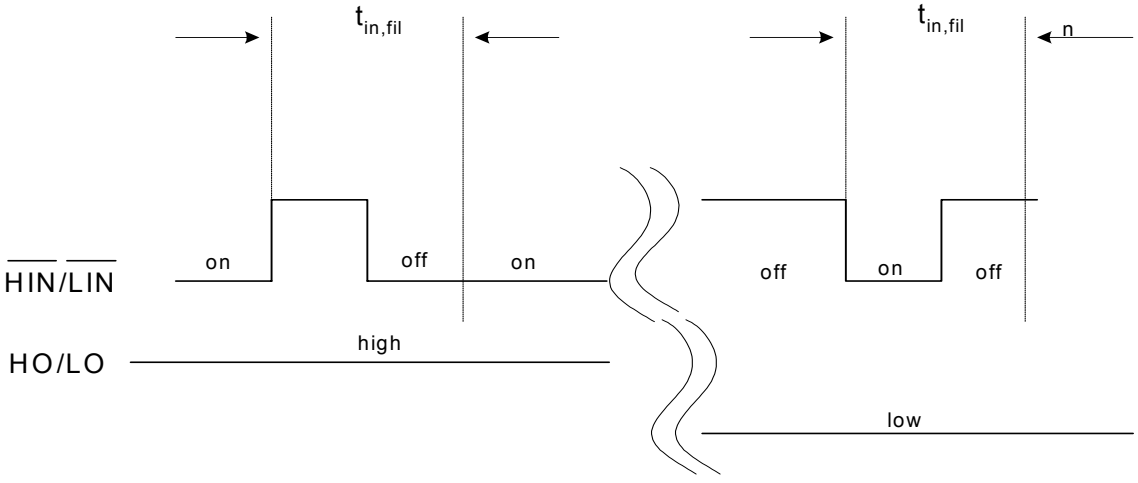


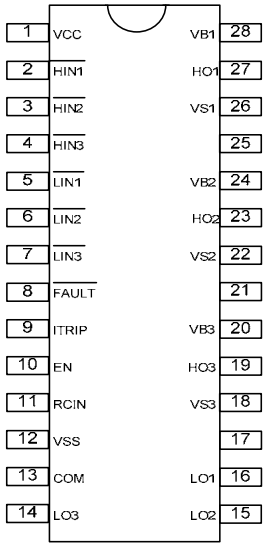
Fig. 6. Input Filter Function

Lead Definitions

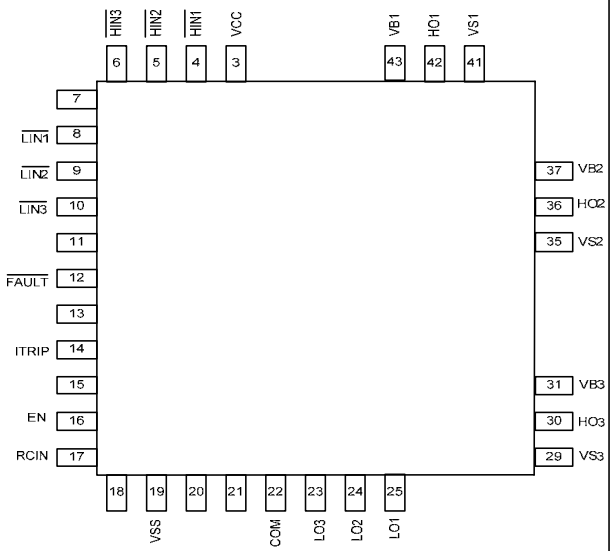
Symbol	Description
V_{CC}	Low side supply voltage
V_{SS}	Logic ground
$\overline{HIN1,2,3}$ HIN1,2,3	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase [IRS213(6,63,65,66,67,68)D] Logic inputs for high side gate driver outputs (HO1,2,3), in phase (IRS21362D)
$\overline{LIN1,2,3}$	Logic input for low side gate driver outputs (LO1,2,3), out of phase
$\overline{FAULT}$	Indicates over-current (ITRIP) or low-side undervoltage lockout has occurred. Negative logic, open-drain output
EN	Logic input to enable I/O functionality. I/O logic functions when ENABLE is high (i.e., positive logic) No effect on $\overline{FAULT}$ and not latched
ITRIP	Analog input for overcurrent shutdown. When active, ITRIP shuts down outputs and activates $\overline{FAULT}$ and RCIN low. When ITRIP becomes inactive, FAULT stays active low for an externally set time T_{FLTCLR}, then automatically becomes inactive (open-drain high impedance).
RCIN	External RC network input used to define FAULT CLEAR delay, $T_{FLTCLR,}$ approximately equal to R*C When RCIN>8 V, the $\overline{FAULT}$ pin goes back into open-drain high-impedance
COM	Low side gate drivers return
$V_{B1,2,3}$	High side floating supply
HO1,2,3	High side gate driver outputs
$V_{S1,2,3}$	High voltage floating supply return
LO1,2,3	Low side driver sourcing outputs

Note: LIN, HIN, EN, and ITRIP are internally clamped with a 5.2 V zener diode.

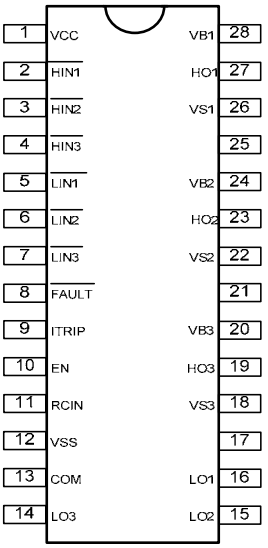
Lead Assignments



28 Lead PDIP

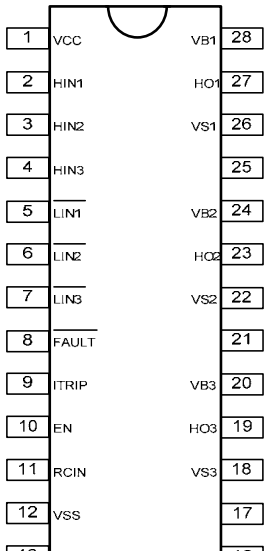


44 Lead PLCC w/o 12 leads

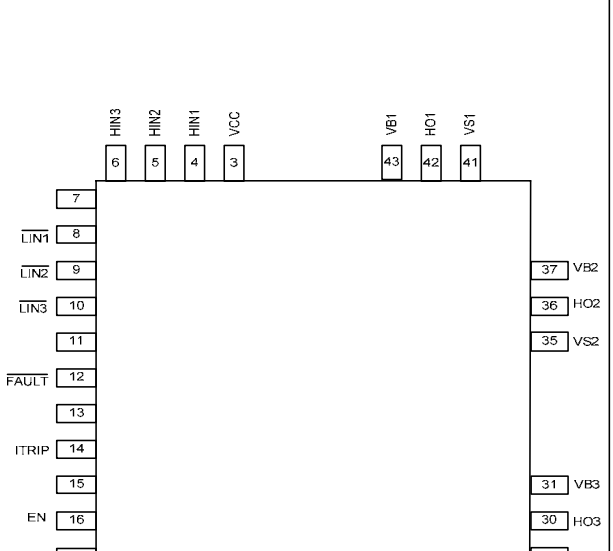


28 Lead SOIC (wide body)

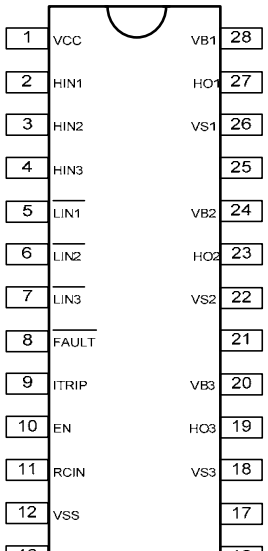
IRS213(6, 63, 65, 66, 67,68)D	IRS213(6, 63, 65, 66, 67,68)DJ	IRS213(6, 63, 65, 66, 67,68)DS



28 Lead PDIP



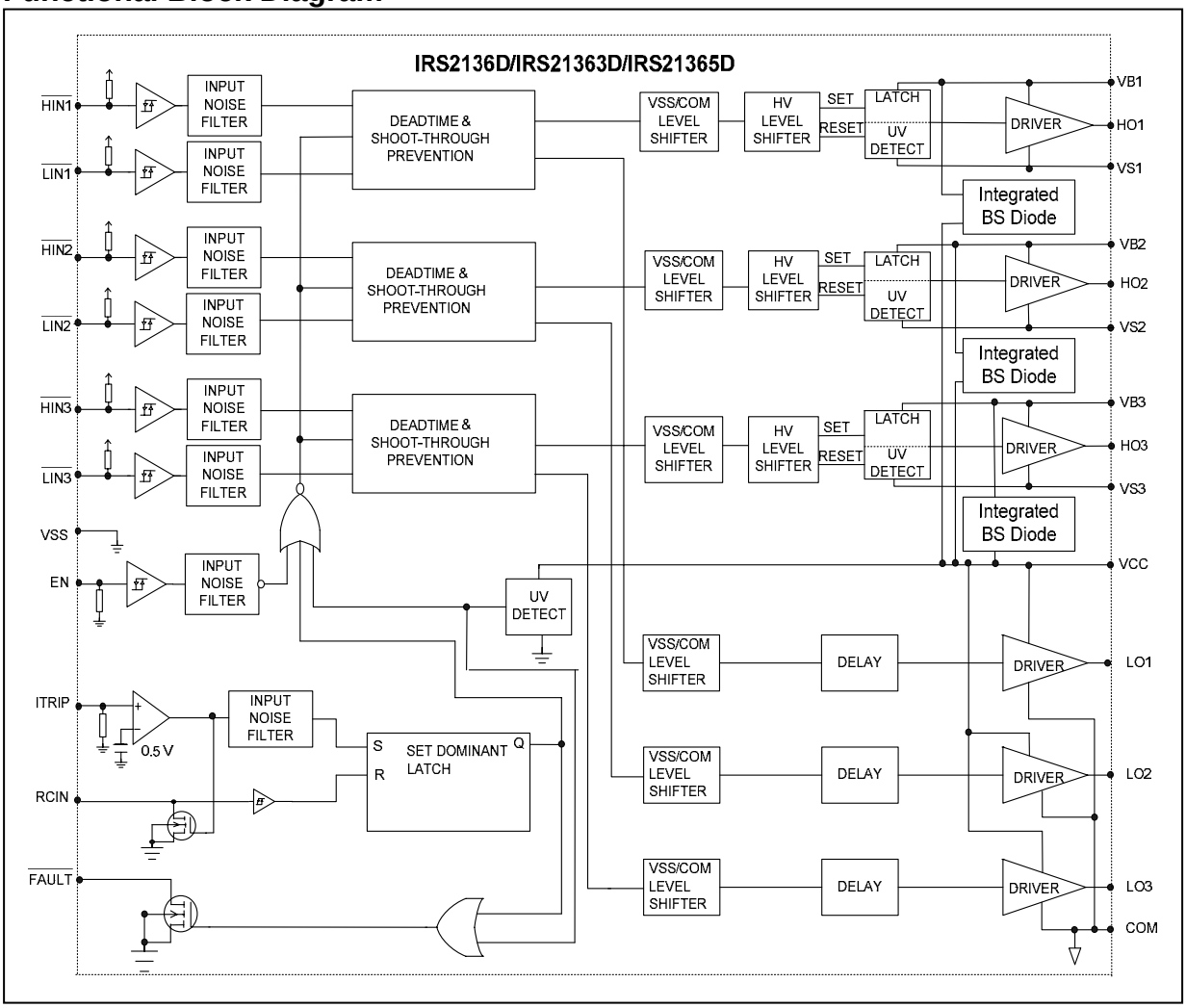
44 Lead PLCC w/o 12 leads



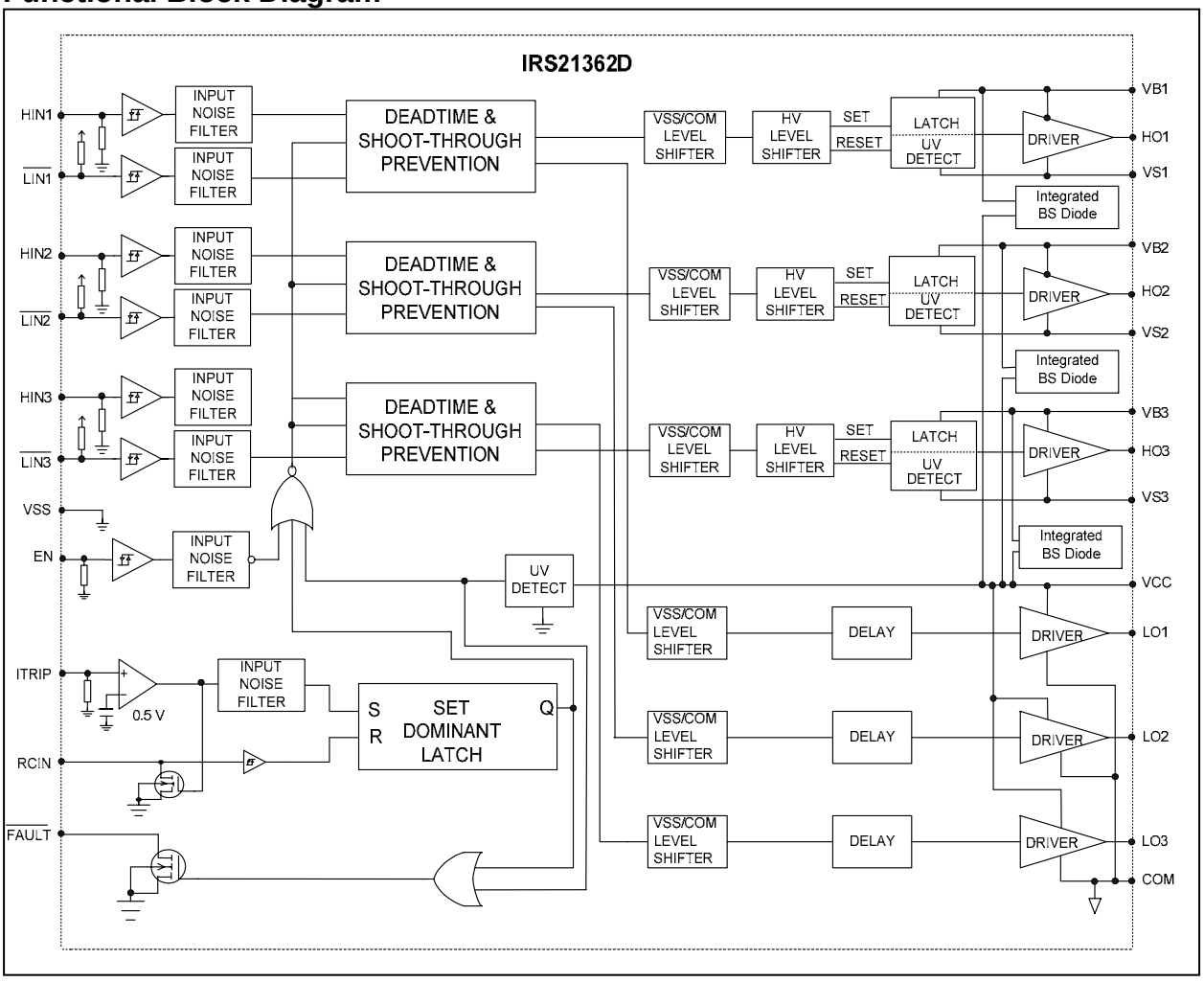
28 Lead SOIC (wide body)

IRS21362D	IRS21362DJ	IRS21362DS

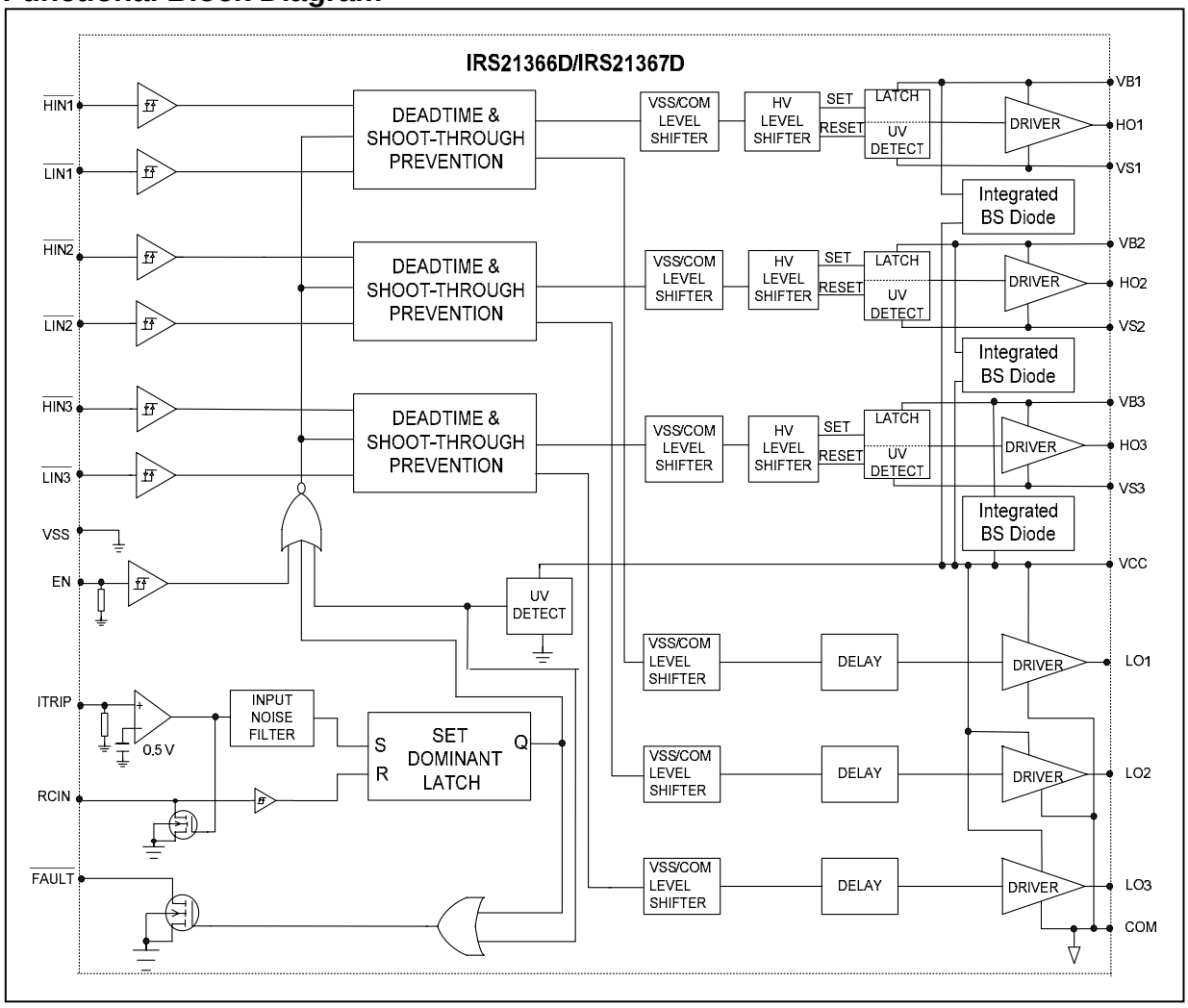
Functional Block Diagram



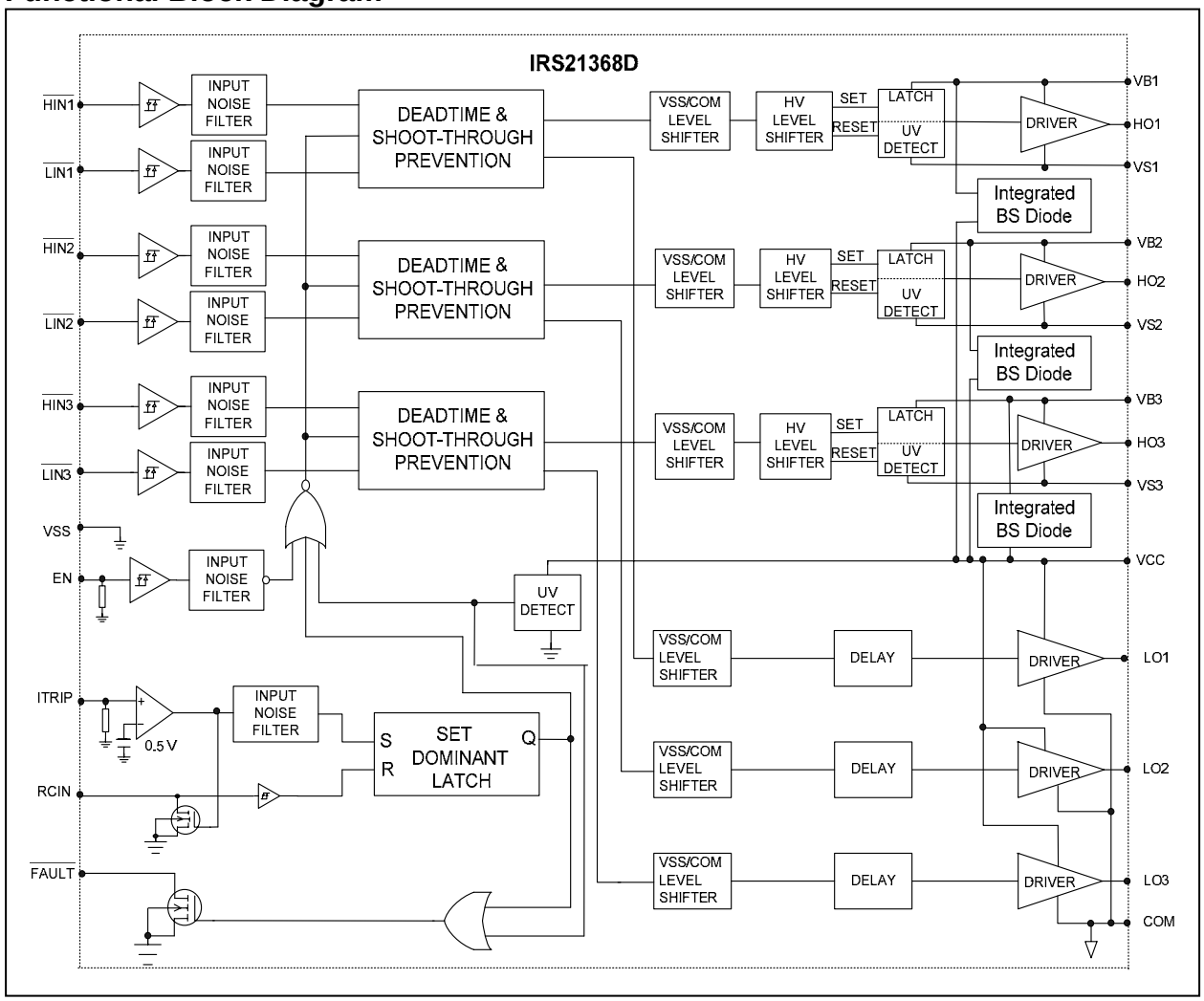
Functional Block Diagram



Functional Block Diagram



Functional Block Diagram



VCC	VBS	ITRIP	ENABLE	FAULT	LO1,2,3	HO1,2,3
<UVCC	X	X	X	0 (note 1)	0	0
15 V	<UVBS	0 V	5 V	high imp	LIN1,2,3	0 (note 2)
15 V	15 V	0 V	5 V	high imp	LIN1,2,3	HIN1,2,3
15 V	15 V	>V_{ITRIP}	5 V	0 (note 3)	0	0
15 V	15 V	0 V	0 V	high imp	0	0

Note 1: A shoot-through prevention logic prevents LO1,2,3 and HO1,2,3 for each channel from turning on simultaneously.
Note 2: UVCC is not latched, when V_{CC} > UVCC, $\overline{FAULT}$ returns to high impedance.
Note 3: When V_{BS} < UVBS, HO goes low. After V_{BS} goes higher than UVBS, HO stays low until a new falling IRS213(6,63,65,66,67,68)D or rising IRS21362D transition of HIN.
Note 4: When ITRIP < V_{ITRIP}, $\overline{FAULT}$ returns to high-impedance after RCIN pin becomes greater than 8 V (@ V_{CC} = 15 V).

1 Features Description

1.1 Integrated Bootstrap Functionality

The IRS2136xD family embeds an integrated bootstrap FET that allows an alternative drive of the bootstrap supply for a wide range of applications.

There is one bootstrap FET for each channel and it is connected between each of the floating supply (V_{B1}, V_{B2}, V_{B3}) and V_{CC} (see Fig. 7).

The bootstrap FET of each channel follows the state of the respective low side output stage (i.e., bootFet is ON when LO is high, it is OFF when LO is low), unless the V_B voltage is higher than approximately 1.1(V_{CC}). In that case the bootstrap FET stays off until the V_B voltage returns below that threshold (see Fig. 8).

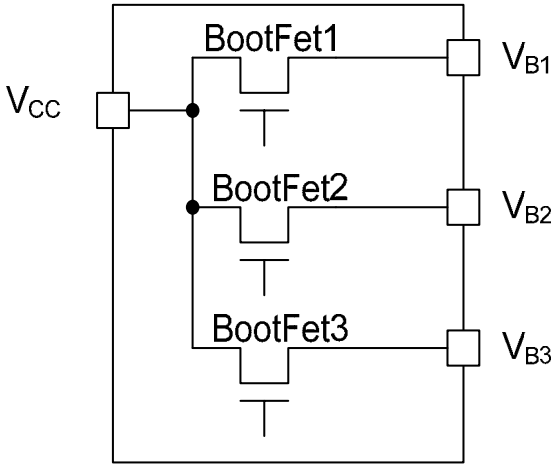


Fig. 7. Simplified BootFet Connection

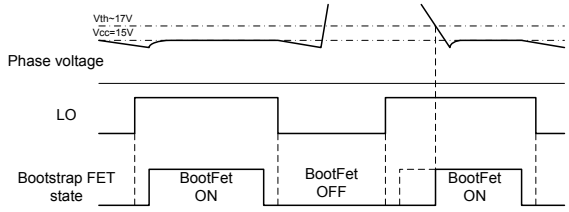


Fig. 8. State Diagram

Bootstrap FET is suitable for most PWM modulation schemes and can be used either in parallel with the external bootstrap network (diode+resistor) or as a replacement of it. The use of the integrated bootstrap as a replacement of the external bootstrap network may have some limitations in the following situations:

- when used in non-complementary PWM schemes (typically 6-step modulations)
- at a very high PWM duty cycle due to the bootstrap FET equivalent resistance (R_{BS}, see page 5).

In these cases, better performances can be achieved by using the IRS2136x non D version with an external bootstrap network.

2 PCB Layout Tips

2.1 Distance from H to L Voltage

The IRS2136xDJ package lacks some pins (see page 8) in order to maximizing the distance between the high voltage and low voltage pins. It's strongly recommended to place the components tied to the floating voltage in the respective high voltage portions of the device ($V_{B1,2,3}$, $V_{S1,2,3}$) side.

2.2 Ground Plane

To minimize noise coupling ground plane must not be placed under or near the high voltage floating side.

2.3 Gate Drive Loops

Current loops behave like an antenna able to receive and transmit EM noise (see Fig. 9). In order to reduce EM coupling and improve the power switch turn on/off performances, gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to develop a voltage across the gate-emitter increasing the possibility of self turn-on effect.

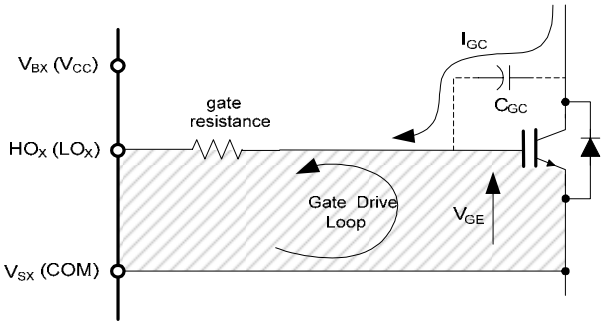


Fig. 9. Antenna Loops

2.4 Supply Capacitors

Supply capacitors must be placed as close as possible to the device pins (V_{CC} and V_{SS} for the ground tied supply, V_B and V_S for the floating supply) in order to minimize parasitic inductance/resistance.

2.5 Routing and Placement

Power stage PCB parasitic may generate dangerous voltage transients for the gate driver and the control logic. In particular it's recommended to limit phase voltage negative transients.

In order to avoid such undervoltage it is highly recommended to minimize high side emitter to low side collector distance and low side emitter to negative bus rail stray inductance. See DT04-4 at www.irf.com for more detailed information.

Figures 10-30 provide information on the experimental performance of the IRS2136DS HVIC. The line plotted in each figure is generated from actual lab data. A large number of individual samples from multiple wafer lots were tested at three temperatures (-40 ºC, 25 ºC, and 125 ºC) in order to generate the experimental (Exp.) curve. The line labeled Exp. consist of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

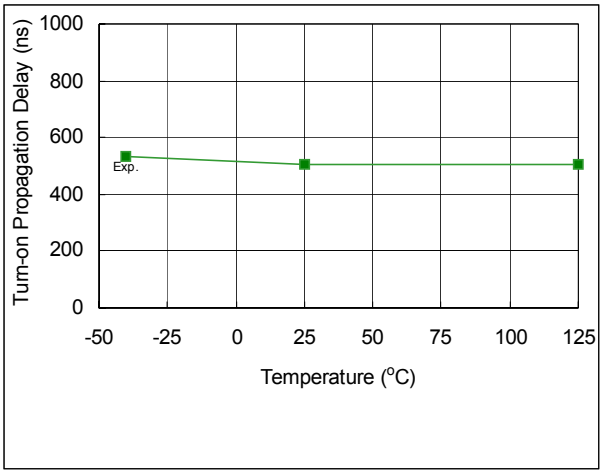


Fig. 10. Turn-On Propagation Delay vs. Temperature

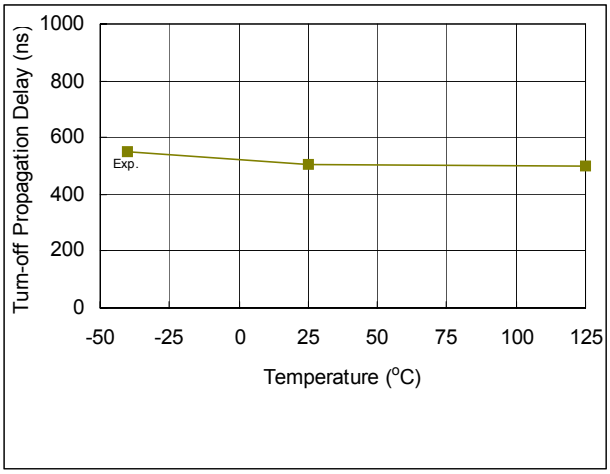


Fig. 11. Turn-Off Propagation Delay vs. Temperature

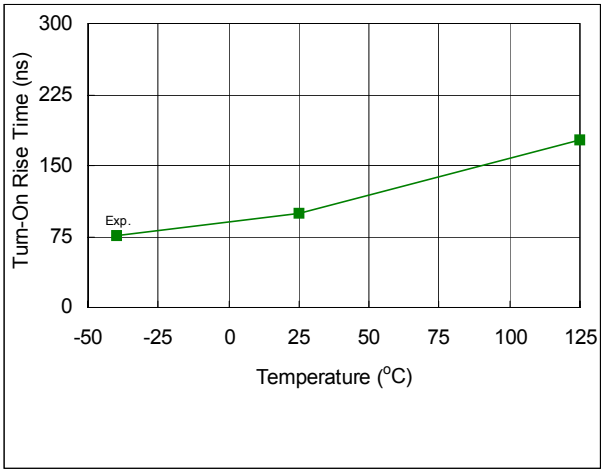


Fig. 12. Turn-On Rise Time vs. Temperature

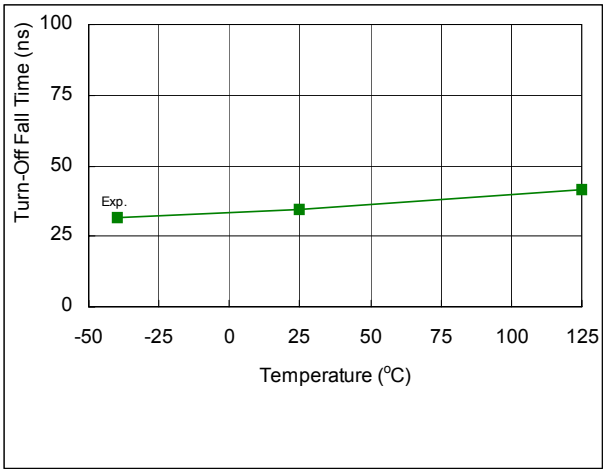


Fig. 13. Turn-Off Fall Time vs. Temperature

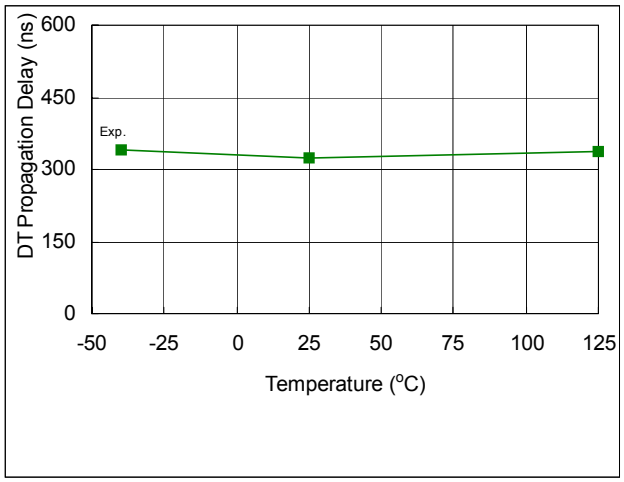


Fig. 14. DT Propagation Delay vs. Temperature

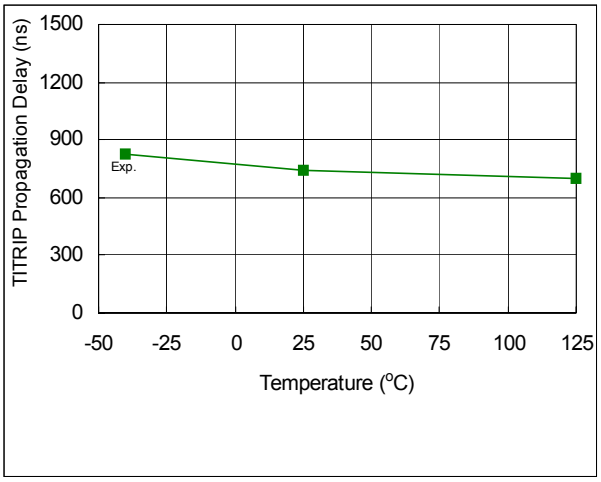


Fig. 15. TITRIP Propagation Delay vs. Temperature

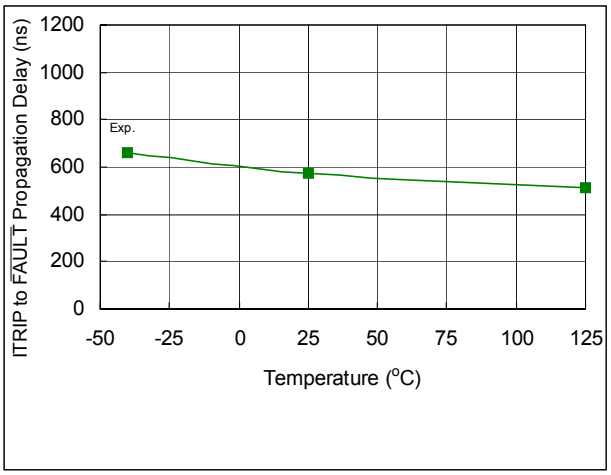


Fig. 16. ITRIP to $\overline{\text{FAULT}}$ Propagation Delay vs. Temperature

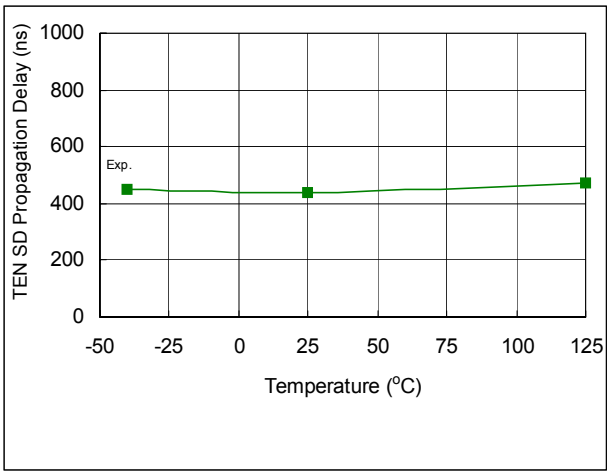


Fig. 17. TEN SD Propagation Delay vs. Temperature

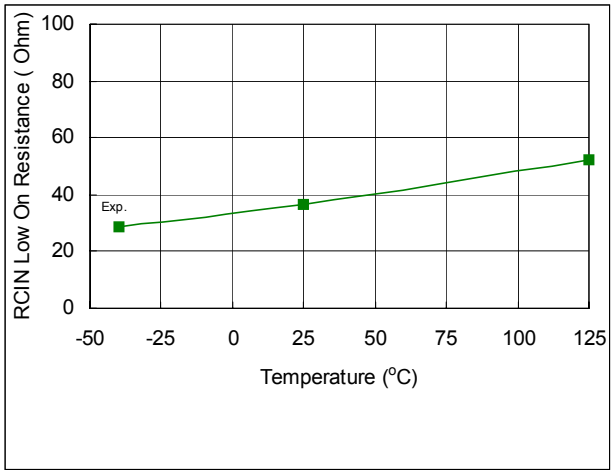


Fig. 18. RCIN Low On Resistance vs. Temperature

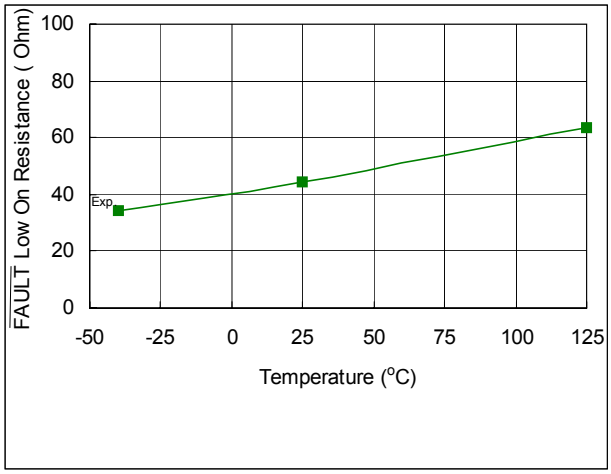


Fig. 19. $\overline{\text{FAULT}}$ Low On Resistance vs. Temperature

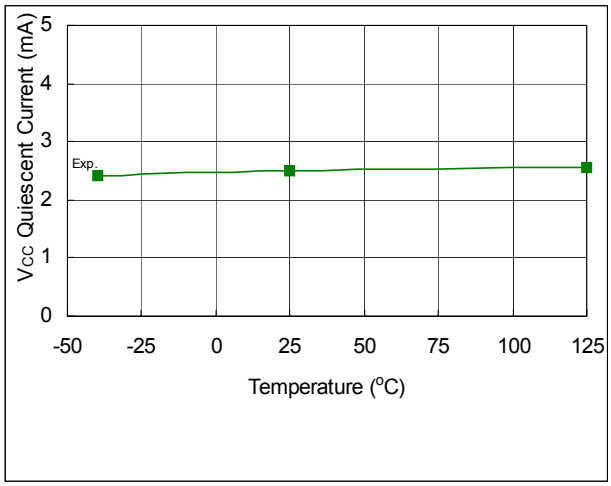


Fig. 20. V_{CC} Quiescent Current vs. Temperature

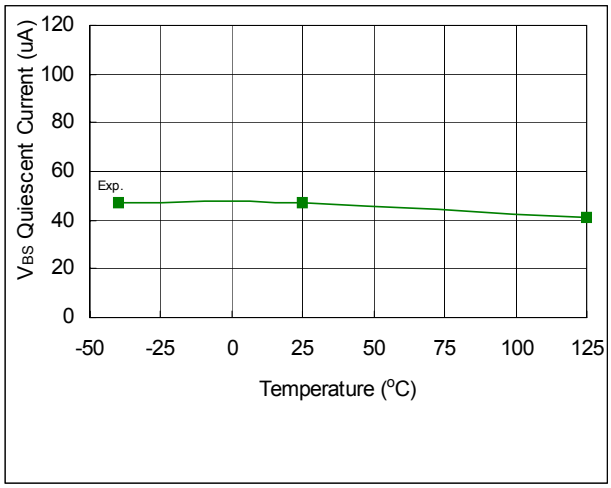


Fig. 21. V_{BS} Quiescent Current vs. Temperature

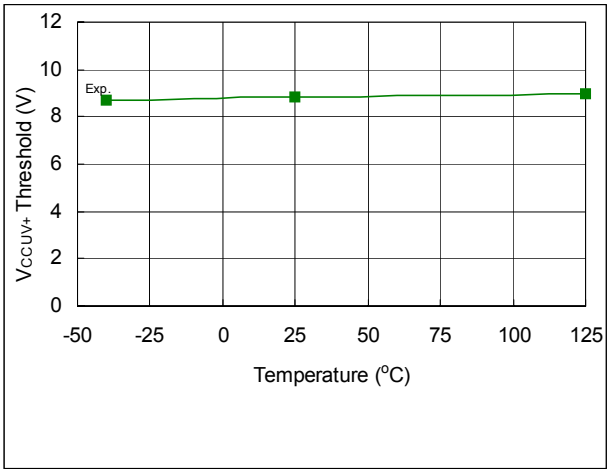


Fig. 22. V_{CCUV+} Threshold vs. Temperature

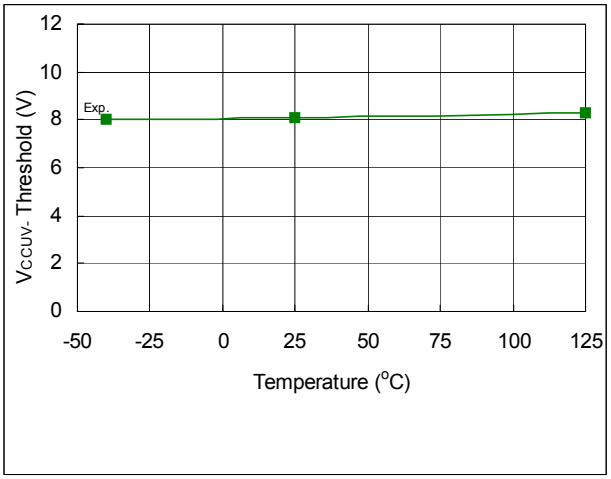


Fig. 23. V_{CCUV-} Threshold vs. Temperature

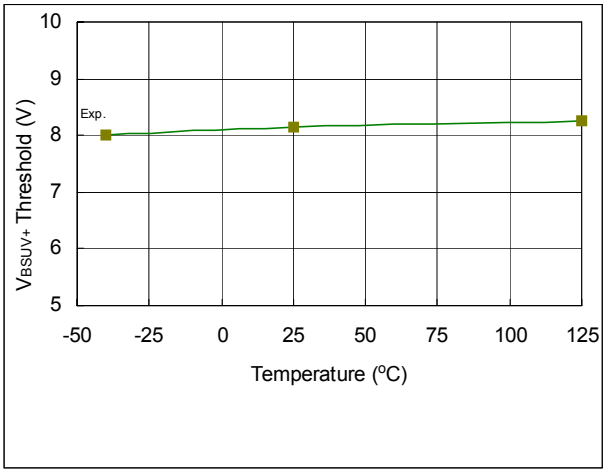


Fig. 24. V_{BSUV+} Threshold vs. Temperature

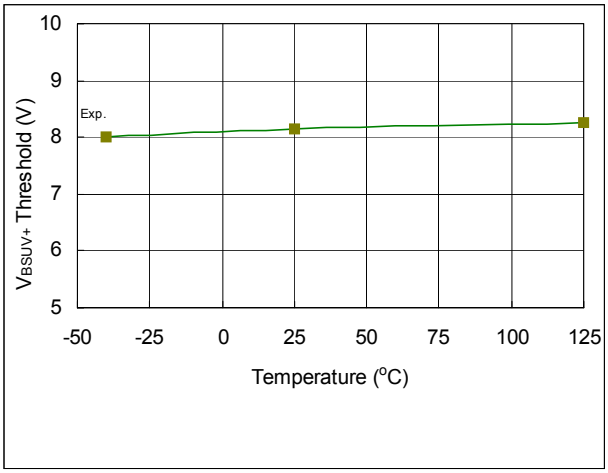


Fig. 25. V_{BSUV-} Threshold vs. Temperature

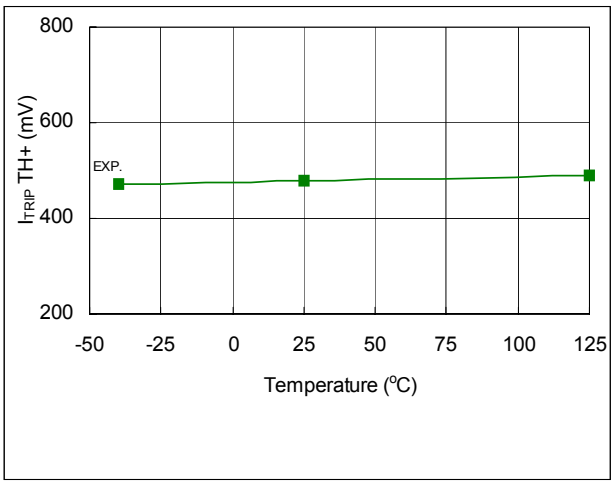


Fig. 26. I_{TRIP} TH+ vs. Temperature

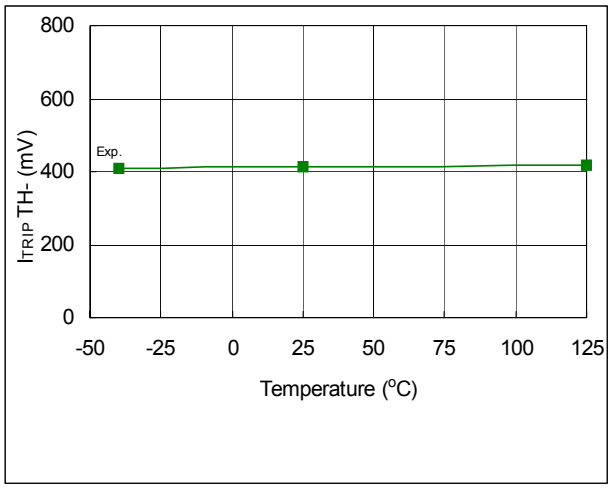


Fig. 27. I_{TRIP} TH- vs. Temperature

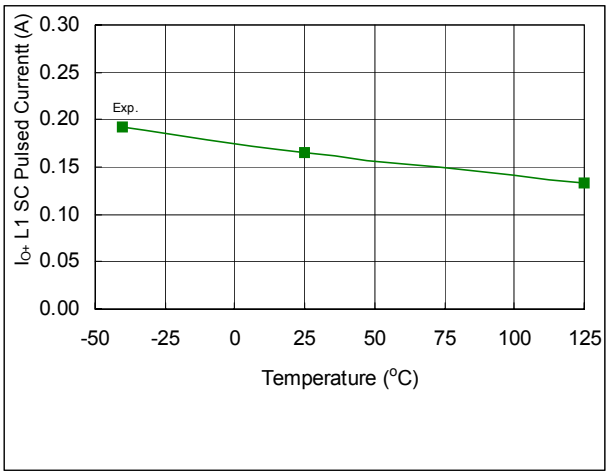


Fig. 28. I_{O+} L1 SC Pulsed Current vs. Temperature

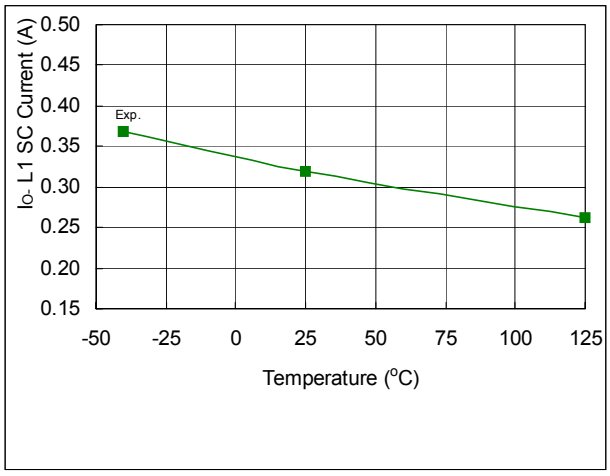


Fig. 29. I_{O-} L1 SC Pulsed Current vs. Temperature

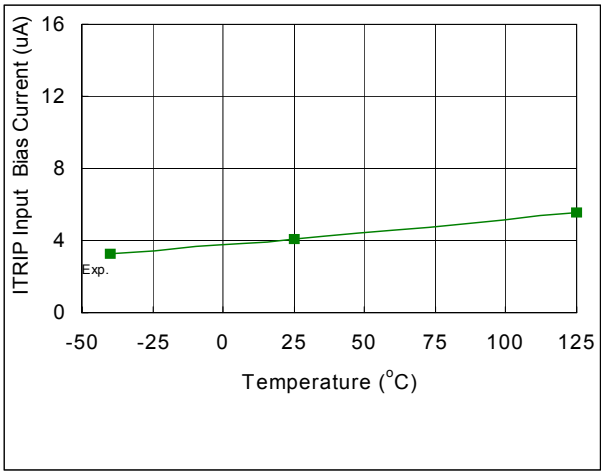
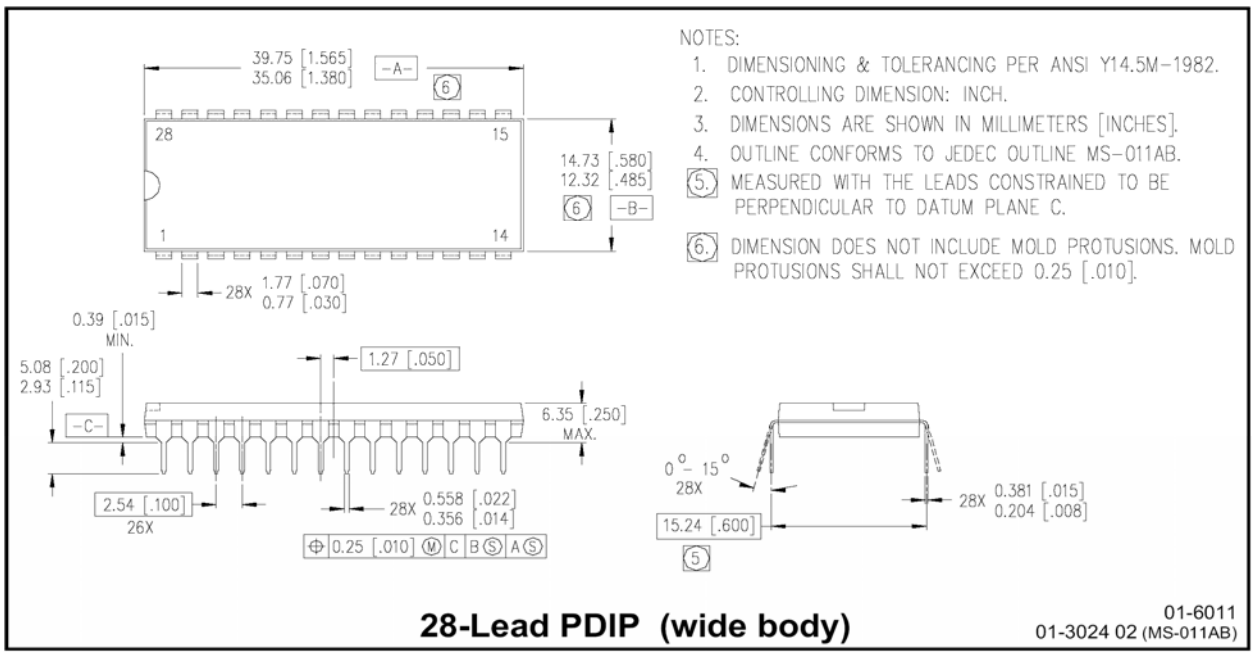
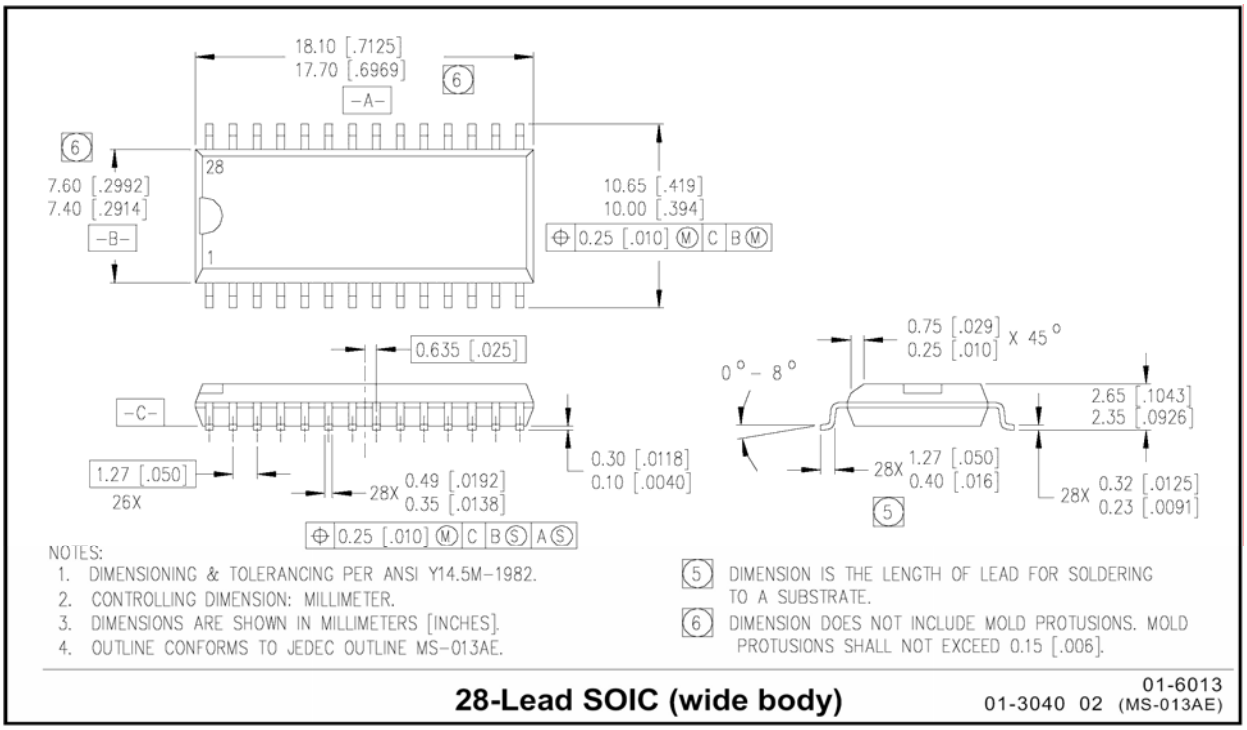


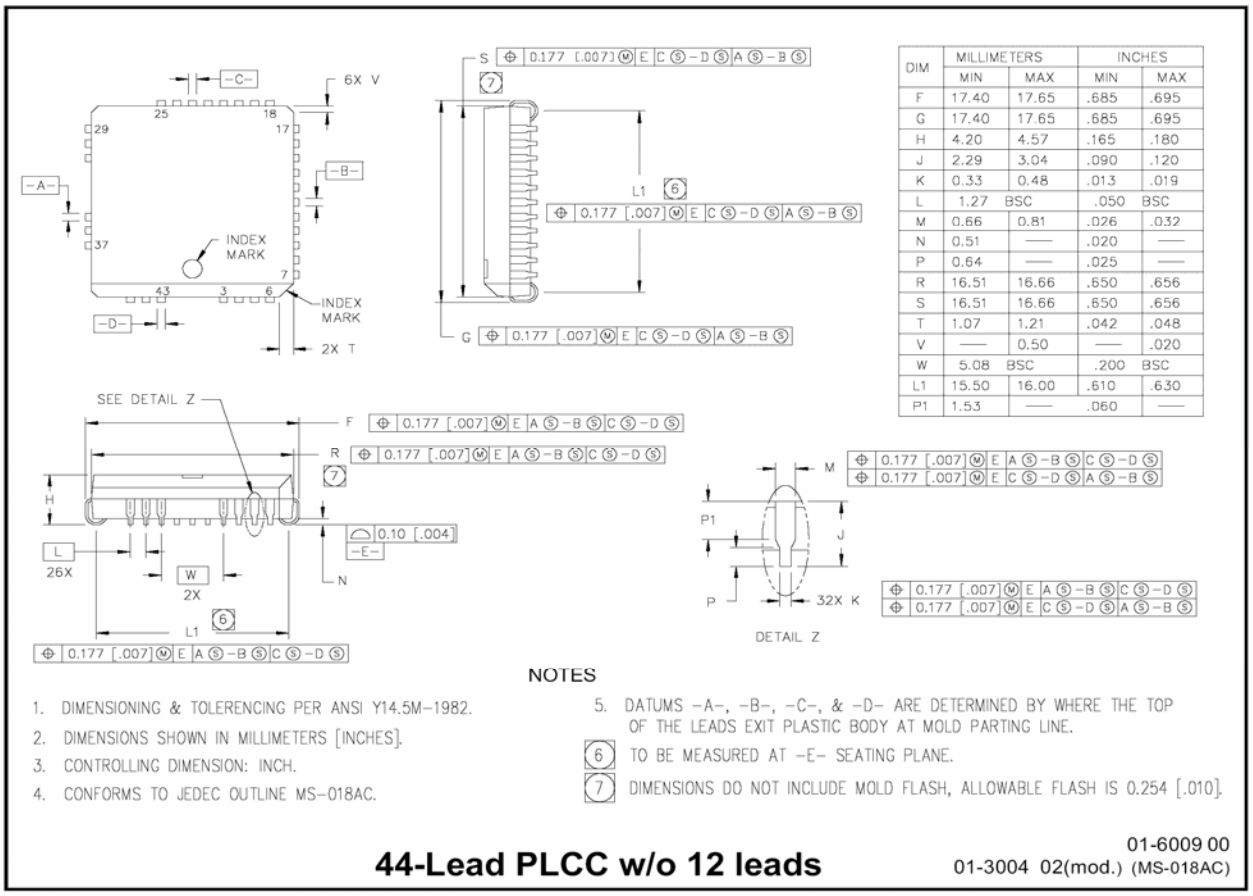
Fig. 30. ITRIP Input Bias Current vs. Temperature

Case Outlines





Case Outlines



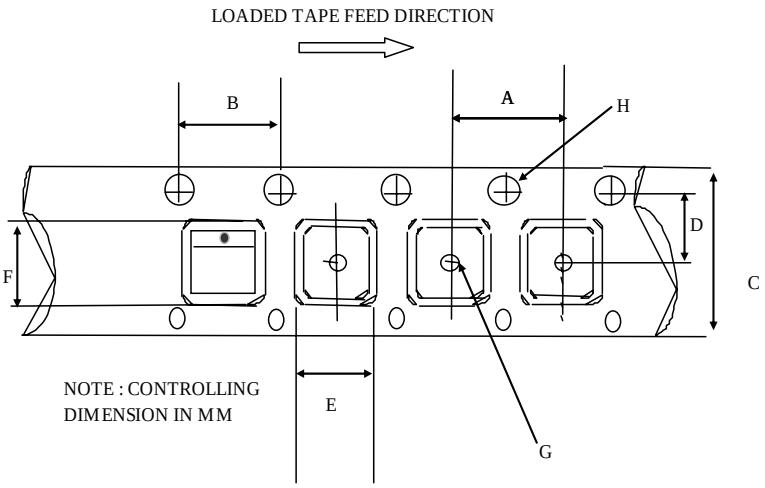
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F	17.40	17.65	.685	.695
G	17.40	17.65	.685	.695
H	4.20	4.57	.165	.180
J	2.29	3.04	.090	.120
K	0.33	0.48	.013	.019
L	1.27 BSC		.050 BSC	
M	0.66	0.81	.026	.032
N	0.51	—	.020	—
P	0.64	—	.025	—
R	16.51	16.66	.650	.656
S	16.51	16.66	.650	.656
T	1.07	1.21	.042	.048
V	—	0.50	—	.020
W	5.08 BSC		.200 BSC	
L1	15.50	16.00	.610	.630
P1	1.53	—	.060	—

NOTES

1. DIMENSIONING & TOLERENCING PER ANSI Y14.5M–1982.
2. DIMENSIONS SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE MS–018AC.
5. DATUMS –A–, –B–, –C–, & –D– ARE DETERMINED BY WHERE THE TOP OF THE LEADS EXIT PLASTIC BODY AT MOLD PARTING LINE.
6. TO BE MEASURED AT –E– SEATING PLANE.
7. DIMENSIONS DO NOT INCLUDE MOLD FLASH, ALLOWABLE FLASH IS 0.254 [.010].

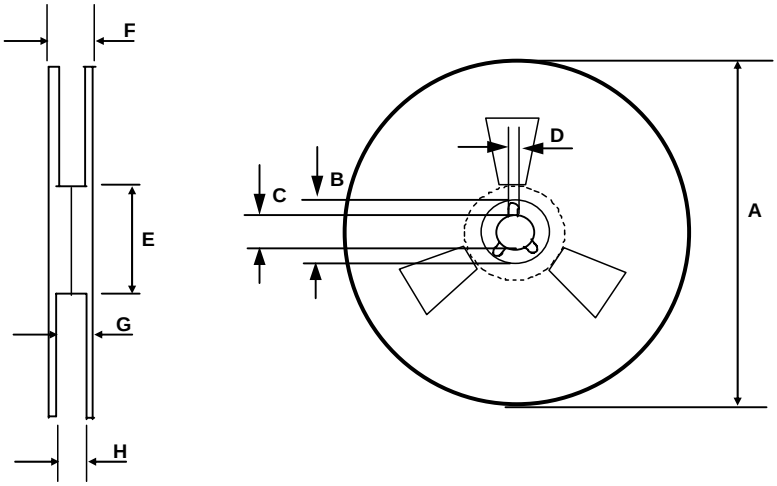
44-Lead PLCC w/o 12 leads

01-6009 00
01-3004 02(mod.) (MS-018AC)



CARRIER TAPE DIMENSION FOR 44PLCC

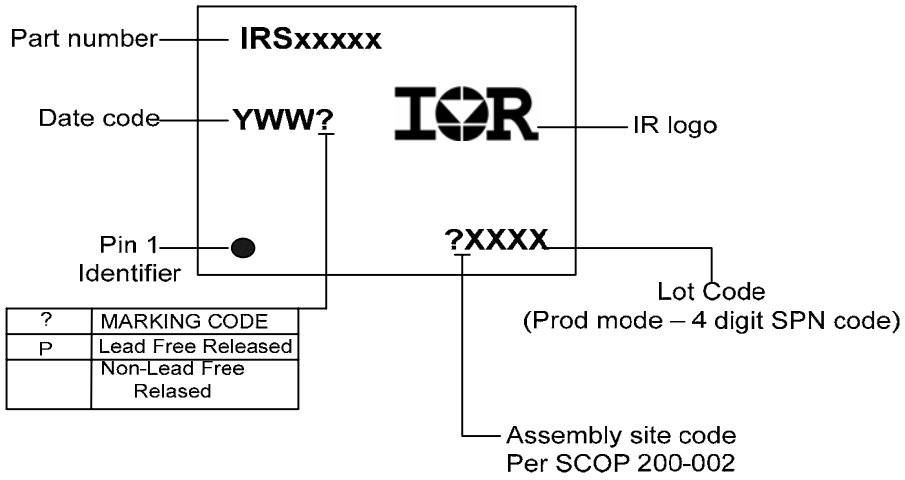
Code	Metric		Imperial	
	Min	Max	Min	Max
A	23.90	24.10	0.94	0.948
B	3.90	4.10	0.153	0.161
C	31.70	32.30	1.248	1.271
D	14.10	14.30	0.555	0.562
E	17.90	18.10	0.704	0.712
F	17.90	18.10	0.704	0.712
G	2.00	n/a	0.078	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 44PLCC

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	38.4	n/a	1.511
G	34.7	35.8	1.366	1.409
H	32.6	33.1	1.283	1.303

LEAD-FREE PART MARKING INFORMATION



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Relased

ORDER INFORMATION

28-Lead PDIP IRS2136DPbF
28-Lead PDIP IRS21362DPbF
28-Lead PDIP IRS21363DPbF
28-Lead PDIP IRS21365DPbF
28-Lead PDIP IRS21366DPbF
28-Lead PDIP IRS21367DPbF
28-Lead PDIP IRS21368DPbF
28-Lead SOIC IRS2136DSPbF
28-Lead SOIC IRS21362DSPbF
28-Lead SOIC IRS21363DSPbF
28-Lead SOIC IRS21365DSPbF
28-Lead SOIC IRS21366DSPbF
28-Lead SOIC IRS21367DSPbF
28-Lead SOIC IRS21368DSPbF
44-Lead PLCC IRS2136DJPbF
44-Lead PLCC IRS21362DJPbF
44-Lead PLCC IRS21363DJPbF
44-Lead PLCC IRS21365DJPbF
44-Lead PLCC IRS21366DJPbF
44-Lead PLCC IRS21367DJPbF
44-Lead PLCC IRS21368DJPbF

28-Lead SOIC Tape & Reel IRS2136DSTRPbF
28-Lead SOIC Tape & Reel IRS21362DSTRPbF
28-Lead SOIC Tape & Reel IRS21363DSTRPbF
28-Lead SOIC Tape & Reel IRS21365DSTRPbF
28-Lead SOIC Tape & Reel IRS21366DSTRPbF
28-Lead SOIC Tape & Reel IRS21367DSTRPbF
28-Lead SOIC Tape & Reel IRS21368DSTRPbF
44-Lead PLCC Tape & Reel IRS2136DJTRPbF
44-Lead PLCC Tape & Reel IRS21362DJTRPbF
44-Lead PLCC Tape & Reel IRS21363DJTRPbF
44-Lead PLCC Tape & Reel IRS21365DJTRPbF
44-Lead PLCC Tape & Reel IRS21366DJTRPbF
44-Lead PLCC Tape & Reel IRS21367DJTRPbF
44-Lead PLCC Tape & Reel IRS21368DJTRPbF

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This part has been qualified per industrial level
http://www.irf.com Data and specifications subject to change without notice. 5/19/2006