International TOR Rectifier RADIATION HARDENED POWER MOSFET

IRHMJ7250 200V, N-CHANNEL

RAD Hard[™]HEXFET[®] TECHNOLOGY

SURFACE MOUNT (TO-254AA Tabless)

Product Summary

Part Number	Radiation Level	RDS(on)	ID
IRHMJ7250	100K Rads (Si)	0.10Ω	26A
IRHMJ3250	300K Rads (Si)	0.10Ω	26A
IRHMJ4250	600K Rads (Si)	0.10Ω	26A
IRHMJ8250	1000K Rads (Si)	0.10Ω	26A

International Rectifier's RADHard HEXFET® technology provides high performance power MOSFETs for space applications. This technology has over a decade of proven performance and reliability in satellite applications. These devices have been characterized for both Total Dose and Single Event Effects (SEE). The combination of low Rdson and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.



Features:

- Single Event Effect (SEE) Hardened
- Low RDS(on)
- Low Total Gate Charge
- Proton Tolerant
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Ceramic Eyelets
- Light Weight

Absolute Maximum Ratings

Pre-Irradiation

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	Parameter		Units
ID @ VGS = 12V, TC = 25°C	Continuous Drain Current	26	
I _D @ V _{GS} = 12V, T _C = 100°C	Continuous Drain Current	16	Α
IDM	Pulsed Drain Current ①	104	
P _D @ T _C = 25°C	Max. Power Dissipation	150	W
	Linear Derating Factor	1.2	W/°C
VGS	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy ②	500	mJ
^I AR	Avalanche Current ①	26	Α
EAR	Repetitive Avalanche Energy ①	15	mJ
dv/dt	Peak Diode Recovery dv/dt 3	5.0	V/ns
TJ	Operating Junction	-55 to 150	
TSTG	Storage Temperature Range		°C
	Pckg. Mounting Surface Temp.	300 (for 5s)	
	Weight	8.0 (Typical)	g

For footnotes refer to the last page

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min	Тур	Max	Units	Test Conditions	
BVDSS	Drain-to-Source Breakdown Voltage	200	_	_	V	Vgs =0 V, Ip = 1.0mA	
ΔBV _{DSS} /ΔT _J	Temperature Coefficient of Breakdown Voltage	_	0.27	_	V/°C	Reference to 25°C, I _D = 1.0mA	
R _{DS(on)}	Static Drain-to-Source	_	_	0.10		VGS = 12V, ID = 16A VGS = 12V, ID = 26A 4	
, ,	On-State Resistance	_	_	0.11	Ω	VGS = 12V, ID = 26A (4)	
VGS(th)	Gate Threshold Voltage	2.0	_	4.0	V	V _{DS} = V _{GS} , I _D = 1.0mA	
9fs	Forward Transconductance	8.0	_	_	S (75)	V _{DS} > 15V, I _{DS} = 16A ④	
IDSS	Zero Gate Voltage Drain Current	_	_	25		VDS= 160V,VGS=0V	
		_	_	250	μΑ	V _{DS} = 160V	
						VGS = 0V, TJ = 125°C	
IGSS	Gate-to-Source Leakage Forward	_	_	100	- 1	VGS = 20V	
IGSS	Gate-to-Source Leakage Reverse	_	_	-100	· nA	VGS = -20V	
Qg	Total Gate Charge	_	_	170		VGS = 12V, ID = 26A	
Qgs	Gate-to-Source Charge	_	_	30	nC	VDS = 100V	
Q _{gd}	Gate-to-Drain ('Miller') Charge	_	_	60			
td(on)	Turn-On Delay Time	_	_	33		$V_{DD} = 100V, I_{D} = 26A,$	
t _r	Rise Time	_	_	140	ns	$V_{GS} = 12V, R_{G} = 2.35\Omega$	
td(off)	Turn-Off Delay Time	_	_	140	1115		
tf	Fall Time	_	_	140			
LS + LD	Total Inductance	_	6.8	_	nH	Measured from drain lead (6mm/0.25in. from package) to source lead (6mm/0.25in. from package)	
Ciss	Input Capacitance		4700	_		VGS = 0V, VDS = 25V	
Coss	Output Capacitance	_	850	_	pF	f = 1.0MHz	
C _{rss}	Reverse Transfer Capacitance	_	210	_			

Source-Drain Diode Ratings and Characteristics

	Parameter			Тур	Max	Units	Test Conditions		
Is	Continuous Source Current (Body Diode)			_	26	۸			
ISM	Pulse Source Current (Body Diode) ①			_	104	Α			
VSD	Diode Forward Voltage		_	_	1.4	V	$T_j = 25$ °C, $I_S = 26A$, $V_{GS} = 0V$ ④		
trr	Reverse Recovery Time		_	_	820	nS	Tj = 25°C, IF = 26A, di/dt ≤100A/μs		
QRR	Reverse Recovery Charge		_	_	12	μC	V _{DD} ≤ 25V ④		
ton	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by LS + LD.							

Thermal Resistance

	Parameter	Min	Тур	Max	Units	Test Conditions
R _{th} JC	Junction-to-Case	-	_	0.83	°C/W	
RthCS	Case-to-sink	_	0.21	_	C/VV	
R _{th} JA	Junction-to-Ambient	-	_	48		Typical socket mount

Note: Corresponding Spice and Saber models are available on International Rectifier website.

For footnotes refer to the last page

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation 56

	Parameter	Up to 600K Rads(Si) ¹		1000K Rads (Si) ²		Units	Test Conditions
		Min	Min Max Min Max				
BV _{DSS}	Drain-to-Source Breakdown Voltage	200	_	200	_	V	$V_{GS} = 0V, I_D = 1.0mA$
V _{GS(th)}	Gate Threshold Voltage ④	2.0	4.0	1.25	4.5		$V_{GS} = V_{DS}$, $I_D = 1.0 \text{mA}$
I _{GSS}	Gate-to-Source Leakage Forward	_	100	_	100	nA	V _{GS} = 20V
IGSS	Gate-to-Source Leakage Reverse	_	-100	_	-100		V _{GS} = -20 V
IDSS	Zero Gate Voltage Drain Current	_	25	_	50	μΑ	V _{DS} =160V, V _{GS} =0V
R _{DS(on)}	Static Drain-to-Source 4	_	0.094	_	0.149	Ω	Vgs = 12V, I _D =16A
	On-State Resistance (TO-3)						
R _{DS(on)}	Static Drain-to-Source 4		0.10	_	0.155	Ω	Vgs = 12V, I _D =16A
` ′	On-State Resistance (TO-254AA)						
V _{SD}	Diode Forward Voltage ④	_	1.4		1.4	V	V _{GS} = 0V, I _S = 26A

^{1.} Part numbers IRHMJ7250, IRHMJ3250 and IRHMJ4250

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Single Event Effect Safe Operating Area

Ion	LET	Energy	Range	VDS(V)						
	MeV/(mg/cm ²))	(MeV)	(µm)	@VGS=0V	@VGS=-5V	@VGS=-10V	@VGS=-15V	@VGS=-20V		
Cu	28	285	43	190	180	170	125			
Br	36.8	305	39	100	100	100	50	_		

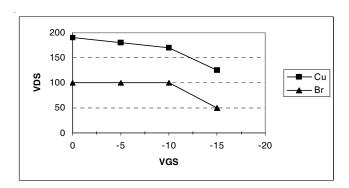
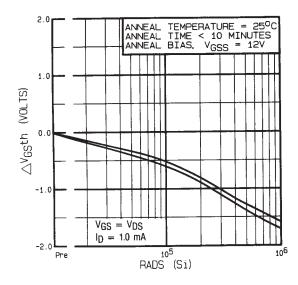


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page

^{2.} Part number IRHMJ8250



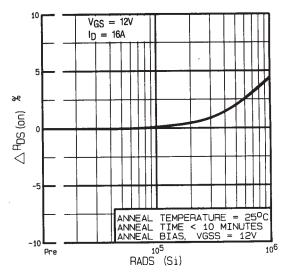
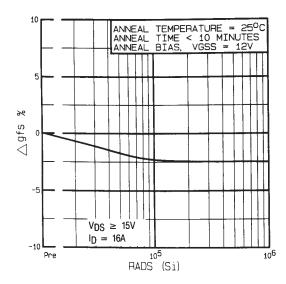
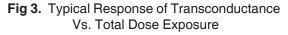


Fig 1. Typical Response of Gate Threshhold Voltage Vs. Total Dose Exposure

Fig 2. Typical Response of On-State Resistance Vs. Total Dose Exposure





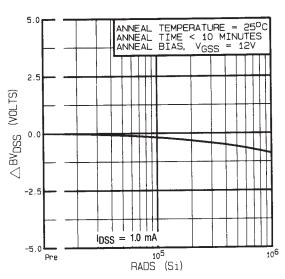
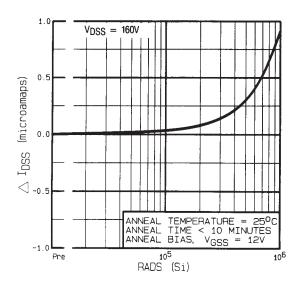


Fig 4. Typical Response of Drain to Source Breakdown Vs. Total Dose Exposure

Post-Irradiation IRHMJ7250



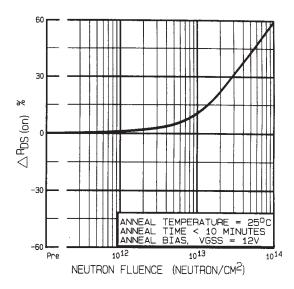


Fig 5. Typical Zero Gate Voltage Drain Current Vs. Total Dose Exposure

Fig 6. Typical On-State Resistance Vs. Neutron Fluence Level

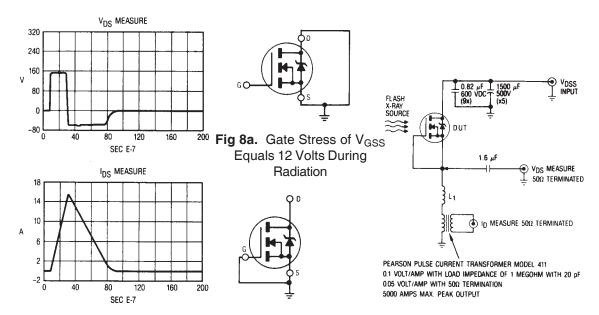


Fig 7. Typical Transient Response of Rad Hard HEXFET During 1x10¹² Rad (Si)/Sec Exposure

Fig 8b. V_{DSS} Stress Equals 80% of B_{VDSS} During Radiation

Fig 9. High Dose Rate (Gamma Dot) Test Circuit

Note: Bias Conditions during radiation: Vgs = 12 Vdc, Vps = 0 Vdc

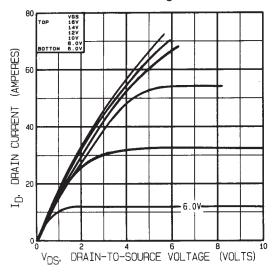
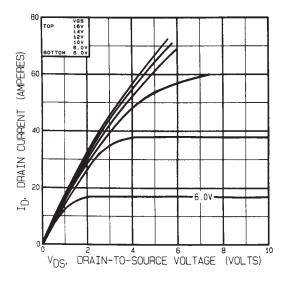


Fig 10. Typical Output Characteristics Pre-Irradiation

Fig 11. Typical Output Characteristics Post-Irradiation 100K Rads (Si)





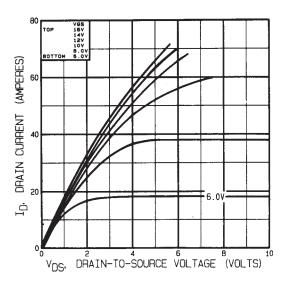
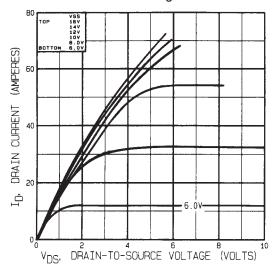


Fig 13. Typical Output Characteristics Post-Irradiation 1 Mega Rads(Si)

Note: Bias Conditions during radiation: Vgs = 0 Vdc, Vps = 160 Vdc



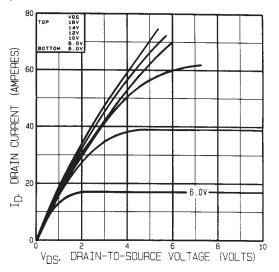
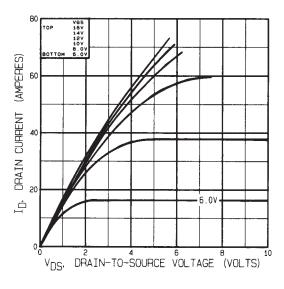


Fig 14. Typical Output Characteristics
Pre-Irradiation

Fig 15. Typical Output Characteristics Post-Irradiation 100K Rads (Si)





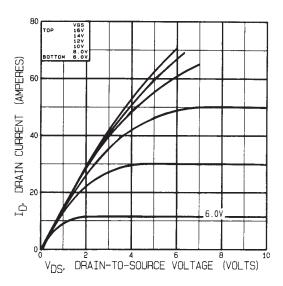
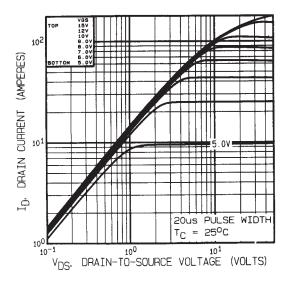


Fig 17. Typical Output Characteristics Post-Irradiation 1 Mega Rads(Si)



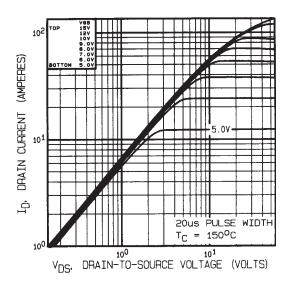
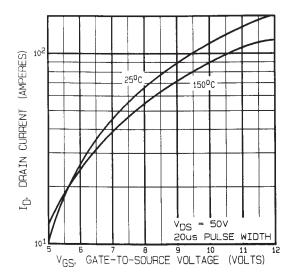
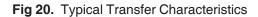


Fig 18. Typical Output Characteristics

Fig 19. Typical Output Characteristics





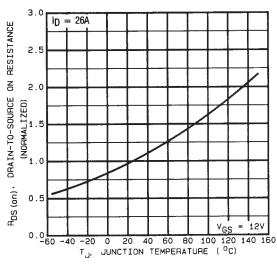
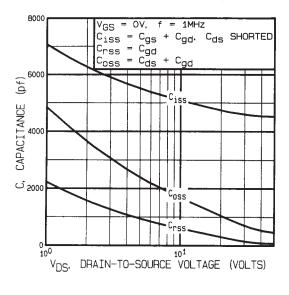


Fig 21. Normalized On-Resistance Vs. Temperature

Pre-Irradiation IRHMJ7250



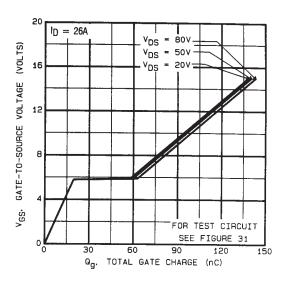


Fig 22. Typical CapacitanceVs. Drain-to-Source Voltage

Fig 23. Typical Gate Charge Vs. Gate-to-Source Voltage

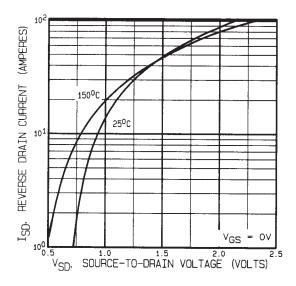


Fig 24. Typical Source-Drain Diode Forward Voltage

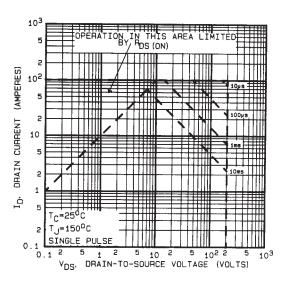


Fig 25. Maximum Safe Operating Area

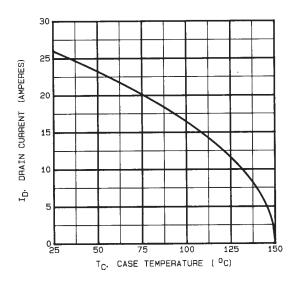


Fig 26. Maximum Drain Current Vs. Case Temperature

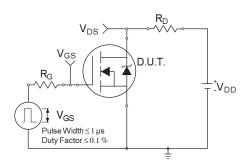


Fig 26a. Switching Time Test Circuit

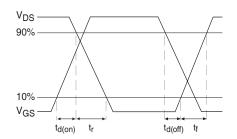


Fig 26b. Switching Time Waveforms

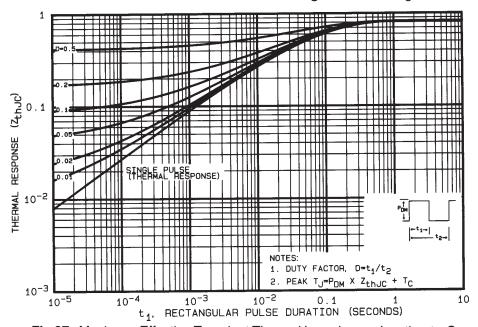


Fig 27. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Pre-Irradiation IRHMJ7250

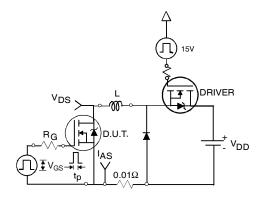


Fig 28a. Unclamped Inductive Test Circuit

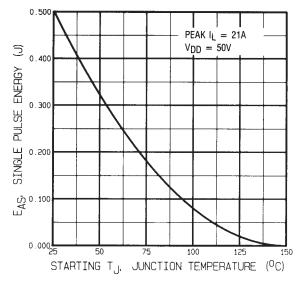


Fig 28c. Maximum Avalanche Energy Vs. Drain Current

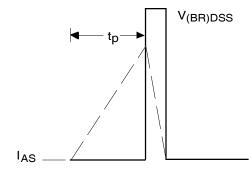


Fig 28b. Unclamped Inductive Waveforms

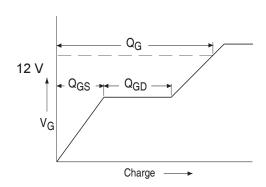


Fig 29a. Basic Gate Charge Waveform

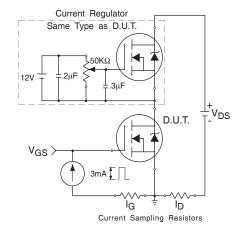


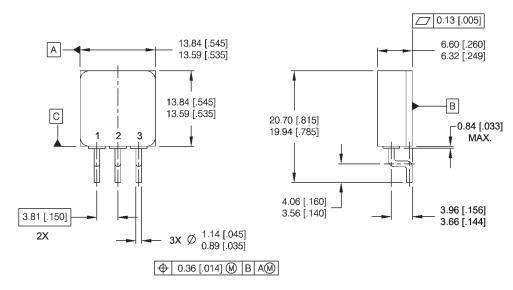
Fig 29b. Gate Charge Test Circuit

Foot Notes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- $^{\circ}$ VDD = 25V, starting TJ = 25°C, L= 1.5mH Peak IL = 26A, VGS = 12V
- $\label{eq:ISD} \begin{tabular}{ll} \begin{$

- ④ Pulse width ≤ 300 μ s; Duty Cycle ≤ 2%
- Total Dose Irradiation with VGS Bias.
 12 volt VGS applied and VDS = 0 during irradiation per MIL-STD-750, method 1019, condition A.
- ® Total Dose Irradiation with Vps Bias. 160 volt Vps applied and Vgs = 0 during irradiation per MIL-STD-750, method 1019, condition A.

Case Outline and Dimensions — TO-254AA Tabless



NOTES:

- 1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
- 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
- 3. CONTROLLING DIMENSION: INCH.
- 4. THIS OUTLINE IS A MODIFIED TO-254AA JEDEC OUTLINE.

PIN ASSIGNMENTS

- 1 = DRAIN
- 2 = SOURCE
- 3 = GATE

CAUTION

BERYLLIA WARNING PER MIL-PRF-19500

Packages containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.



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