ALPHA & OMEGA SEMICONDUCTOR

AO4702

N-Channel Enhancement Mode Field Effect Transistor with Schottky Diode

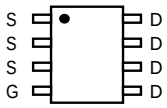
General Description

The AO4702 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. A Schottky Diode is packaged in parallel to improve device performance in synchronous recitification applications, or H-bridge configurations. *Standard Product AO4702 is Pb-free (meets ROHS & Sony 259 specifications). AO4702L is a Green Product ordering option. AO4702and AO4702L are electrically identical.*

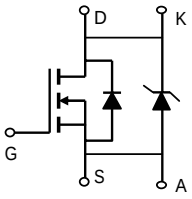
Features

V_{DS} (V) = 30V
I_D = 11A (V_{GS} = 10V)
$R_{DS(ON)}$ < 16mΩ (V_{GS} = 10V)
$R_{DS(ON)}$ < 25mΩ (V_{GS} = 4.5V)

SCHOTTKY
VDS (V) = 30V, IF = 3A, VF<0.5V@1A



SOIC-8



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	MOSFET	Schottky	Units
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	±20		V
Continuous Drain Current [A]	T_A=25°C	I_D	11		A
	T_A=70°C		9.3		
Pulsed Drain Current [B]		I_{DM}	50		
Schottky reverse voltage		V_{KA}		30	V
Continuous Forward Current [A]	T_A=25°C	I_F		4.4	A
	T_A=70°C			3.2	
Pulsed Diode Forward Current [B]		I_{FM}		30	
Power Dissipation	T_A=25°C	P_D	3	3	W
	T_A=70°C		2	2	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	-55 to 150	°C

Thermal Characteristics: MOSFET					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	31	40	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		59	75	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	16	24	°C/W

Thermal Characteristics: Schottky					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	36	40	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		67	75	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	25	30	°C/W

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in ^{2} FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.
B: Repetitive rating, pulse width limited by junction temperature.
C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
D. The static characteristics in Figures 1 to 6 are obtained using 80 μs pulses, duty cycle 0.5% max.
E. These tests are performed with the device mounted on 1 in ^{2} FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.
F. The Schottky appears in parallel with the MOSFET body diode, even though it is a separate chip. Therefore, we provide the net forward drop, capacitance and recovery characteristics of the MOSFET and Schottky. However, the thermal resistance is specified for each chip separately.
Rev 5 : Aug 2005

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current (Set by Schottky leakage)	V_R=30V		0.007	0.05	mA
		V_R=30V, T_J=125°C		3.2	10	
		V_R=30V, T_J=150°C		12	20	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1	1.8	3	V
$I_{D(ON)}$	On state drain current	V_{GS}=4.5V, V_{DS}=5V	40			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=11A		13.4	16	mΩ
		T_J=125°C		16.8	21	
		V_{GS}=4.5V, I_D=8A		20	25	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=11A		25		S
V_{SD}	Diode + Schottky Forward Voltage	I_S=1A,V_{GS}=0V		0.45	0.5	V
I_S	Maximum Body-Diode + Schottky Continuous Current				5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		1040	1250	pF
C_{oss}	Output Capacitance (FET+Schottky)			212		pF
C_{rss}	Reverse Transfer Capacitance			121		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		0.7	0.85	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=11A		19.8	24	nC
Q_g(4.5V)	Total Gate Charge			9.8	12	nC
Q_{gs}	Gate Source Charge			2.5		nC
Q_{gd}	Gate Drain Charge			3.5		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=1.35Ω, R_{GEN}=3Ω		4.5	7	ns
t_r	Turn-On Rise Time			3.9	7	ns
$t_{D(off)}$	Turn-Off DelayTime			17.4	30	ns
t_f	Turn-Off Fall Time			3.2	5.7	ns
t_{rr}	Body Diode + Schottky Reverse Recovery Time	I_F=11A, dI/dt=100A/µs		19	23	ns
Q_{rr}	Body Diode + Schottky Reverse Recovery Charge	I_F=11A, dI/dt=100A/µs		9	11	nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in ^{2} FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6 are obtained using 80 µs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in ^{2} FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

F. The Schottky appears in parallel with the MOSFET body diode, even though it is a separate chip. Therefore, we provide the net forward drop, capacitance and recovery characteristics of the MOSFET and Schottky. However, the thermal resistance is specified for each chip separately.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

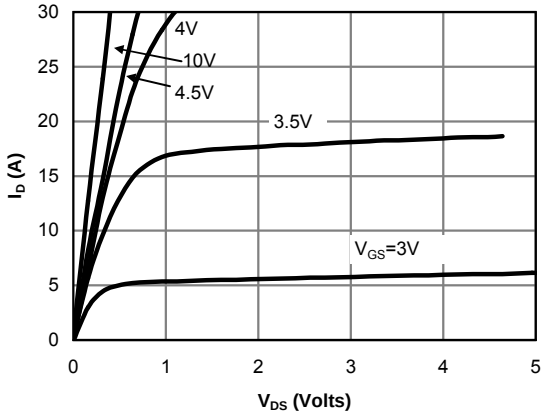

Fig 1: On-Region Characteristics

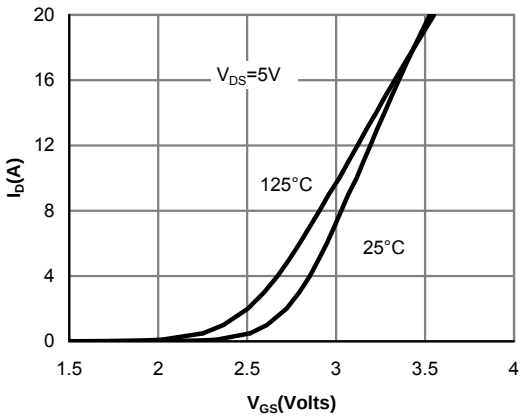

Figure 2: Transfer Characteristics

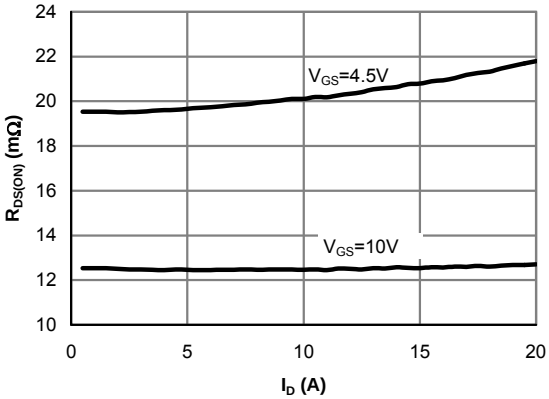

Figure 3: On-Resistance vs. Drain Current and Gate Voltage

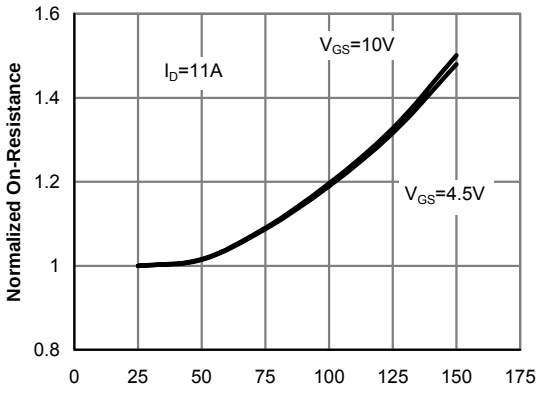

Figure 4: On-Resistance vs. Junction Temperature

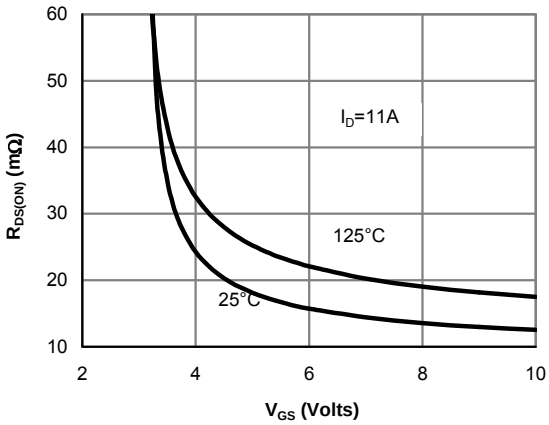

Figure 5: On-Resistance vs. Gate-Source Voltage

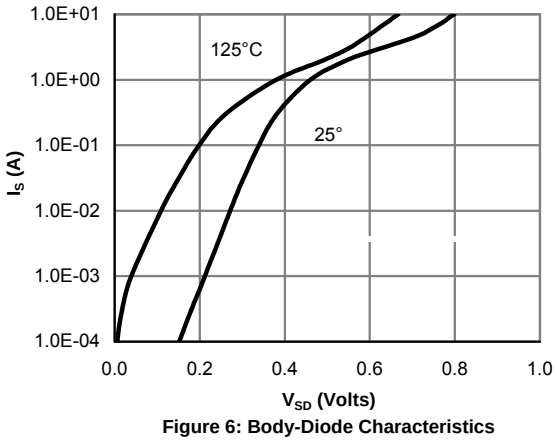

Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

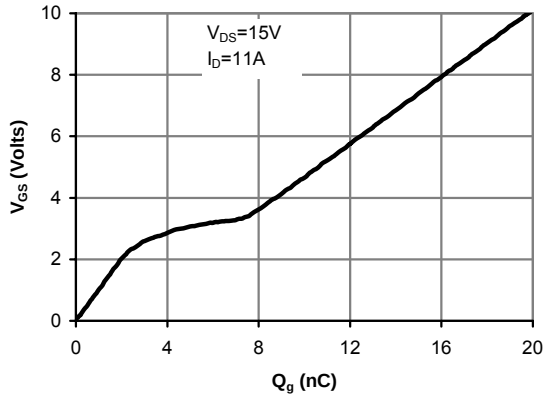

Figure 7: Gate-Charge Characteristics

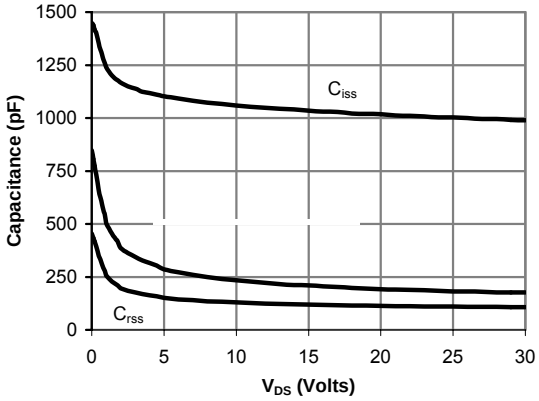

Figure 8: Capacitance Characteristics

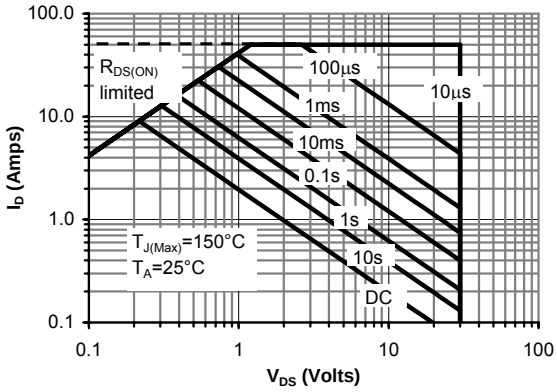

Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

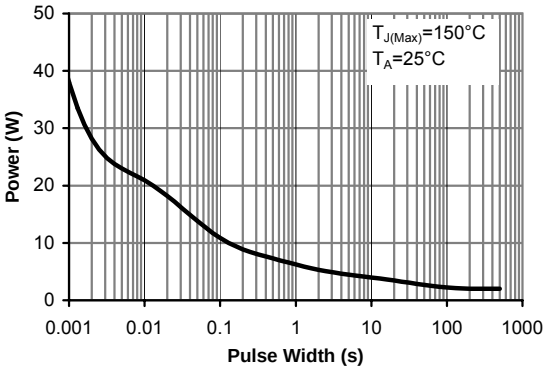

Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

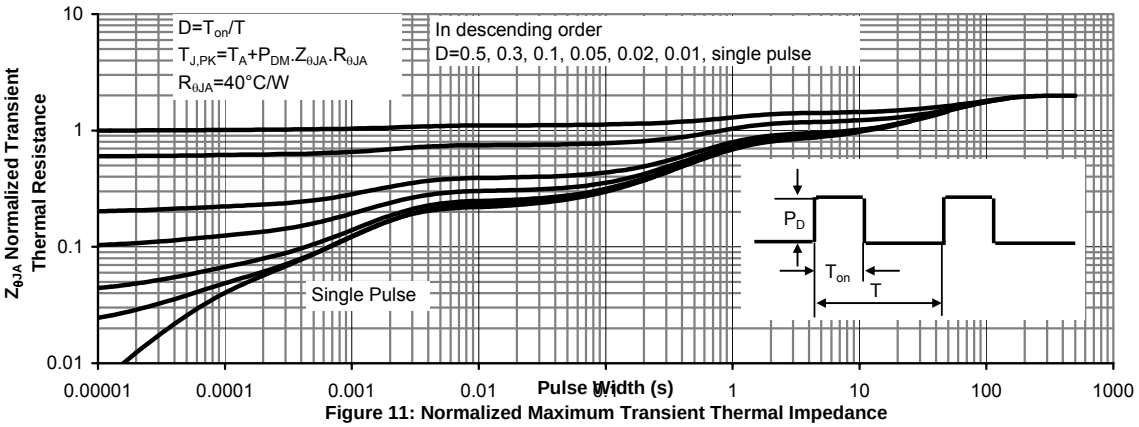

Figure 11: Normalized Maximum Transient Thermal Impedance