FAIRCHILD SEMICONDUCTOR®

July 2001
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NC7NZU04
TinyLogic® UHS Unbuffered Inverter

General Description

The NC7NZU04 is a triple unbuffered inverter from Fairchild's Ultra High Speed Series of TinyLogic®. The special purpose unbuffered circuit design is primarily intended for crystal oscillator or analog applications. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.65V to 5.5V V_{CC} range.

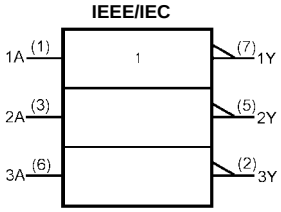
Features

- Space saving US8 surface mount package
- MicroPak™ leadless package
- Unbuffered for crystal oscillator and analog applications
- Balanced Output Drive; ± 8 mA at 4.5V V_{CC}
- Broad V_{CC} Operating Range: 1.65V to 5.5V
- Low Quiescent Power;
  I_{CC} < 1 µA, V_{CC} = 5.5V, T_A = 25°C

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7NZU04K8X	MAB08A	7NZU4	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3k Units on Tape and Reel
NC7NZU04L8X (Preliminary)	MAC08A	U6	8-Lead MicroPak, 1.6 mm Wide	5k Units on Tape and Reel

Logic Symbol



Pin Descriptions

Pin Names	Description
A	Input
Y	Output

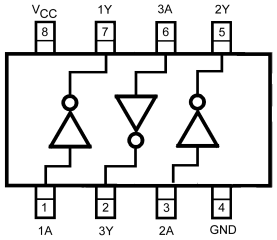
Function Table

$Y = \overline{A}$

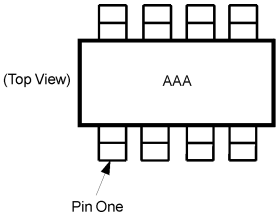
Input	Output
A	**Y**
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

Connection Diagrams

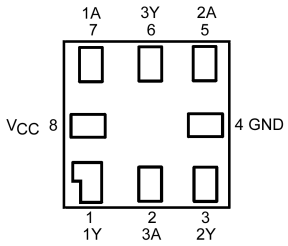


(Top View)



AAA represents Product Code Top Mark - see ordering code
Note: Orientation of Top Mark determines Pin One location. Read the Top Product Code Mark left to right, Pin One is the lower left pin (see diagram).

Pad Assignment for MicroPak



(Top Thru View)

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7V
DC Input Voltage (V_{IN})	−0.5V to +7V
DC Output Voltage (V_{OUT})	−0.5V to +7V
DC Input Diode Current (I_{IK})	
@ V_{IN} < −0.5V	−50 mA
@ V_{IN} > V_{CC} + 0.5V	+20 mA
DC Output Diode Current (I_{OK})	
@ V_{OUT} < −0.5V	−50 mA
@ V_{OUT} > 0.5V, V_{CC} = GND	+50 mA
DC Output Current (I_{OUT})	±50 mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	±100 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature under Bias (T_J)	150°C
Junction Lead Temperature (T_L);	
(Soldering, 10 seconds)	260°C
Power Dissipation (P_D) @ +85°C	250 mW

Recommended Operating Conditions (Note 2)

Supply Voltage Operating (V_{CC})	1.65V to 5.5V
Supply Voltage Data Retention (V_{CC})	1.5V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Thermal Resistance (θ_{JA})	250°C/W

Note 1: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = +25°C			T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level Input Voltage	1.65 to 2.7	0.85 V_{CC}			0.85 V_{CC}		V		
		3.0 to 5.5	0.8 V_{CC}			0.8 V_{CC}				
V_{IL}	LOW Level Input Voltage	1.65 to 2.7			0.15 V_{CC}		0.15 V_{CC}	V		
		3.0 to 5.5			0.2 V_{CC}		0.2 V_{CC}			
V_{OH}	HIGH Level Output Voltage	1.65	1.55	1.65		1.55			V_{IN} = V_{IL}	I_{OH} = −100 µA
		2.3	2.1	2.3		2.1				
		3.0	2.7	3.0		2.7				
		4.5	4.0	4.4		4.0				
		1.65	1.29	1.52		1.29		V	V_{IN} = GND	I_{OH} = −2 mA
		2.3	1.9	2.14		1.9				I_{OH} = −2 mA
		3.0	2.4	2.75		2.4				I_{OH} = −4 mA
		3.0	2.3	2.61		2.3				I_{OH} = −6 mA
		4.5	3.8	4.13		3.8				I_{OH} = −8 mA
V_{OL}	LOW Level Output Voltage	1.65		0.0	0.2		0.2		V_{IN} = V_{IH}	I_{OL} = 100 µA
		2.3		0.0	0.2		0.2			
		3.0		0.0	0.3		0.3			
		4.5		0.0	0.5		0.5			
		1.65		0.08	0.24		0.24	V	V_{IN} = V_{CC}	I_{OL} = 2 mA
		2.3		0.10	0.3		0.3			I_{OL} = 2 mA
		3.0		0.17	0.4		0.4			I_{OL} = 4 mA
		3.0		0.25	0.55		0.55			I_{OL} = 6 mA
		4.5		0.26	0.55		0.55			I_{OL} = 8 mA
I_{IN}	Input Leakage Current	0 to 5.5			±0.1		±1.0	µA	V_{IN} = 5.5V, GND	
I_{CC}	Quiescent Supply Current	1.65 to 5.5			1		10	µA	V_{IN} = 5.5V, GND	
I_{CCPEAK}	Peak Supply Current in	1.8		1				mA	V_{OUT} = Open	
	Analog Operation	2.5		2					V_{IN} = Adjust for	
		3.3		5					Peak I_{CC} Current	
		5.0		15						

AC Electrical Characteristics

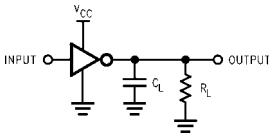
Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions	Figure Number
			Min	Typ	Max	Min	Max			
t_{PLH}, t_{PHL}	Propagation Delay	1.8 ± 0.05	1.0		8.5	1.0	9.0	ns	C_L = 15 pF, R_L = 1 MΩ	Figures 1, 3
		2.5 ± 0.2	0.8		6.2	0.8	6.5			
		3.3 ± 0.3	0.5		4.5	0.5	4.8			
		5.0 ± 0.5	0.5		3.9	0.5	4.1			
t_{PLH}, t_{PHL}	Propagation Delay	3.3 ± 0.3	1.0		6.0	1.0	6.5	ns	C_L = 50 pF, R_L = 500Ω	Figures 1, 3
		5.0 ± 0.5	0.8		5.0	0.8	5.5			
C_{IN}	Input Capacitance	0		2.5				pF		
C_{PD}	Power Dissipation Capacitance	3.3		9				pF	(Note 3)	Figure 2
		5.0		11						

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC}\text{static})$.

Dynamic Switching Characteristics

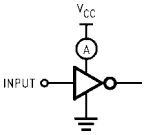
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Typical	Unit
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	C_L = 50pF, V_{IH} = 5.0V, V_{IL} = 0V	5.0	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	C_L = 50pF, V_{IH} = 5.0V, V_{IL} = 0V	5.0	–0.8	V

AC Loading and Waveforms



C_L includes load and stray capacitance
Input PRR = 1.0 MHz; t_W = 500 ns

FIGURE 1. AC Test Circuit



Application Note: When operating the NC7NZU04's unbuffered output stage in its linear range, as in oscillator applications, care must be taken to observe maximum power rating for the device and package. The high drive nature of the design of the output stage will result in substantial simultaneous conduction currents when the stage is in the linear region. See the I_{CCPEAK} specification in the DC Electrical Characteristics table.

Input = AC Waveform; $t_r = t_f$ = 1.8 ns;
PRR = variable; Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit

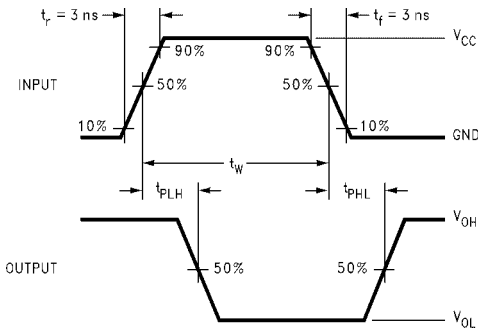


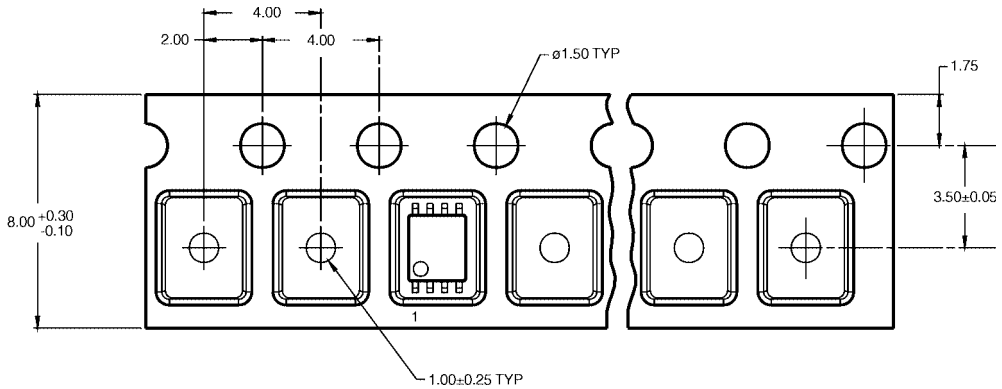
FIGURE 3. AC Waveforms

Tape and Reel Specification

TAPE FORMAT for US8

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
K8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

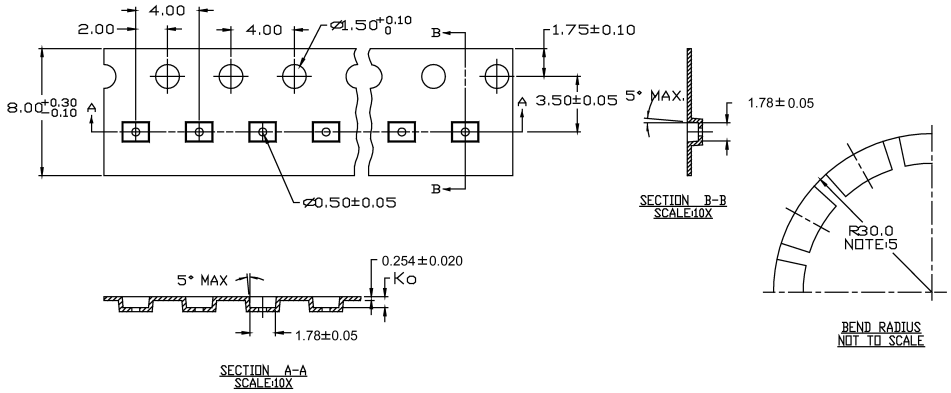
TAPE DIMENSIONS inches (millimeters)



TAPE FORMAT for MicroPak

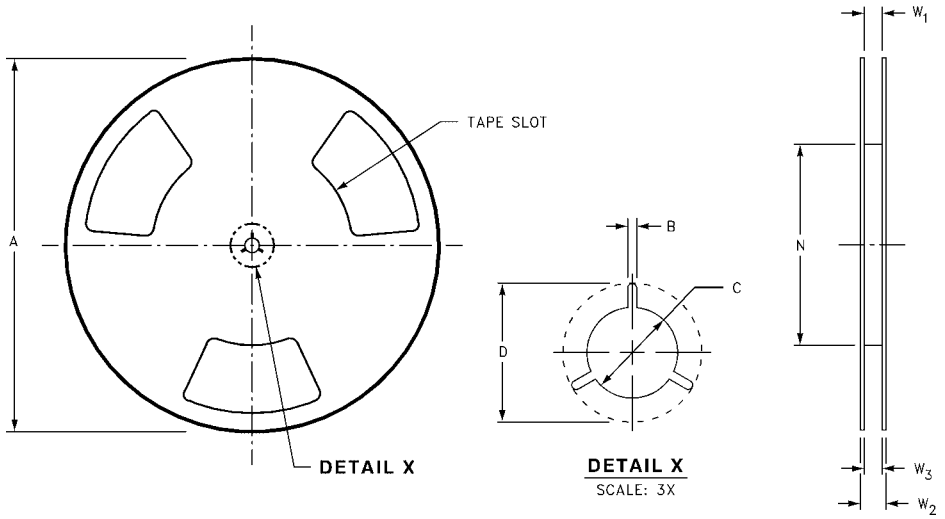
Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)



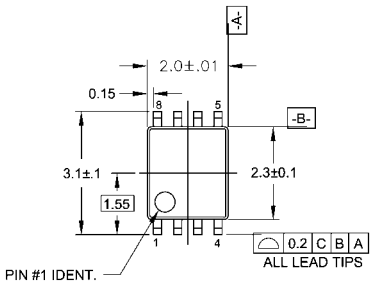
Tape and Reel Specification (Continued)

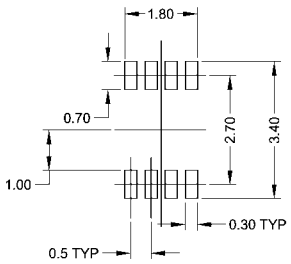
REEL DIMENSIONS inches (millimeters)



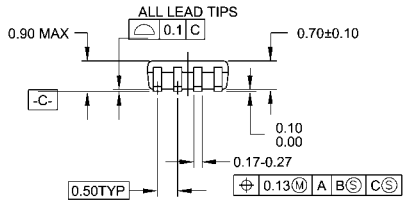
Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/–0.000 (8.40 + 1.5/–0.00)	0.567 (14.40)	W1 + 0.078/–0.039 (W1 + 2.00/–1.00)

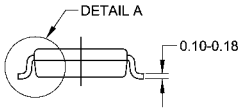
Physical Dimensions inches (millimeters) unless otherwise noted

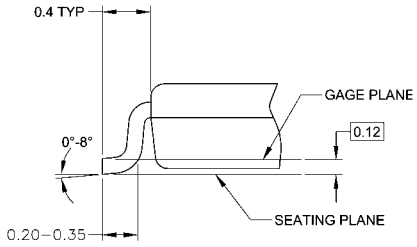




LAND PATTERN RECOMMENDATION







DETAIL A

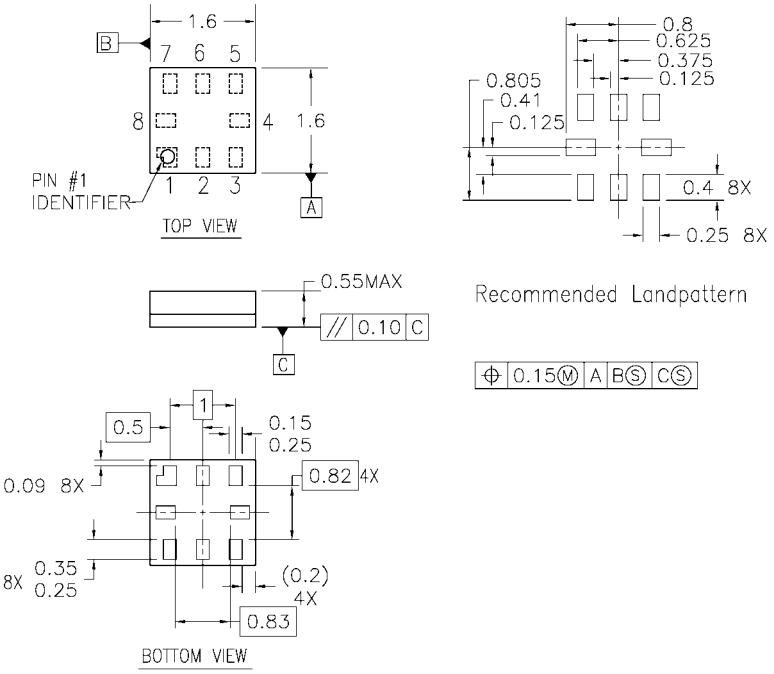
NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-187
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MAB08AREVC

8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide
Package Number MAB08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Notes:

1. PACKAGE REGISTRATION WITH JEDEC IS ANTICIPATED
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y.14M–1994

MAC08AREVB

8-Lead MicroPak, 1.6 mm Wide
Package Number MAC08A
(Preliminary)

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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