

Sitronix

ST7625

65K Color Dot Matrix LCD Controller/Driver

1. INTRODUCTION

The ST7625 is a driver & controller LSI for 65K color graphic dot-matrix liquid crystal display systems. It generates 306 Segment and 96 Common driver circuits. This chip is connected directly to a microprocessor, accepts Serial Peripheral Interface (SPI) or 8-bit/16-bit parallel display data and stores in an on-chip display data RAM. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

Driver Output Circuits

- ◆ 306 Segment Outputs / 96 Common Outputs

Applicable Duty Ratios

- ◆ Various Partial Display
- ◆ Partial Window Moving & Data Scrolling

Gray-Scale Display

- ◆ 4FRC & 31 PWM function circuit to display
- ◆ 64 gray-scale display
- ◆ Support 8 color mode (Idle mode)

On-chip Display Data RAM

- ◆ Capacity: 102 x 96 x 16 =156,672 bits

Color support by Interface

- ◆ 256 color mode, (RGB)=(332) mode
- ◆ 4K color mode, (RGB)=(444) mode
- ◆ 65K color mode, (RGB)=(565) mode
- ◆ Truncated 262K color mode, (RGB)=(666) mode
- ◆ Truncated 16M color mode, (RGB)=(888) mode

Microprocessor Interface

- ◆ 8/16-bit parallel bi-directional interface with 6800-series or 8080-series
- ◆ 4-line serial interface

- ◆ 3-line (9-bits) serial interface

On-chip Low Power Analog Circuit

- ◆ On-chip Oscillator Circuit
- ◆ On-chip Voltage Converter (x2, x3, x4, x5, x6, x7, X8) with internal booster capacitors.
- ◆ Extremely Few Outsider Components. (Required outsider components: Three Capacitors)
- ◆ On-chip Voltage Regulator
- ◆ On-chip Electronic Contrast Control Function
- ◆ Voltage Follower (LCD bias: 1/5~1/12)

Operating Voltage Range

- ◆ Supply Digital Voltage (VDD, VDD1): 1.65 to 3.0V
- ◆ Supply Analog Voltage (VDD2, VDD3, VDD4, VDD5): 2.4 to 3.3V
- ◆ LCD Driving Voltage (VOP = V0 - VSS): Max to 18V

LCD Driving Voltage (OTP)

- ◆ Contrast Adjustment Value is stored in the Built-In OTP-ROM for better display quality.

LCD Driving setting suggestion

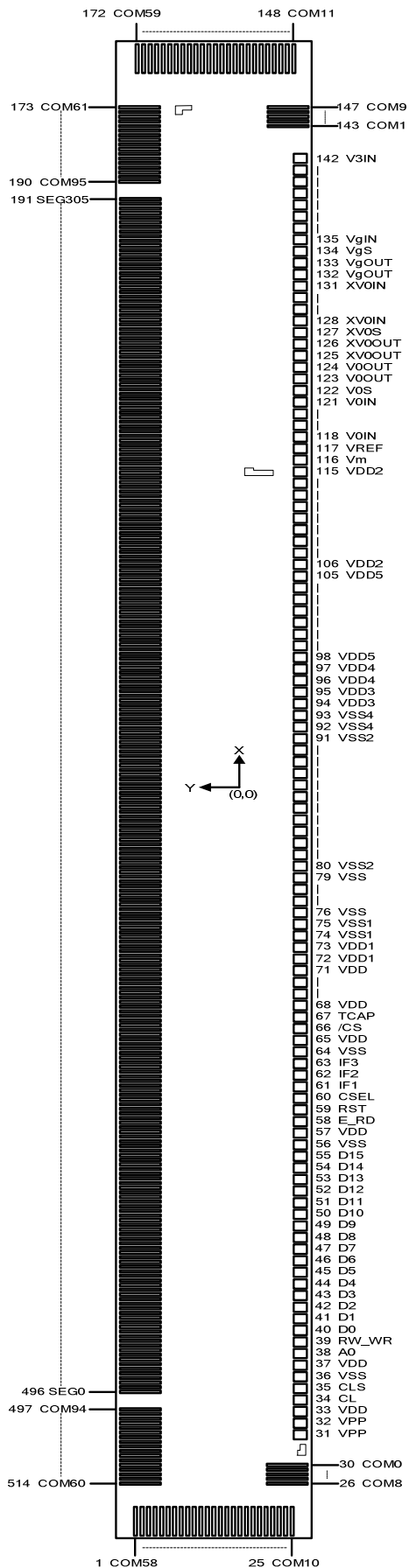
- ◆ VOP = 11V, BIAS=1/9. (VDD=2.8V)

Package Type

- ◆ Application for COG

ST7625-G3	Chip thickness=400um	
ST7625-G4	Chip thickness=300um	
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3. ST7625 Pad Arrangement (COG)



Chip Size :

9,930 um x 820 um

Bump Pitch :

PAD NO. 1 ~ 30, 143 ~ 514 : 27 um (COM/SEG)

PAD NO. 31 ~ 142 : 80 um (I/O)

Bump Size :

PAD NO. 1 ~ 25, 148 ~ 172 :

120.5 um(x) ~ 15 um(y) (COM)

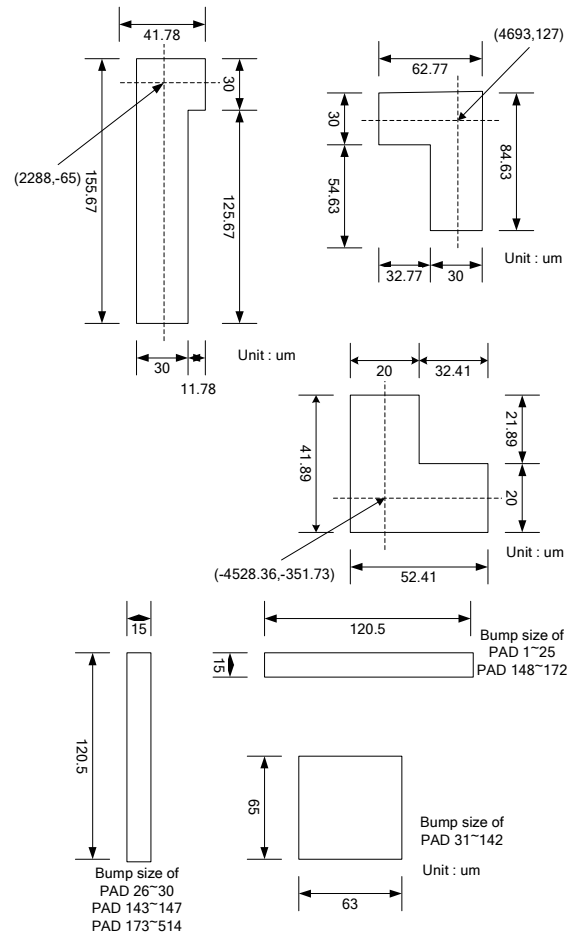
PAD NO. 26 ~ 30, 143 ~ 147, 173 ~ 514 :

15 um(x) ~ 120.5 um(y) (COM/SEG)

PAD NO. 31 ~ 142 :

65 um(x) ~ 63 um(y) (I/O)

Bump Height : 15 um



4. Pad Center Coordinates

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
001	COM[58]	-4861.75	320.50	034	CL	-4184.71	-329.50
002	COM[56]	-4861.75	293.50	035	CLS	-4104.71	-329.50
003	COM[54]	-4861.75	266.50	036	VSS	-4024.71	-329.50
004	COM[52]	-4861.75	239.50	037	VDD	-3944.71	-329.50
005	COM[50]	-4861.75	212.50	038	A0	-3864.71	-329.50
006	COM[48]	-4861.75	185.50	039	RW_WR	-3784.71	-329.50
007	COM[46]	-4861.75	158.50	040	D0	-3704.71	-329.50
008	COM[44]	-4861.75	131.50	041	D1	-3624.71	-329.50
009	COM[42]	-4861.75	104.50	042	D2	-3544.71	-329.50
010	COM[40]	-4861.75	77.50	043	D3	-3464.71	-329.50
011	COM[38]	-4861.75	50.50	044	D4	-3384.71	-329.50
012	COM[36]	-4861.75	23.50	045	D5	-3304.71	-329.50
013	COM[34]	-4861.75	-3.50	046	D6	-3224.71	-329.50
014	COM[32]	-4861.75	-30.50	047	D7	-3144.71	-329.50
015	COM[30]	-4861.75	-57.50	048	D8	-3064.71	-329.50
016	COM[28]	-4861.75	-84.50	049	D9	-2984.71	-329.50
017	COM[26]	-4861.75	-111.50	050	D10	-2904.71	-329.50
018	COM[24]	-4861.75	-138.50	051	D11	-2824.71	-329.50
019	COM[22]	-4861.75	-165.50	052	D12	-2744.71	-329.50
020	COM[20]	-4861.75	-192.50	053	D13	-2664.71	-329.50
021	COM[18]	-4861.75	-219.50	054	D14	-2584.71	-329.50
022	COM[16]	-4861.75	-246.50	055	D15	-2504.71	-329.50
023	COM[14]	-4861.75	-273.50	056	VSS	-2424.71	-329.50
024	COM[12]	-4861.75	-300.50	057	VDD	-2344.71	-329.50
025	COM[10]	-4861.75	-327.50	058	E_RD	-2264.71	-329.50
026	COM[8]	-4684.02	-306.75	059	/RST	-2184.71	-329.50
027	COM[6]	-4657.02	-306.75	060	CSEL	-2104.71	-329.50
028	COM[4]	-4630.02	-306.75	061	IF1	-2024.71	-329.50
029	COM[2]	-4603.02	-306.75	062	IF2	-1944.71	-329.50
030	COM[0]	-4576.02	-306.75	063	IF3	-1864.71	-329.50
031	VPP	-4424.71	-329.50	064	VSS	-1784.71	-329.50
032	VPP	-4344.71	-329.50	065	VDD	-1704.71	-329.50
033	VDD	-4264.71	-329.50	066	/CS	-1624.71	-329.50

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
067	TCAP	-1544.71	-329.50	102	VDD5	1255.29	-329.50
068	VDD	-1464.71	-329.50	103	VDD5	1335.29	-329.50
069	VDD	-1384.71	-329.50	104	VDD5	1415.29	-329.50
070	VDD	-1304.71	-329.50	105	VDD5	1495.29	-329.50
071	VDD	-1224.71	-329.50	106	VDD2	1575.29	-329.50
072	VDD1	-1144.71	-329.50	107	VDD2	1655.29	-329.50
073	VDD1	-1064.71	-329.50	108	VDD2	1735.29	-329.50
074	VSS1	-984.71	-329.50	109	VDD2	1815.29	-329.50
075	VSS1	-904.71	-329.50	110	VDD2	1895.29	-329.50
076	VSS	-824.71	-329.50	111	VDD2	1975.29	-329.50
077	VSS	-744.71	-329.50	112	VDD2	2055.29	-329.50
078	VSS	-664.71	-329.50	113	VDD2	2135.29	-329.50
079	VSS	-584.71	-329.50	114	VDD2	2215.29	-329.50
080	VSS2	-504.71	-329.50	115	VDD2	2295.29	-329.50
081	VSS2	-424.71	-329.50	116	Vm	2375.29	-329.50
082	VSS2	-344.71	-329.50	117	VREF	2455.29	-329.50
083	VSS2	-264.71	-329.50	118	V0IN	2535.29	-329.50
084	VSS2	-184.71	-329.50	119	V0IN	2615.29	-329.50
085	VSS2	-104.71	-329.50	120	V0IN	2695.29	-329.50
086	VSS2	-24.71	-329.50	121	V0IN	2775.29	-329.50
087	VSS2	55.29	-329.50	122	V0S	2855.29	-329.50
088	VSS2	135.29	-329.50	123	V0OUT	2935.29	-329.50
089	VSS2	215.29	-329.50	124	V0OUT	3015.29	-329.50
090	VSS2	295.29	-329.50	125	XV0OUT	3095.29	-329.50
091	VSS2	375.29	-329.50	126	XV0OUT	3175.29	-329.50
092	VSS4	455.29	-329.50	127	XV0S	3255.29	-329.50
093	VSS4	535.29	-329.50	128	XV0IN	3335.29	-329.50
094	VDD3	615.29	-329.50	129	XV0IN	3415.29	-329.50
095	VDD3	695.29	-329.50	130	XV0IN	3495.29	-329.50
096	VDD4	775.29	-329.50	131	XV0IN	3575.29	-329.50
097	VDD4	855.29	-329.50	132	VgOUT	3655.29	-329.50
098	VDD5	935.29	-329.50	133	VgOUT	3735.29	-329.50
099	VDD5	1015.29	-329.50	134	VgS	3815.29	-329.50
100	VDD5	1095.29	-329.50	135	VgIN	3895.29	-329.50
101	VDD5	1175.29	-329.50	136	VgIN	3975.29	-329.50

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
137	VgIN	4055.29	-329.50	172	COM[59]	4861.75	320.50
138	VgIN	4135.29	-329.50	173	COM[61]	4684.02	306.75
139	VgIN	4215.29	-329.50	174	COM[63]	4657.02	306.75
140	VgIN	4295.29	-329.50	175	COM[65]	4630.02	306.75
141	VgIN	4375.29	-329.50	176	COM[67]	4603.02	306.75
142	VgIN	4455.29	-329.50	177	COM[69]	4576.02	306.75
143	COM[1]	4576.02	-306.75	178	COM[71]	4549.02	306.75
144	COM[3]	4603.02	-306.75	179	COM[73]	4522.02	306.75
145	COM[5]	4630.02	-306.75	180	COM[75]	4495.02	306.75
146	COM[7]	4657.02	-306.75	181	COM[77]	4468.02	306.75
147	COM[9]	4684.02	-306.75	182	COM[79]	4441.02	306.75
148	COM[11]	4861.75	-327.50	183	COM[81]	4414.02	306.75
149	COM[13]	4861.75	-300.50	184	COM[83]	4387.02	306.75
150	COM[15]	4861.75	-273.50	185	COM[85]	4360.02	306.75
151	COM[17]	4861.75	-246.50	186	COM[87]	4333.02	306.75
152	COM[19]	4861.75	-219.50	187	COM[89]	4306.02	306.75
153	COM[21]	4861.75	-192.50	188	COM[91]	4279.02	306.75
154	COM[23]	4861.75	-165.50	189	COM[93]	4252.02	306.75
155	COM[25]	4861.75	-138.50	190	COM[95]	4225.02	306.75
156	COM[27]	4861.75	-111.50	191	SEG[305]	4117.50	306.75
157	COM[29]	4861.75	-84.50	192	SEG[304]	4090.50	306.75
158	COM[31]	4861.75	-57.50	193	SEG[303]	4063.50	306.75
159	COM[33]	4861.75	-30.50	194	SEG[302]	4036.50	306.75
160	COM[35]	4861.75	-3.50	195	SEG[301]	4009.50	306.75
161	COM[37]	4861.75	23.50	196	SEG[300]	3982.50	306.75
162	COM[39]	4861.75	50.50	197	SEG[299]	3955.50	306.75
163	COM[41]	4861.75	77.50	198	SEG[298]	3928.50	306.75
164	COM[43]	4861.75	104.50	199	SEG[297]	3901.50	306.75
165	COM[45]	4861.75	131.50	200	SEG[296]	3874.50	306.75
166	COM[47]	4861.75	158.50	201	SEG[295]	3847.50	306.75
167	COM[49]	4861.75	185.50	202	SEG[294]	3820.50	306.75
168	COM[51]	4861.75	212.50	203	SEG[293]	3793.50	306.75
169	COM[53]	4861.75	239.50	204	SEG[292]	3766.50	306.75
170	COM[55]	4861.75	266.50	205	SEG[291]	3739.50	306.75
171	COM[57]	4861.75	293.50	206	SEG[290]	3712.50	306.75

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PAD No.	PIN Name	X	Y
207	SEG[289]	3685.50	306.75
208	SEG[288]	3658.50	306.75
209	SEG[287]	3631.50	306.75
210	SEG[286]	3604.50	306.75
211	SEG[285]	3577.50	306.75
212	SEG[284]	3550.50	306.75
213	SEG[283]	3523.50	306.75
214	SEG[282]	3496.50	306.75
215	SEG[281]	3469.50	306.75
216	SEG[280]	3442.50	306.75
217	SEG[279]	3415.50	306.75
218	SEG[278]	3388.50	306.75
219	SEG[277]	3361.50	306.75
220	SEG[276]	3334.50	306.75
221	SEG[275]	3307.50	306.75
222	SEG[274]	3280.50	306.75
223	SEG[273]	3253.50	306.75
224	SEG[272]	3226.50	306.75
225	SEG[271]	3199.50	306.75
226	SEG[270]	3172.50	306.75
227	SEG[269]	3145.50	306.75
228	SEG[268]	3118.50	306.75
229	SEG[267]	3091.50	306.75
230	SEG[266]	3064.50	306.75
231	SEG[265]	3037.50	306.75
232	SEG[264]	3010.50	306.75
233	SEG[263]	2983.50	306.75
234	SEG[262]	2956.50	306.75
235	SEG[261]	2929.50	306.75
236	SEG[260]	2902.50	306.75
237	SEG[259]	2875.50	306.75
238	SEG[258]	2848.50	306.75
239	SEG[257]	2821.50	306.75
240	SEG[256]	2794.50	306.75
241	SEG[255]	2767.50	306.75

PAD No.	PIN Name	X	Y
242	SEG[254]	2740.50	306.75
243	SEG[253]	2713.50	306.75
244	SEG[252]	2686.50	306.75
245	SEG[251]	2659.50	306.75
246	SEG[250]	2632.50	306.75
247	SEG[249]	2605.50	306.75
248	SEG[248]	2578.50	306.75
249	SEG[247]	2551.50	306.75
250	SEG[246]	2524.50	306.75
251	SEG[245]	2497.50	306.75
252	SEG[244]	2470.50	306.75
253	SEG[243]	2443.50	306.75
254	SEG[242]	2416.50	306.75
255	SEG[241]	2389.50	306.75
256	SEG[240]	2362.50	306.75
257	SEG[239]	2335.50	306.75
258	SEG[238]	2308.50	306.75
259	SEG[237]	2281.50	306.75
260	SEG[236]	2254.50	306.75
261	SEG[235]	2227.50	306.75
262	SEG[234]	2200.50	306.75
263	SEG[233]	2173.50	306.75
264	SEG[232]	2146.50	306.75
265	SEG[231]	2119.50	306.75
266	SEG[230]	2092.50	306.75
267	SEG[229]	2065.50	306.75
268	SEG[228]	2038.50	306.75
269	SEG[227]	2011.50	306.75
270	SEG[226]	1984.50	306.75
271	SEG[225]	1957.50	306.75
272	SEG[224]	1930.50	306.75
273	SEG[223]	1903.50	306.75
274	SEG[222]	1876.50	306.75
275	SEG[221]	1849.50	306.75
276	SEG[220]	1822.50	306.75

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PAD No.	PIN Name	X	Y
277	SEG[219]	1795.50	306.75
278	SEG[218]	1768.50	306.75
279	SEG[217]	1741.50	306.75
280	SEG[216]	1714.50	306.75
281	SEG[215]	1687.50	306.75
282	SEG[214]	1660.50	306.75
283	SEG[213]	1633.50	306.75
284	SEG[212]	1606.50	306.75
285	SEG[211]	1579.50	306.75
286	SEG[210]	1552.50	306.75
287	SEG[209]	1525.50	306.75
288	SEG[208]	1498.50	306.75
289	SEG[207]	1471.50	306.75
290	SEG[206]	1444.50	306.75
291	SEG[205]	1417.50	306.75
292	SEG[204]	1390.50	306.75
293	SEG[203]	1363.50	306.75
294	SEG[202]	1336.50	306.75
295	SEG[201]	1309.50	306.75
296	SEG[200]	1282.50	306.75
297	SEG[199]	1255.50	306.75
298	SEG[198]	1228.50	306.75
299	SEG[197]	1201.50	306.75
300	SEG[196]	1174.50	306.75
301	SEG[195]	1147.50	306.75
302	SEG[194]	1120.50	306.75
303	SEG[193]	1093.50	306.75
304	SEG[192]	1066.50	306.75
305	SEG[191]	1039.50	306.75
306	SEG[190]	1012.50	306.75
307	SEG[189]	985.50	306.75
308	SEG[188]	958.50	306.75
309	SEG[187]	931.50	306.75
310	SEG[186]	904.50	306.75
311	SEG[185]	877.50	306.75

PAD No.	PIN Name	X	Y
312	SEG[184]	850.50	306.75
313	SEG[183]	823.50	306.75
314	SEG[182]	796.50	306.75
315	SEG[181]	769.50	306.75
316	SEG[180]	742.50	306.75
317	SEG[179]	715.50	306.75
318	SEG[178]	688.50	306.75
319	SEG[177]	661.50	306.75
320	SEG[176]	634.50	306.75
321	SEG[175]	607.50	306.75
322	SEG[174]	580.50	306.75
323	SEG[173]	553.50	306.75
324	SEG[172]	526.50	306.75
325	SEG[171]	499.50	306.75
326	SEG[170]	472.50	306.75
327	SEG[169]	445.50	306.75
328	SEG[168]	418.50	306.75
329	SEG[167]	391.50	306.75
330	SEG[166]	364.50	306.75
331	SEG[165]	337.50	306.75
332	SEG[164]	310.50	306.75
333	SEG[163]	283.50	306.75
334	SEG[162]	256.50	306.75
335	SEG[161]	229.50	306.75
336	SEG[160]	202.50	306.75
337	SEG[159]	175.50	306.75
338	SEG[158]	148.50	306.75
339	SEG[157]	121.50	306.75
340	SEG[156]	94.50	306.75
341	SEG[155]	67.50	306.75
342	SEG[154]	40.50	306.75
343	SEG[153]	13.50	306.75
344	SEG[152]	-13.50	306.75
345	SEG[151]	-40.50	306.75
346	SEG[150]	-67.50	306.75

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PAD No.	PIN Name	X	Y
347	SEG[149]	-94.50	306.75
348	SEG[148]	-121.50	306.75
349	SEG[147]	-148.50	306.75
350	SEG[146]	-175.50	306.75
351	SEG[145]	-202.50	306.75
352	SEG[144]	-229.50	306.75
353	SEG[143]	-256.50	306.75
354	SEG[142]	-283.50	306.75
355	SEG[141]	-310.50	306.75
356	SEG[140]	-337.50	306.75
357	SEG[139]	-364.50	306.75
358	SEG[138]	-391.50	306.75
359	SEG[137]	-418.50	306.75
360	SEG[136]	-445.50	306.75
361	SEG[135]	-472.50	306.75
362	SEG[134]	-499.50	306.75
363	SEG[133]	-526.50	306.75
364	SEG[132]	-553.50	306.75
365	SEG[131]	-580.50	306.75
366	SEG[130]	-607.50	306.75
367	SEG[129]	-634.50	306.75
368	SEG[128]	-661.50	306.75
369	SEG[127]	-688.50	306.75
370	SEG[126]	-715.50	306.75
371	SEG[125]	-742.50	306.75
372	SEG[124]	-769.50	306.75
373	SEG[123]	-796.50	306.75
374	SEG[122]	-823.50	306.75
375	SEG[121]	-850.50	306.75
376	SEG[120]	-877.50	306.75
377	SEG[119]	-904.50	306.75
378	SEG[118]	-931.50	306.75
379	SEG[117]	-958.50	306.75
380	SEG[116]	-985.50	306.75
381	SEG[115]	-1012.50	306.75

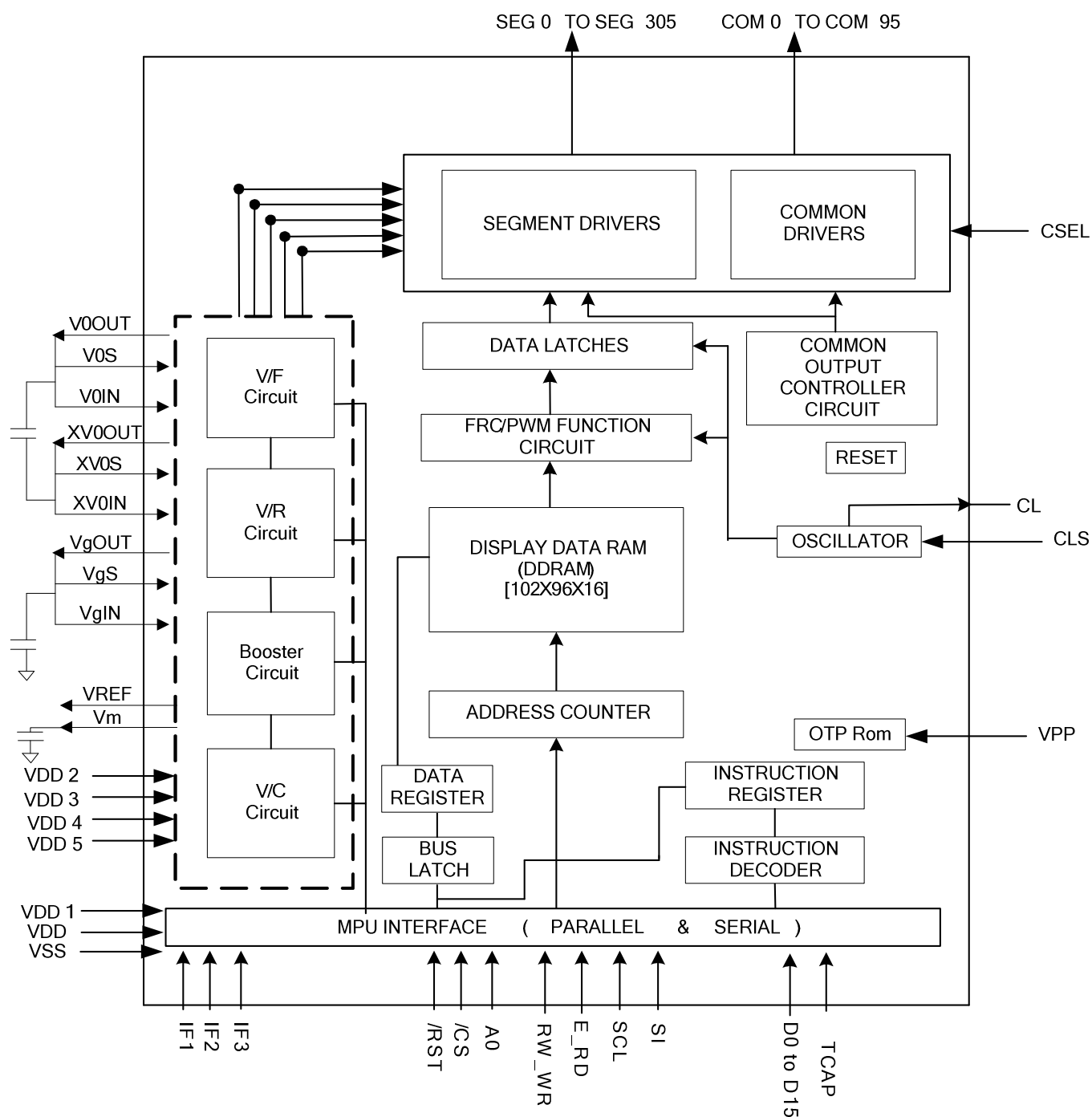
PAD No.	PIN Name	X	Y
382	SEG[114]	-1039.50	306.75
383	SEG[113]	-1066.50	306.75
384	SEG[112]	-1093.50	306.75
385	SEG[111]	-1120.50	306.75
386	SEG[110]	-1147.50	306.75
387	SEG[109]	-1174.50	306.75
388	SEG[108]	-1201.50	306.75
389	SEG[107]	-1228.50	306.75
390	SEG[106]	-1255.50	306.75
391	SEG[105]	-1282.50	306.75
392	SEG[104]	-1309.50	306.75
393	SEG[103]	-1336.50	306.75
394	SEG[102]	-1363.50	306.75
395	SEG[101]	-1390.50	306.75
396	SEG[100]	-1417.50	306.75
397	SEG[99]	-1444.50	306.75
398	SEG[98]	-1471.50	306.75
399	SEG[97]	-1498.50	306.75
400	SEG[96]	-1525.50	306.75
401	SEG[95]	-1552.50	306.75
402	SEG[94]	-1579.50	306.75
403	SEG[93]	-1606.50	306.75
404	SEG[92]	-1633.50	306.75
405	SEG[91]	-1660.50	306.75
406	SEG[90]	-1687.50	306.75
407	SEG[89]	-1714.50	306.75
408	SEG[88]	-1741.50	306.75
409	SEG[87]	-1768.50	306.75
410	SEG[86]	-1795.50	306.75
411	SEG[85]	-1822.50	306.75
412	SEG[84]	-1849.50	306.75
413	SEG[83]	-1876.50	306.75
414	SEG[82]	-1903.50	306.75
415	SEG[81]	-1930.50	306.75
416	SEG[80]	-1957.50	306.75

ST7625

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
417	SEG[79]	-1984.50	306.75	452	SEG[44]	-2929.50	306.75
418	SEG[78]	-2011.50	306.75	453	SEG[43]	-2956.50	306.75
419	SEG[77]	-2038.50	306.75	454	SEG[42]	-2983.50	306.75
420	SEG[76]	-2065.50	306.75	455	SEG[41]	-3010.50	306.75
421	SEG[75]	-2092.50	306.75	456	SEG[40]	-3037.50	306.75
422	SEG[74]	-2119.50	306.75	457	SEG[39]	-3064.50	306.75
423	SEG[73]	-2146.50	306.75	458	SEG[38]	-3091.50	306.75
424	SEG[72]	-2173.50	306.75	459	SEG[37]	-3118.50	306.75
425	SEG[71]	-2200.50	306.75	460	SEG[36]	-3145.50	306.75
426	SEG[70]	-2227.50	306.75	461	SEG[35]	-3172.50	306.75
427	SEG[69]	-2254.50	306.75	462	SEG[34]	-3199.50	306.75
428	SEG[68]	-2281.50	306.75	463	SEG[33]	-3226.50	306.75
429	SEG[67]	-2308.50	306.75	464	SEG[32]	-3253.50	306.75
430	SEG[66]	-2335.50	306.75	465	SEG[31]	-3280.50	306.75
431	SEG[65]	-2362.50	306.75	466	SEG[30]	-3307.50	306.75
432	SEG[64]	-2389.50	306.75	467	SEG[29]	-3334.50	306.75
433	SEG[63]	-2416.50	306.75	468	SEG[28]	-3361.50	306.75
434	SEG[62]	-2443.50	306.75	469	SEG[27]	-3388.50	306.75
435	SEG[61]	-2470.50	306.75	470	SEG[26]	-3415.50	306.75
436	SEG[60]	-2497.50	306.75	471	SEG[25]	-3442.50	306.75
437	SEG[59]	-2524.50	306.75	472	SEG[24]	-3469.50	306.75
438	SEG[58]	-2551.50	306.75	473	SEG[23]	-3496.50	306.75
439	SEG[57]	-2578.50	306.75	474	SEG[22]	-3523.50	306.75
440	SEG[56]	-2605.50	306.75	475	SEG[21]	-3550.50	306.75
441	SEG[55]	-2632.50	306.75	476	SEG[20]	-3577.50	306.75
442	SEG[54]	-2659.50	306.75	477	SEG[19]	-3604.50	306.75
443	SEG[53]	-2686.50	306.75	478	SEG[18]	-3631.50	306.75
444	SEG[52]	-2713.50	306.75	479	SEG[17]	-3658.50	306.75
445	SEG[51]	-2740.50	306.75	480	SEG[16]	-3685.50	306.75
446	SEG[50]	-2767.50	306.75	481	SEG[15]	-3712.50	306.75
447	SEG[49]	-2794.50	306.75	482	SEG[14]	-3739.50	306.75
448	SEG[48]	-2821.50	306.75	483	SEG[13]	-3766.50	306.75
449	SEG[47]	-2848.50	306.75	484	SEG[12]	-3793.50	306.75
450	SEG[46]	-2875.50	306.75	485	SEG[11]	-3820.50	306.75
451	SEG[45]	-2902.50	306.75	486	SEG[10]	-3847.50	306.75

PAD No.	PIN Name	X	Y
487	SEG[9]	-3874.50	306.75
488	SEG[8]	-3901.50	306.75
489	SEG[7]	-3928.50	306.75
490	SEG[6]	-3955.50	306.75
491	SEG[5]	-3982.50	306.75
492	SEG[4]	-4009.50	306.75
493	SEG[3]	-4036.50	306.75
494	SEG[2]	-4063.50	306.75
495	SEG[1]	-4090.50	306.75
496	SEG[0]	-4117.50	306.75
497	COM[94]	-4225.02	306.75
498	COM[92]	-4252.02	306.75
499	COM[90]	-4279.02	306.75
500	COM[88]	-4306.02	306.75
501	COM[86]	-4333.02	306.75
502	COM[84]	-4360.02	306.75
503	COM[82]	-4387.02	306.75
504	COM[80]	-4414.02	306.75
505	COM[78]	-4441.02	306.75
506	COM[76]	-4468.02	306.75
507	COM[74]	-4495.02	306.75
508	COM[72]	-4522.02	306.75
509	COM[70]	-4549.02	306.75
510	COM[68]	-4576.02	306.75
511	COM[66]	-4603.02	306.75
512	COM[64]	-4630.02	306.75
513	COM[62]	-4657.02	306.75
514	COM[60]	-4684.02	306.75

5. BLOCK DIAGRAM



6. PIN DESCRIPTION

6.1 POWER SUPPLY

Name	I/O	Description
VDD	Supply	Power supply for logic circuit (Digital VDD 1.65V~3.0V)
VDD1	Supply	Power supply for OSC circuit (Digital VDD 1.65V~3.0V)
VDD2	Supply	Power supply for Booster Circuit (Analog VDD 2.4V~3.3V)
VDD3	Supply	Power supply for LCD. (Analog VDD 2.4V~3.3V)
VDD4	Supply	Power supply for LCD. (Analog VDD 2.4V~3.3V)
VDD5	Supply	Power supply for LCD. (Analog VDD 2.4V~3.3V)
VSS	Supply	Ground for logic circuit. Ground system should be connected together.
VSS1	Supply	Ground for OSC circuit. Ground system should be connected together.
VSS2	Supply	Ground for Booster Circuit. Ground system should be connected together.
VSS4	Supply	Ground for LCD. Ground system should be connected together.

6.2 LCD Power Supply Pins

Name	I/O	Description						
V0 _{OUT} V0 _{IN} V0 _S	I/O	Positive LCD driver supply voltages. V0_{OUT} is the output voltage of V0 generated by ST7625. V0_{IN} is the input pin of power supply to generate V0 voltage for LCD. V0_S is the input pin of power supply to sense the V0 voltage. V0_{OUT} 、V0_{IN} & V0_S should be connected together by FPC.						
XV0 _{OUT} XV0 _{IN} XV0 _S	I/O	Negative LCD driver supply voltages. XV0_{OUT} is the output voltage of XV0 generated by ST7625. XV0_{IN} is the input pin of power supply to generate XV0 voltage for LCD. XV0_S is the input pin of power supply to sense the XV0 voltage. XV0_{OUT} 、XV0_{IN} & XV0_S should be connected together by FPC.						
Vg _{OUT} Vg _{IN} Vg _S Vm	I/O	Bias LCD driver supply voltages. Vg_{OUT} is the output voltage of Vg generated by ST7625. Vg_{IN} is the input pin of power supply to generate Vg voltage for LCD. Vg_S is the input pin of power supply to sense the Vg voltage. Vg_{OUT} 、Vg_{IN} & Vg_S should be connected together by FPC. Vm is the I/O pin of LCD bias supply voltage Voltages should have the following relationship; $V0 > Vg > Vm > VSS > XV0$, $0.7V < Vm < VDDA - 0.7V$ and $1.8V < Vg < 2 \times VDDA$. When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias. <table border="1"> <thead> <tr> <th>LCD bias</th><th>Vg</th><th>Vm</th></tr> </thead> <tbody> <tr> <td>1/N bias</td><td>$(2/N) \times V0$</td><td>$(1/N) \times V0$</td></tr> </tbody> </table> NOTE: N = 5 to 12	LCD bias	Vg	Vm	1/N bias	$(2/N) \times V0$	$(1/N) \times V0$
LCD bias	Vg	Vm						
1/N bias	$(2/N) \times V0$	$(1/N) \times V0$						

6.3 SYSTEM CONTROL

Name	I/O	Description
CLS	I	Reserved for testing only. Please fix this pin to VDD.
CL	I/O	Reserved for testing only. Leave this pin open.
CSEL	I	This pin should connect to VDD.
TCAP	I/O	Test pin. Leave it open.
VREF	O	Reference voltage output for monitor only. Leave it open.
VPP	I	When writing OTP, it needs external power supply voltage 7.5V~7.75V (>4 mA) input to write successfully.

6.4 MICROPROCESSOR INTERFACE

Name	I/O	Description																												
RST	I	Reset input pin, when RST is "L", initialization is executed.																												
IF[3:1]	I	Parallel / Serial data input select input <table><thead><tr><th>IF3</th><th>IF2</th><th>IF1</th><th>MPU interface type</th></tr></thead><tbody><tr><td>H</td><td>H</td><td>H</td><td>80 series 16-bit parallel</td></tr><tr><td>L</td><td>H</td><td>H</td><td>80 series 8-bit parallel</td></tr><tr><td>L</td><td>L</td><td>H</td><td>68 series 16-bit parallel</td></tr><tr><td>H</td><td>H</td><td>L</td><td>68 series 8-bit parallel</td></tr><tr><td>H</td><td>L</td><td>L</td><td>9-bit serial (3 line)</td></tr><tr><td>L</td><td>L</td><td>L</td><td>8-bit serial (4 line)</td></tr></tbody></table> Note Refer to table 7.1.1 for detail serial interface connections.	IF3	IF2	IF1	MPU interface type	H	H	H	80 series 16-bit parallel	L	H	H	80 series 8-bit parallel	L	L	H	68 series 16-bit parallel	H	H	L	68 series 8-bit parallel	H	L	L	9-bit serial (3 line)	L	L	L	8-bit serial (4 line)
IF3	IF2	IF1	MPU interface type																											
H	H	H	80 series 16-bit parallel																											
L	H	H	80 series 8-bit parallel																											
L	L	H	68 series 16-bit parallel																											
H	H	L	68 series 8-bit parallel																											
H	L	L	9-bit serial (3 line)																											
L	L	L	8-bit serial (4 line)																											
/CS	I	Chip select input pins Data / Instruction I/O is enabled only when /CS is "L". When chip select is non-active, D0 to D15 become high impedance.																												
A0	I	Register select input pin A0 = "H": D0 to D15 or SI are display data A0 = "L": D0 to D15 or SI are control Command In 3-line or 4-line interface this PIN is define to SCL. A0 pin is used to input serial clock when the serial interface is selected (SCL). (3 line and 4 line)																												

RW_WR	I	Read / Write execution control pin		
		MPU type	RW_WR	Description
		6800-series	RW	Read / Write control input pin R/W = “H” : read R/W = “L” : write
		8080-series	/WR	Write enable clock input pin The data on D0 to D15 are latched at the rising edge of the /WR signal.
		When in the serial interface, connect it to VDD.		

E_RD	I	Read / Write execution control pin		
		MPU Type	E_RD	Description
		6800-series	E	Read / Write control input pin R/W = “H”: When E is “H”, D0 to D15 are in an output status. R/W = “L”: The data on D0 to D15 are latched at the falling edge of the E signal.
		8080-series	/RD	Read enable clock input pin When /RD is “L”, D0 to D15 are in an output status.
		When in the serial interface, connect it to VDD.		

D15 to D0	I/O	They connect to the standard 8-bit or 16 bit MPU bus via the 8/16 –bit bi-directional bus.		
		When the following interface is selected and the /CS pin is high, the following pins become high impedance.		
		1. In 8-bit parallel: D15-D8 pins are in the state of high impedance should connect to VDD.		
		2. In 3-line/4-line interface D0 pad will be used for SI function (SI)		
		3. In 4-line interface D1 pad will be used for A0 function		

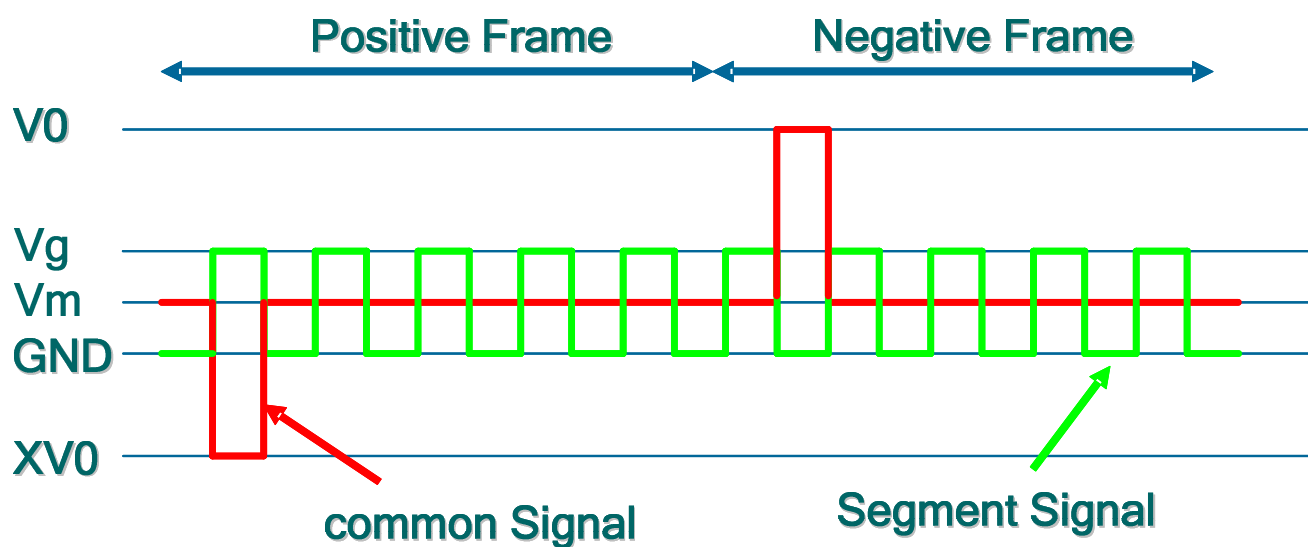
D15 to D0	I/O	4. In Serial interface: unused pins are in the state of high impedance should connect to VDD.		
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NOTE :

1. The MPU Interface (control bus and data bus) can not be left floating in any operation mode.
2. Unused pins should connect to VDD (Supply Digital Voltage).

6.5 LCD DRIVER OUTPUTS

Name	I/O	Description																										
SEG0 to SEG305	O	LCD segment driver outputs																										
		The display data and the frame inversion signal control the output voltage of segment driver.																										
		<table><tr><th rowspan="2">Display data</th><th rowspan="2">Frame Inversion (Internal)</th><th colspan="2">Segment driver output voltage</th></tr><tr><th>Normal display</th><th>Reverse display</th></tr><tr><td>H</td><td>H</td><td>Vg</td><td>VSS</td></tr><tr><td>H</td><td>L</td><td>VSS</td><td>Vg</td></tr><tr><td>L</td><td>H</td><td>VSS</td><td>Vg</td></tr><tr><td>L</td><td>L</td><td>Vg</td><td>VSS</td></tr><tr><td colspan="2">Sleep-In mode</td><td>VSS</td><td>VSS</td></tr></table>	Display data	Frame Inversion (Internal)	Segment driver output voltage		Normal display	Reverse display	H	H	Vg	VSS	H	L	VSS	Vg	L	H	VSS	Vg	L	L	Vg	VSS	Sleep-In mode		VSS	VSS
		Display data			Frame Inversion (Internal)	Segment driver output voltage																						
			Normal display	Reverse display																								
		H	H	Vg	VSS																							
		H	L	VSS	Vg																							
		L	H	VSS	Vg																							
L	L	Vg	VSS																									
Sleep-In mode		VSS	VSS																									
COM0 to COM95	O	LCD common driver outputs																										
		The internal scanning data and M signal control the output voltage of common driver.																										
		<table><tr><th>Scan data</th><th>Frame Inversion (Internal)</th><th>Common driver output voltage</th></tr><tr><td>H</td><td>H</td><td>XV0</td></tr><tr><td>H</td><td>L</td><td>V0</td></tr><tr><td>L</td><td>H</td><td>Vm</td></tr><tr><td>L</td><td>L</td><td>Vm</td></tr><tr><td colspan="2">Sleep-In mode</td><td>VSS</td></tr></table>	Scan data	Frame Inversion (Internal)	Common driver output voltage	H	H	XV0	H	L	V0	L	H	Vm	L	L	Vm	Sleep-In mode		VSS								
		Scan data	Frame Inversion (Internal)	Common driver output voltage																								
		H	H	XV0																								
		H	L	V0																								
		L	H	Vm																								
		L	L	Vm																								
Sleep-In mode		VSS																										



ST7625 I/O PIN ITO Resister Limitation

Pin Name	ITO Resister
VDD, VDD1~VDD5, VSS,VSS1,VSS2,VSS4	<100Ω
V0 _{IN} , V0 _{OUT} , V0 _S , XV0 _{IN} , XV0 _{OUT} , XV0 _S , Vg _{IN} , Vg _{OUT} , Vg _S , Vm	<300Ω
VPP	<50Ω
A0, E_RD, RW_WR, /CS, D0 ...D15, (SI), (SCL)	<1KΩ
/RST	<10KΩ
IF[3:1], CLS, CSEL	<1KΩ
TCAP, CL, VREF	Floating

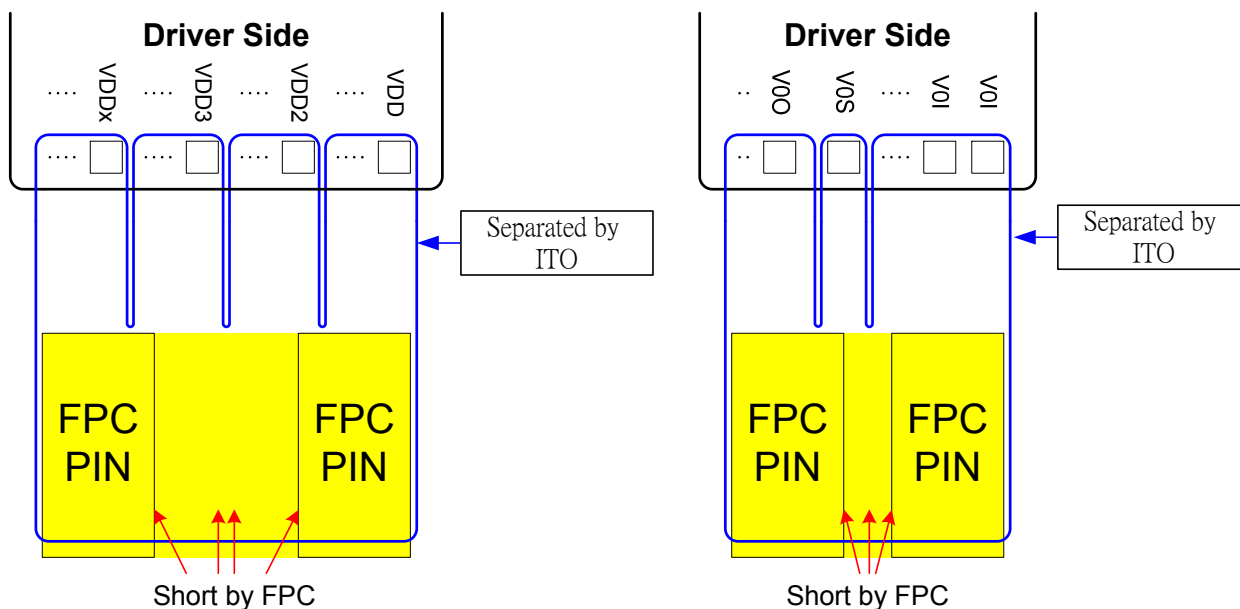
NOTE:

1. Make sure that the ITO resistance of COM0 ~ COM69 is equal, and so is it of SEG0 ~ SEG293.

These Limitations include the bottleneck of ITO layout.

2. To avoid the noise in different power system affect other power system, please separate different power source on ITO layout.

3. The V0, XV0 and Vg power circuits have output pins, input pins and a sensor input. To avoid the power noise affects the sensor of the power circuits. The trace should be separated by ITO and should be connected together by FPC.



7. FUNCTIONAL DESCRIPTION

7.1 MICROPROCESSOR INTERFACE

Chip Select Input

/CS pin is chip selection. The ST7625 is active when /CS=L. In serial interface mode, the internal shift register and the counter are reset when /CS=H.

7.1.1 Selecting Parallel / Serial Interface

ST7625 has six types of interface with an MPU, which are two serial and four parallel interfaces. The parallel or serial interface is determined by IF pin as shown in Table 7.1.1.

Table 7.1.1 Parallel / Serial Interface Mode

I/F Mode			I/F Description	Pin Assignment							
IF1	IF2	IF3		/CS	A0	E_RD	RW_WR	D15 to D8	D7 to D2	D0	D1
H	H	H	80 serial 16-bit parallel	/CS	A0	/RD	/WR	D15 ~ D8	D7 ~ D2	D0	D1
H	H	L	80 serial 8-bit parallel	/CS	A0	/RD	/WR	--	D7 ~ D2	D0	D1
H	L	L	68 serial 16-bit parallel	/CS	A0	E	R/W	D15 ~ D8	D7 ~ D2	D0	D1
L	H	H	68 serial 8-bit parallel	/CS	A0	E	R/W	--	D7 ~ D2	D0	D1
L	L	L	8-bit SPI mode (4 line)	/CS	SCL	--	--	--	--	SI	A0
L	L	H	9-bit SPI mode (3 line)	/CS	SCL	--	--	--	--	SI	--

NOTE: When these pins are set to any other combination, A0, E_RD and RW_WR inputs are disabled and D0 to D15 are high impedance.

7.1.2 8-bit or 16-bit Parallel Interface

The ST7625 identifies the type of the data bus signals according to the combination of A0, /RD (E) and /WR (W/R) signals, as shown in Table 7.1.2.

Table 7.1.2 Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	R/W	E	/WR	/RD	
H	H	↑	H	↓	Display data read out
H	H	↑	H	↓	Register status read
L	L	↓	↑	H	Insturction write
H	L	↓	↑	H	Display data write

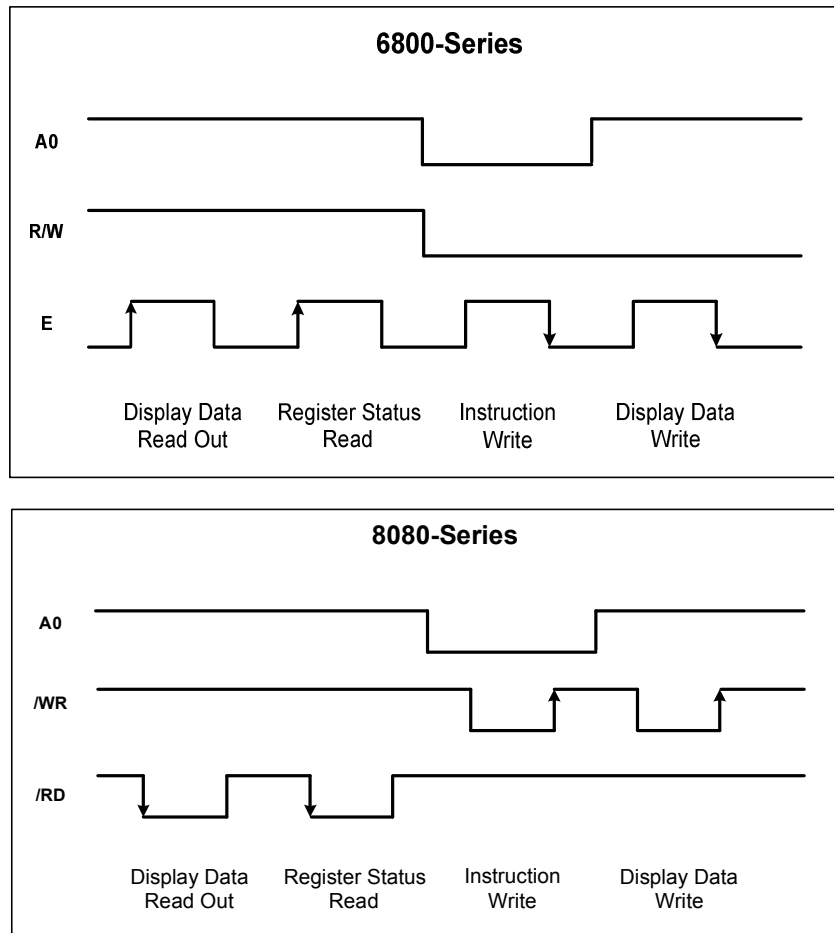


Figure 7.1 Parallel Data Transfer Example Chart

Relation between Data Bus and Gradation Data

The interface of ST7625 supports 256 color display, 4096 color display, 65K color display, truncated 262K color display, and truncated 16M color display.

When using 256, 4096, 65K, 262K, and 16M color display; you can specify color for each of R, G, B using the palette function.

Use the command for switching between these modes.

(1) 256 color input mode

1. 8-bit interface

D7, D6, D5, D4, D3, D2, D1, D0: **RRRGGGBB** 1st writes

There is only 1 write operation for 1 pixel data.

The data of a single pixel is written in the display data RAM when the 1st write operation finishes.

(2) 4096-color display

(1-1) Type A 4096 color display

1. 8-bit interface

D7, D6, D5, D4, D3, D2, D1, D0: **RRRRGGGG** 1st writes

D7, D6, D5, D4, D3, D2, D1, D0: **BBBBRRRR** 2nd writes

D7, D6, D5, D4, D3, D2, D1, D0: **GGGGBBBB** 3rd writes

There are 3 write operations for 2 pixel data.

The data of a single pixel is written in the display data RAM when the 2nd write operation finishes, and the 2nd pixel data is written in the display data RAM when the 3rd write operation finishes.

(1-2) Type B 4096 color display

1. 8-bit interface

D7, D6, D5, D4, D3, D2, D1, D0: **XXXXRRRR** 1st writes

D7, D6, D5, D4, D3, D2, D1, D0: **GGGGBBBB** 2nd writes

There are 2 write operations for 1 pixel data.

The data of a single pixel is written in the display data RAM when the 2nd write operation finishes. "X" are ignored dummy bits.

2. 16-bit interface

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: **XXXXRRRRGGGGBBBB**

There is only 1 write operation for 1 pixel data.

The data of a single pixel is written in the display data RAM when the 1st write operation finishes. "X" are ignored dummy bits.

(3) 65K color input mode

1. 8-bit interface

D7, D6, D5, D4, D3, D2, D1, D0: **RRRRGGGG** 1st writes

D7, D6, D5, D4, D3, D2, D1, D0: **GGGBBBBB** 2nd writes

There are 2 write operations for 1 pixel data.

The data of a single pixel is written in the display data RAM when the 2nd write operation finishes.

2. 16-bit interface

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: **RRRRGGGGGGBBBB** 1st writes

There is only 1 write operation for 1 pixel data.

The data of a single pixel is written in the display data RAM when the 1st write operation finishes.

(4) Truncated 262K color input mode

1. 8-bit interface

D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRXX 1st writes

D7, D6, D5, D4, D3, D2, D1, D0: GGGGGGXX 2nd writes

D7, D6, D5, D4, D3, D2, D1, D0: BBBBXX 3rd writes

The data of a single pixel is read after the third write operation as shown, and it is written in the display RAM.

"X" is dummy bit, and it is ignored for display.

2. 16-bit interface

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRXXGGGGGGXX 1st writes

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: BBBBXXXXXXXXXXXX 2nd writes

The data of a single pixel is read after the second write operation as shown, and it is written in the display RAM.

(5) Truncated 16M color input mode

1. 8-bit interface

D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRRR 1st writes

D7, D6, D5, D4, D3, D2, D1, D0: GGGGGGGG 2nd writes

D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBBB 3rd writes

The data of a single pixel is read after the third write operation as shown, and it is written in the display RAM.

2. 16-bit interface

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRRRGGGGGG 1st writes

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBBBXXXXXXXX 2nd writes

The data of a single pixel is read after the second write operation as shown, and it is written in the display RAM.

7.1.3 8-bit and 9-bit Serial Interface

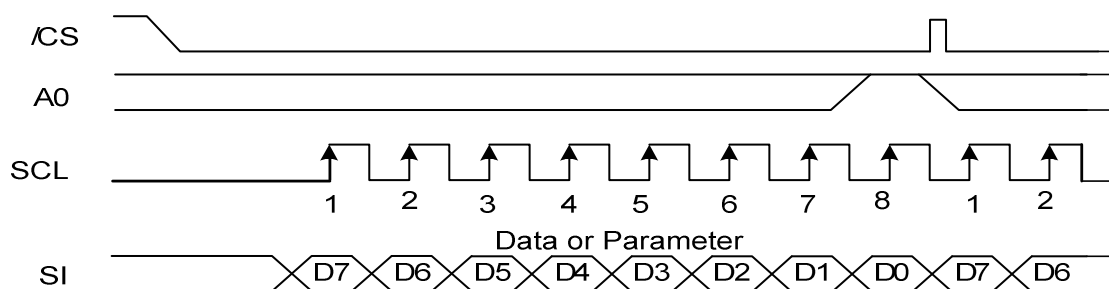
The 8-bit serial interface uses four pins /CS, SI, SCL, and A0 to enter commands and data. Meanwhile, the 9-bit serial interface uses three pins /CS, SI and SCL for the same purpose.

Data read is not available in the serial interface. Data entered must be 8 bits for each time.

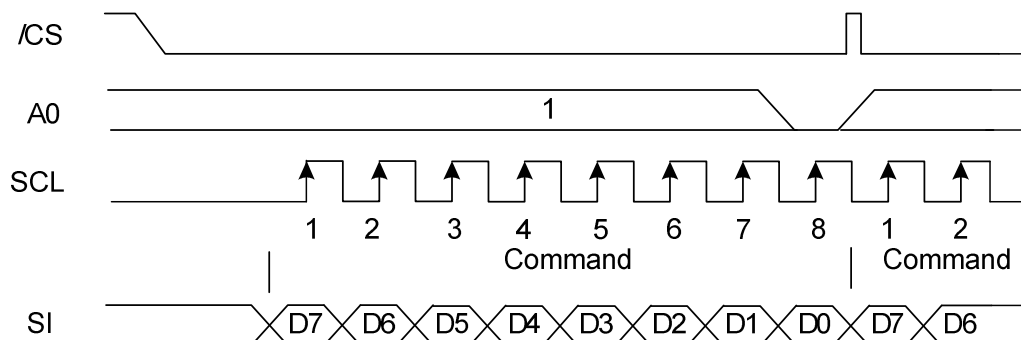
The relation between gray-scale data and data bus in the serial input is the same as that in the 8-bit parallel interface mode at every gradation.

(1) 8-bit serial interface (4-line)

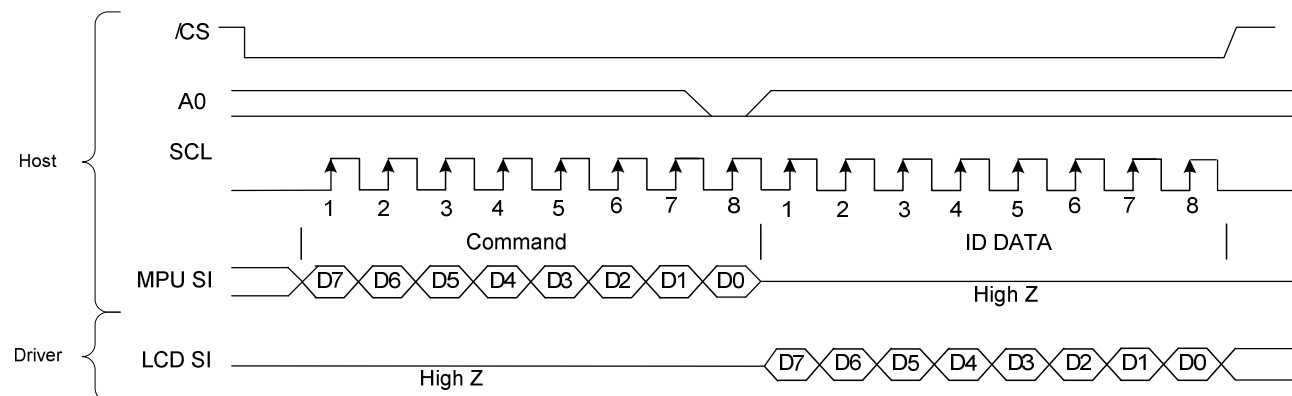
When entering data (parameters): A0= HIGH at the rising edge of the 8th SCL.



When entering command: A0= LOW at the rising edge of the 8th SCL

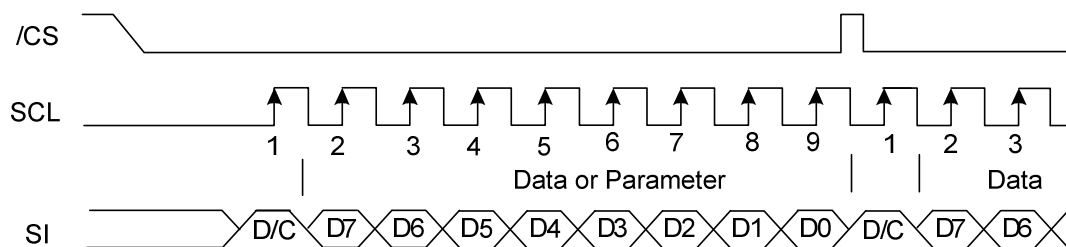


When entering reading command:

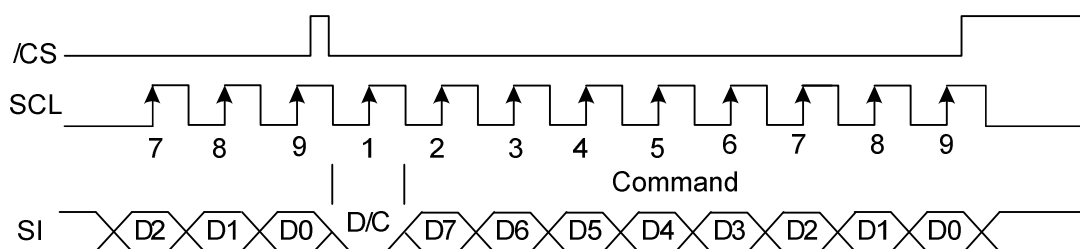


(2) 9-bit serial interface (3-line)

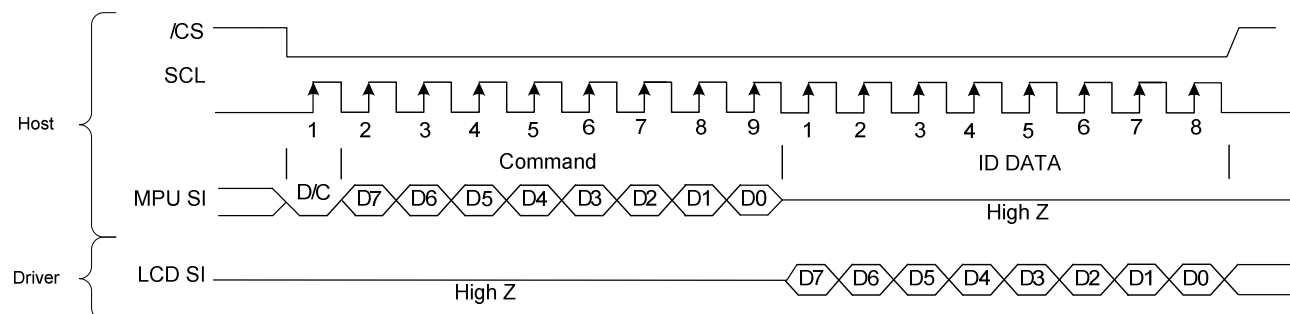
When entering data (parameters): SI= HIGH at the rising edge of the 1st SCL.



When entering command: SI= LOW at the rising edge of the 1st SCL.



When entering reading command:

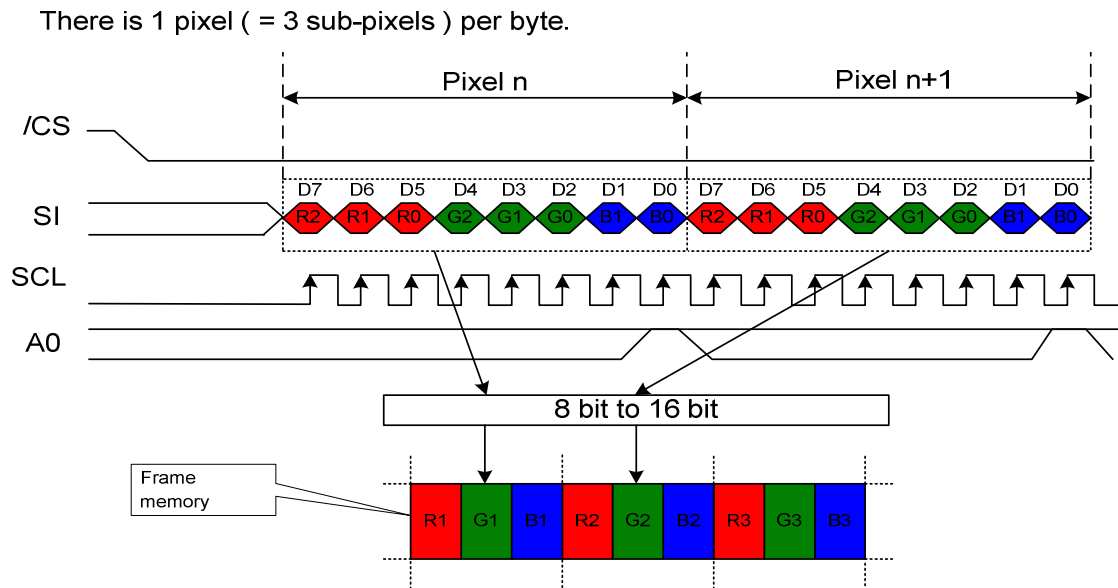


- If /CS is set to HIGH while the 8 bits from D7 to D0 are entered, the data concerned is invalidate. Before entering succeeding sets of data, you must correctly input the data concerned again.
- In order to avoid data transfer error due to incoming noise, it is recommended to set /CS at HIGH on byte basis to initialize the serial-to-parallel conversion counter and the register
- When executing the command RAMWR, set /CS to HIGH after writing the last address. The internal shift register and the counter will reset when /CS =H.

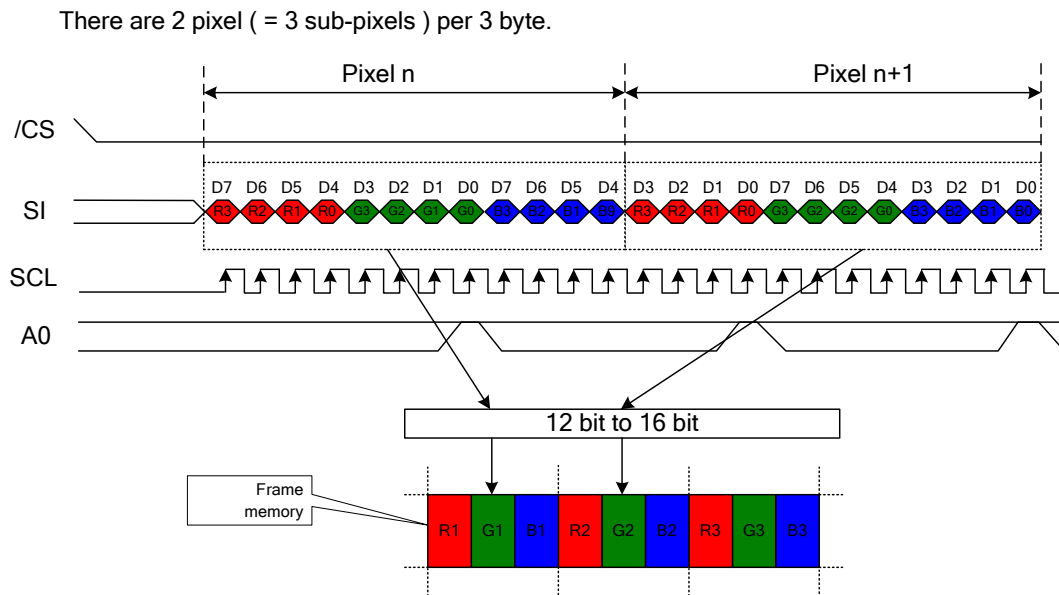
7.1.4 8-bit and 9-bit Serial Interface Data Color Coding

8-bit serial interface (4-line)

(1) R 3-bit, G 3-bit, B 2-bit, 256 colors

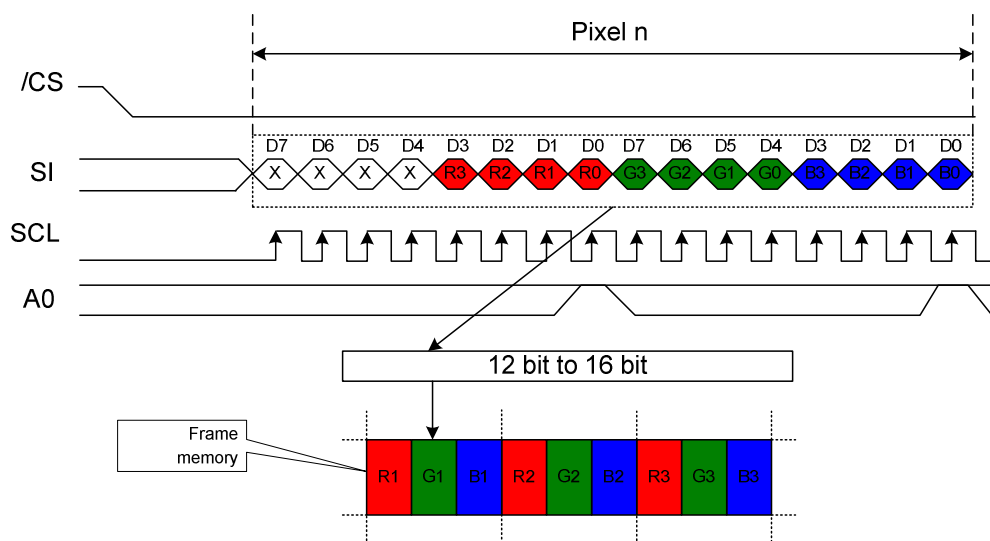


(2) R 4-bit, G 4-bit, B 4-bit, 4,096 colors – Type A



(3) R 4-bit, G 4-bit, B 4-bit, 4,096 colors – Type B

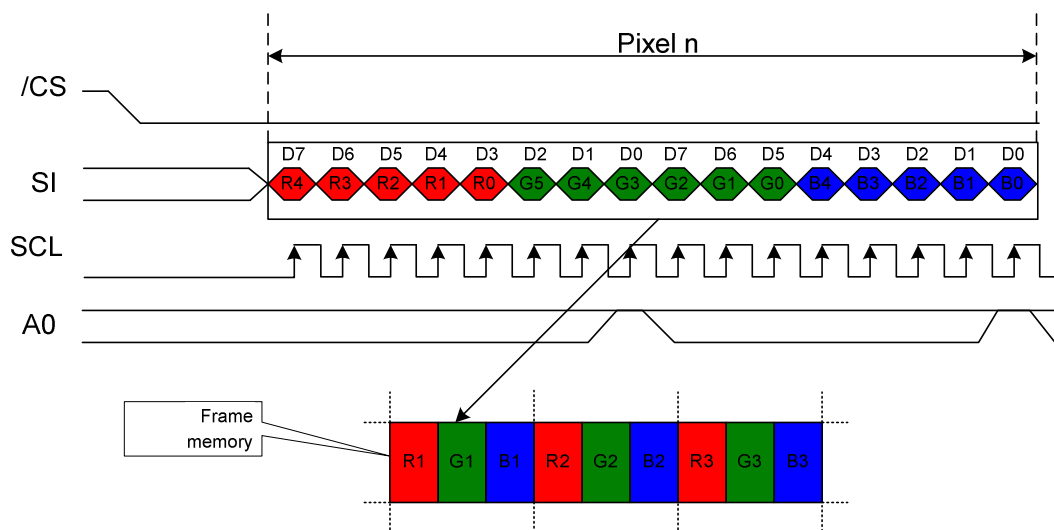
There is 1 pixel (= 3 sub-pixels) per 2 bytes.



Note: R3, G3, B3 are the most significant bits and R0, G0, B0 are the least significant bits.

(4) R 5-bit, G 6-bit, B 5-bit, 65,536 colors

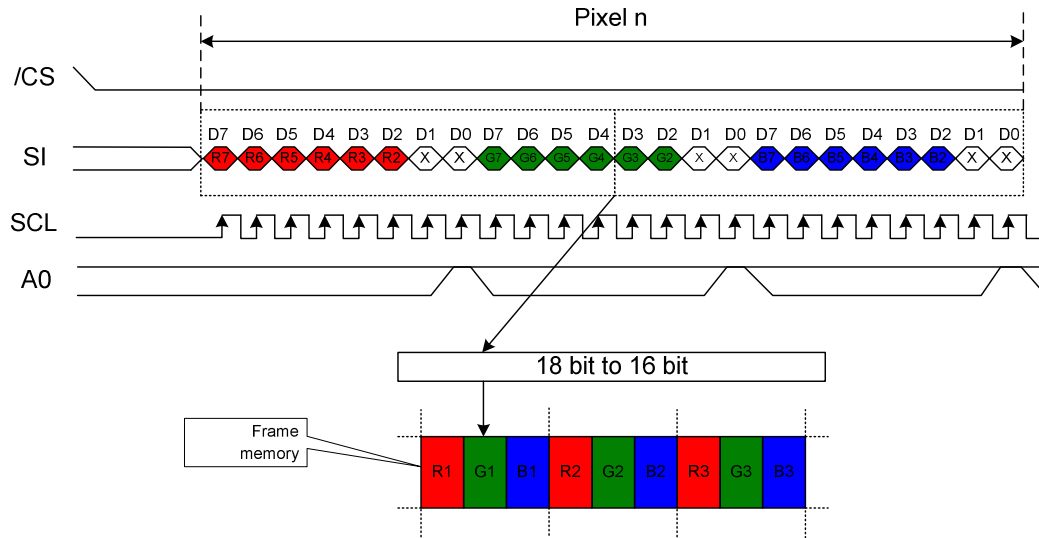
There is 1 pixel (= 3 sub-pixels) per 2 byte.



Note: R4, G5, B4 are the most significant bits and R0, G0, B0 are the least significant bits.

(5) R 6-bit, G 6-bit, B 6-bit, 262k colors

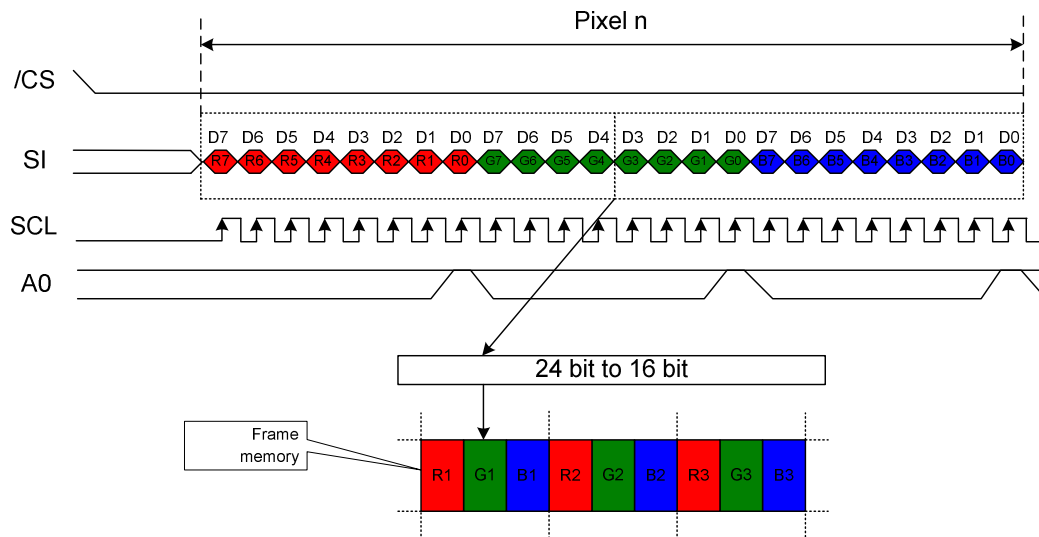
There is 1 pixel (= 3 sub-pixels) per 3 byte.



Note: R7, G7, B7 are the most significant bits and R2, G2, B2 are the least significant bits.

(6) R 8-bit, G 8-bit, B 8-bit, 16M colors

There is 1 pixel (= 3 sub-pixels) per 3 byte.

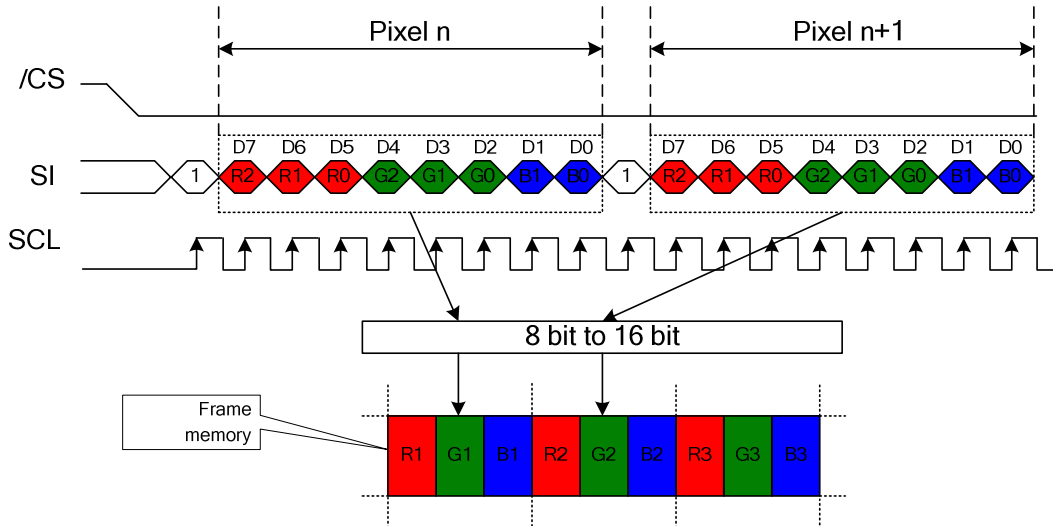


Note: R7, G7, B7 are the most significant bits and R0, G0, B0 are the least significant bits.

9-bit serial interface (3-line)

(1) R 3-bit, G 3-bit, B 2-bit, 256 colors

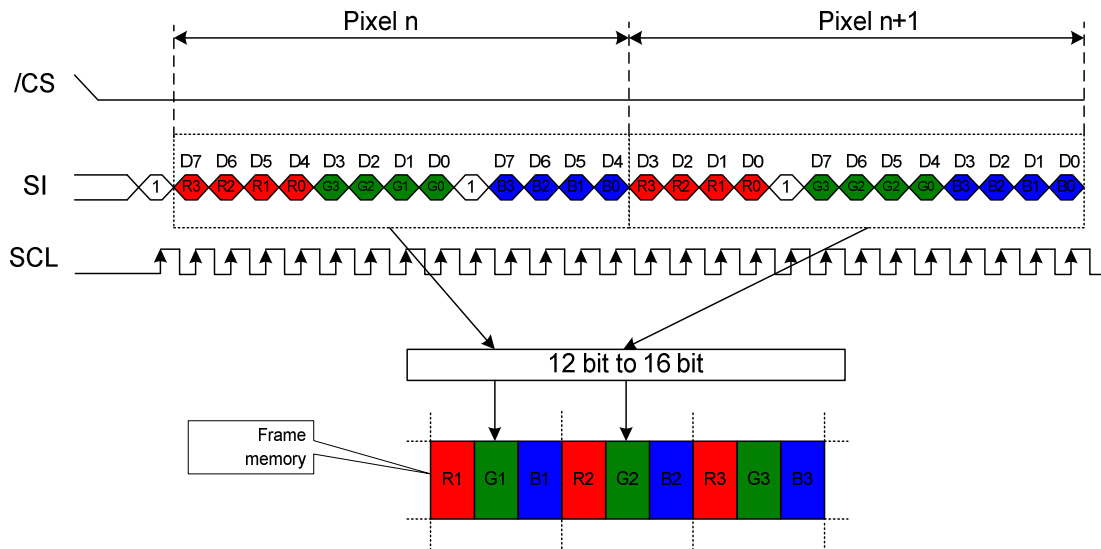
There is 1 pixel (= 3 sub-pixels) per byte.



Note: R2, G2, B1 are the most significant bits and R0, G0, B0 are the least significant bits.

(2) R 4-bit, G 4-bit, B 4-bit, 4,096 colors – Type A

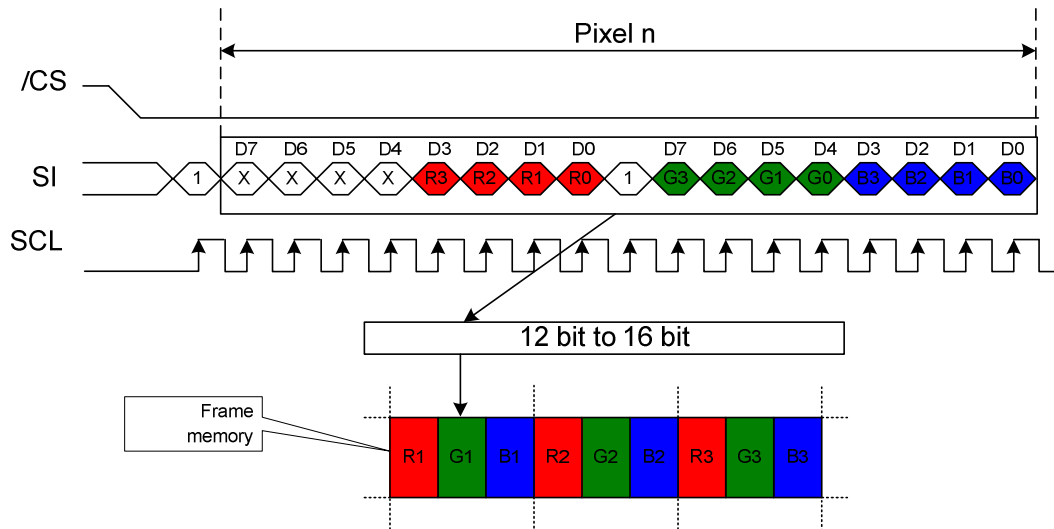
There are 2 pixel (= 3 sub-pixels) per 3 byte.



Note: R3, G3, B3 are the most significant bits and R0, G0, B0 are the least significant bits.

(3) R 4-bit, G 4-bit, B 4-bit, 4,096 colors – Type B

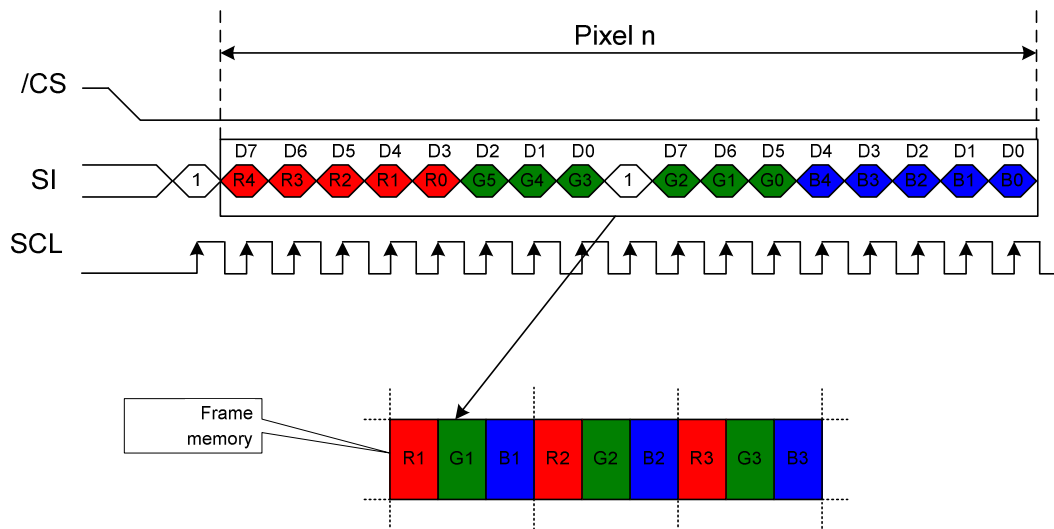
There is 1 pixel (= 3 sub-pixels) per 2 bytes.



Note: R3, G3, B3 are the most significant bits and R0, G0, B0 are the least significant bits.

(4) R 5-bit, G 6-bit, B 5-bit, 65,536 colors

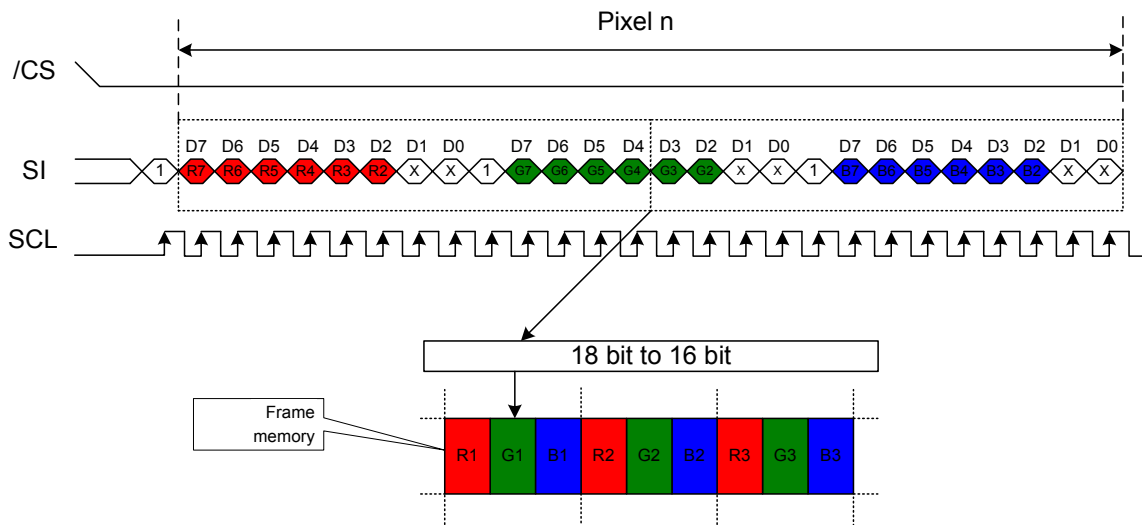
There is 1 pixel (= 3 sub-pixels) per 2 byte.



Note: R4, G5, B4 are the most significant bits and R0, G0, B0 are the least significant bits.

(5) R 6-bit, G 6-bit, B 6-bit, 262k colors

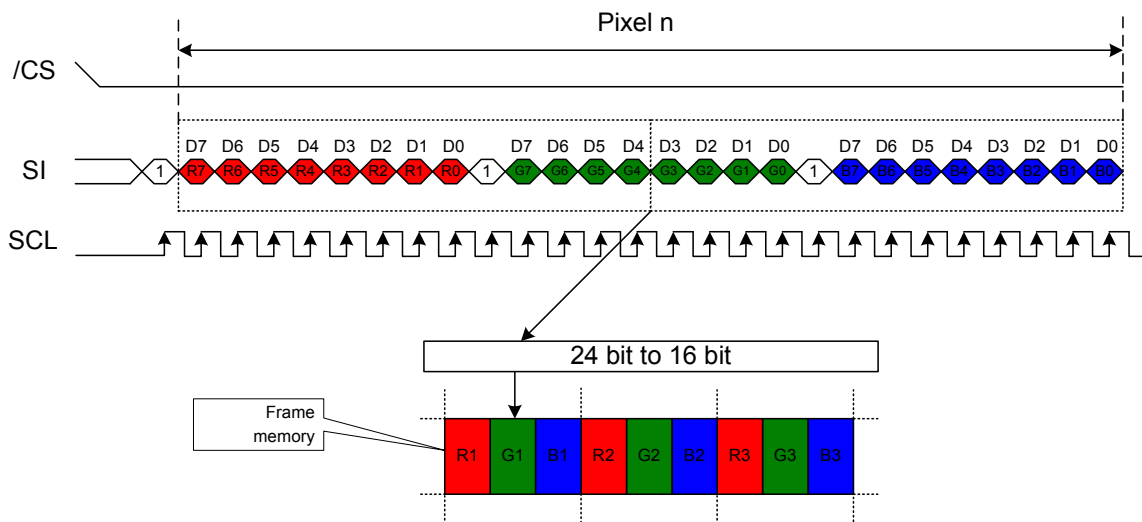
There is 1 pixel (= 3 sub-pixels) per 3 byte.



Note: R7, G7, B7 are the most significant bits and R2, G2, B2 are the least significant bits.

(6) R 8-bit, G 8-bit, B 8-bit, 16M colors

There is 1 pixel (= 3 sub-pixels) per 3 byte.



Note: R7, G7, B7 are the most significant bits and R0, G0, B0 are the least significant bits.

7.2 ACCESS TO DDRAM AND INTERNAL REGISTERS

ST7625 realizes high-speed data transfer because the access from MPU is a sort of pipeline processing done via the bus holder attached to the internal, requiring the cycle time alone without needing the wait time.

For example, when MPU writes data to the DDRAM, the data is once held by the bus holder and then written to the DDRAM before the succeeding write cycle is started. When MPU reads data from the DDRAM, the first read cycle is dummy and the bus holder holds the data read in the dummy cycle, and then it read from the bus holder to the system bus in the succeeding read cycle. Figure 7.2 illustrates these relations.

In 80-series interface mode:

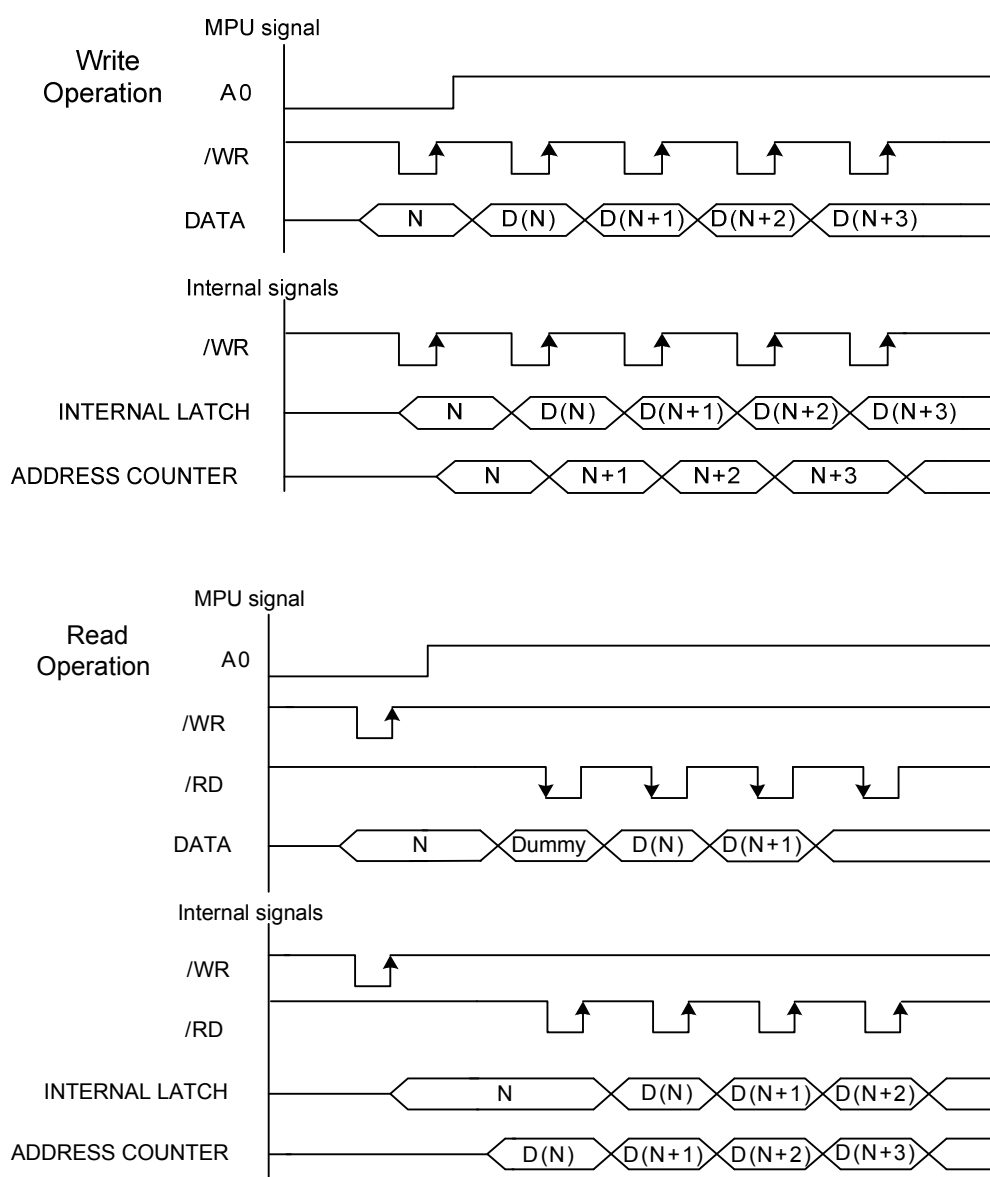


Figure 7.2

7.3 DISPLAY DATA RAM (DDRAM)

7.3.1 DDRAM

It is 102 X 96 X 16 bits capacity RAM prepared for storing dot data. Refer to the following memory map for the RAM configuration.

Memory Map

RGB alignment														
Data control command					Column									
	(MADCTR) MX=0				0		1				101			
														
	(MADCTR) MX=1				101		100				0			
														
	Color				R	G	B	R	G	B		R	G	B
Data														
Page														
	(MADCTR) MY=0		(MADCTR) MY=1											
	0		95											
	1		94											
	2		93											
	3		92											
	4		91											
	5		90											
	6		89											
	7		88											
	:		:											
	88		7											
	89		6											
	90		5											
	91		4											
	92		3											
	93		2											
	94		1											
	95		0											
	SEGout					0	1	2	3	4	5		303	304

You can change position of R and B with MADCTR command.

7.3.2 Address Counter

The address counter sets the addresses of the display data RAM for writing.

Data is written pixel into the RAM matrix of ST7625. The data for one pixel or two pixels is collected (RGB 5-6-5-bit), according to the data formats. As soon as this pixel-data information is complete, the "Write access" is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=101 (65hex) and Y=0 to Y=95 (5Fh). Addresses outside these ranges are not allowed.

Before writing to the RAM, a window must be defined into which will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=101 (65h), YE=95 (5Fh).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (MV=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS). For flexibility in handling a wide variety of display architectures, the commands "CASET, RASET" and "MADCTR" (see section "9.1.21"), define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Figure 7.3 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data must be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as below:

Condition	Column Counter	Row Counter
When RAMWR command is accepted	Return to "Start Column (XS)"	Return to "Start Row (YS)"
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than "End Column (XE)"	Return to "Start Column (XS)"	Increment by 1
The Column counter value is larger than "End Column (XE)" and the Row counter value is larger than "End Row (YE)"	Return to "Start Column (XS)"	Return to "Start Row (YS)"

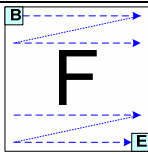
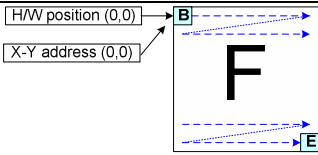
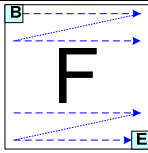
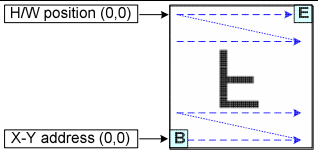
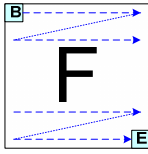
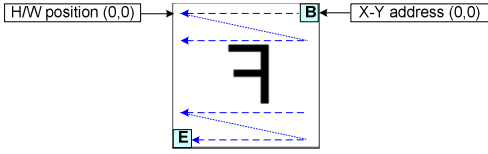
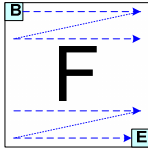
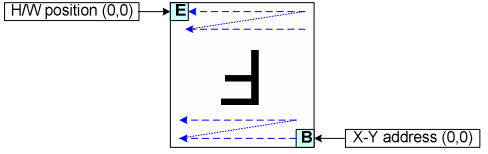
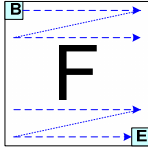
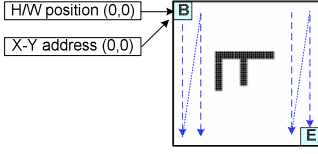
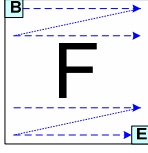
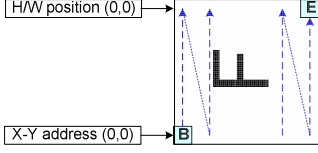
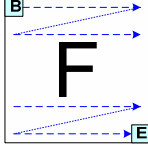
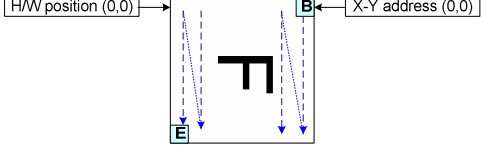
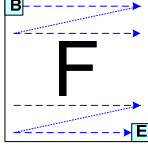
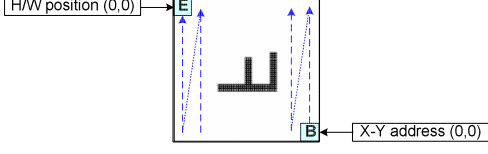
Display Data Direction	MADCTR Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

Figure 7.3

Frame Data Write Direction According to the MADCTR parameters (MV, MX and MY)

7.3.3 I/O Buffer Circuit

It is the bi-directional buffer used when MPU reads or writes the DDRAM. Since MPU's read or write of DDRAM is performed independently from data output to the display data latch circuit, asynchronous access to the DDRAM when the LCD is turned on does not cause troubles such as flicking of the display images.

7.3.4 Scroll Address Circuit

The circuit associates lines on DDRAM with COM output. ST7625 processes signals for the liquid crystal display on 1-line basis. Thus, when specifying a specific area in the area scroll display or partial display, you must designate it in line.

7.3.5 Display data Latch Circuit

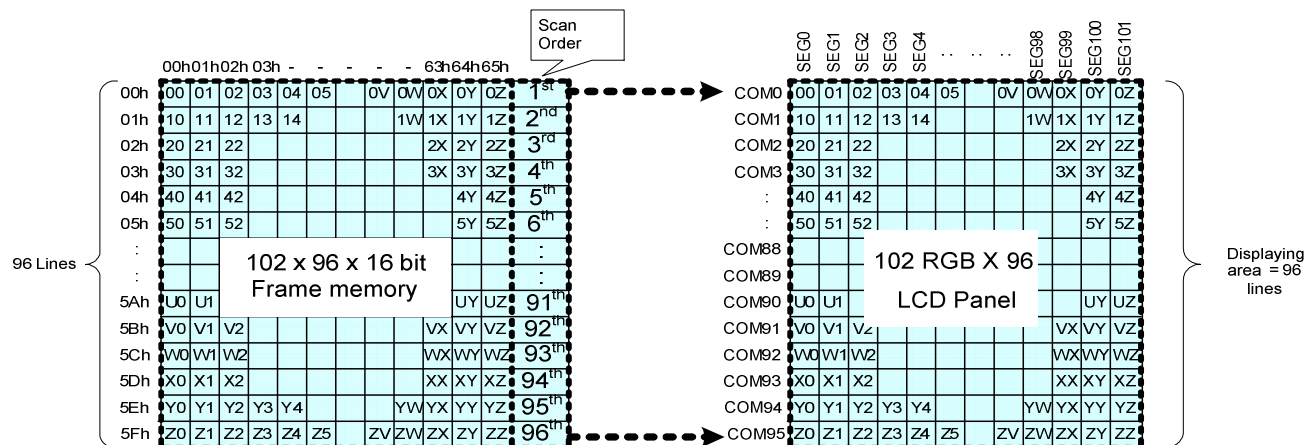
This circuit is used to temporarily hold display data to be output from the DDRAM to the SEG decoder circuit. Since display normal/inverse and display on/off commands are used to control data in the latch circuit alone, they do not modify data in the DDRAM.

7.3.6 Normal Display On or Partial Mode On, Vertical Scroll Off

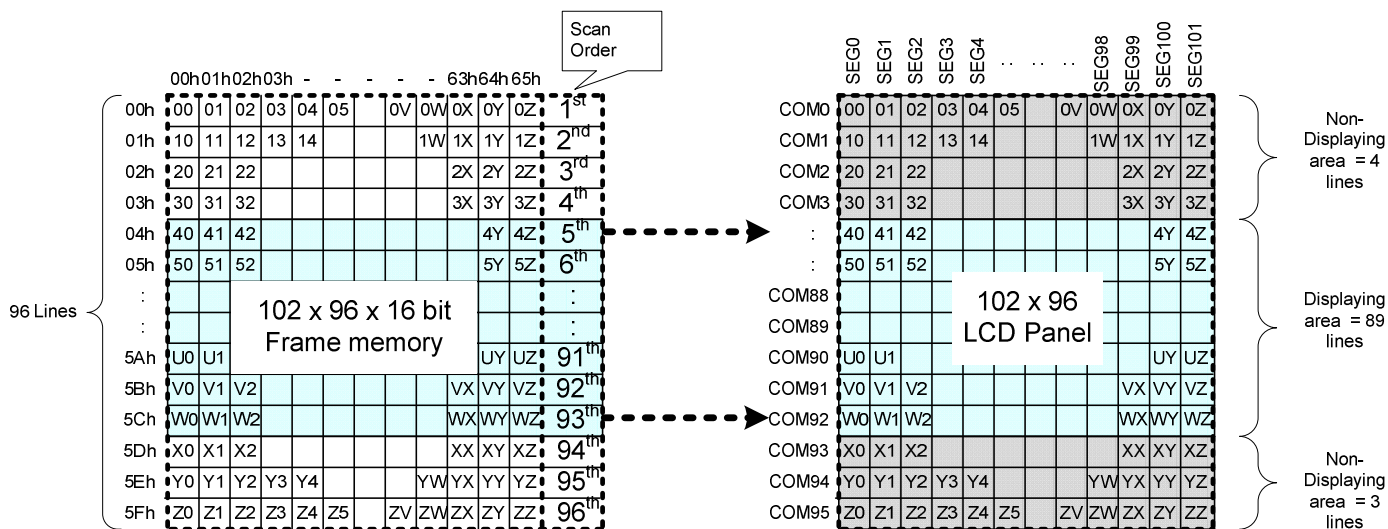
In this mode, contents of the frame memory within an area where column address is 00h to 65h and row address is 00h to 5Fh is displayed.

To display a dot on leftmost top corner, store the dot data at (column address, row address) = (0,0).

Example1) Normal Display On



Example2) Partial Display On: PSL[6:0] = 04h, PEL[6:0] = 5Eh, MADCTR (ML)=0



7.3.7 Vertical Scroll

Rolling Scroll

There is just one type of vertical scrolling, which is determined by the commands "Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

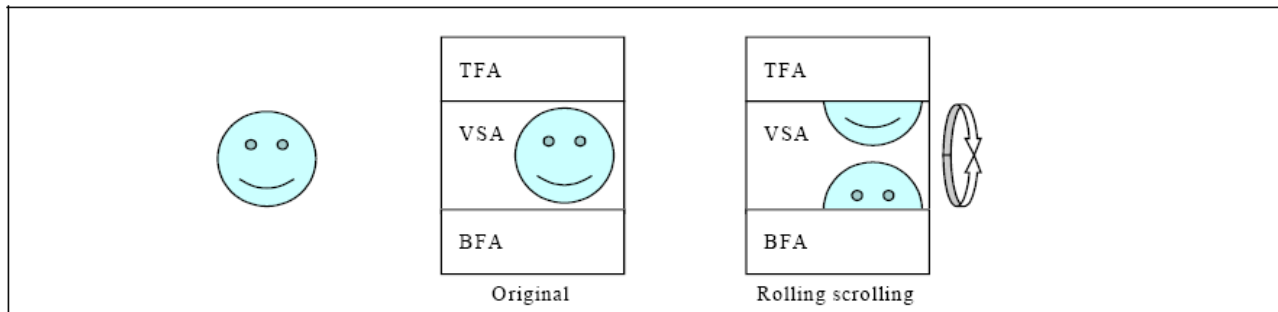
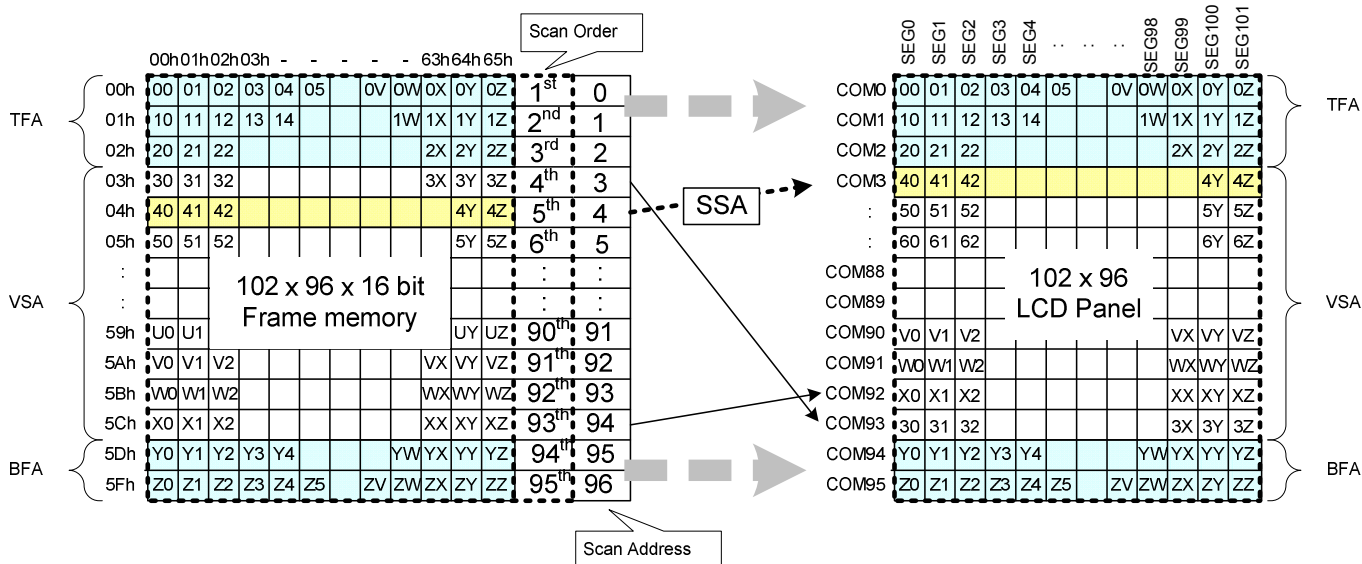


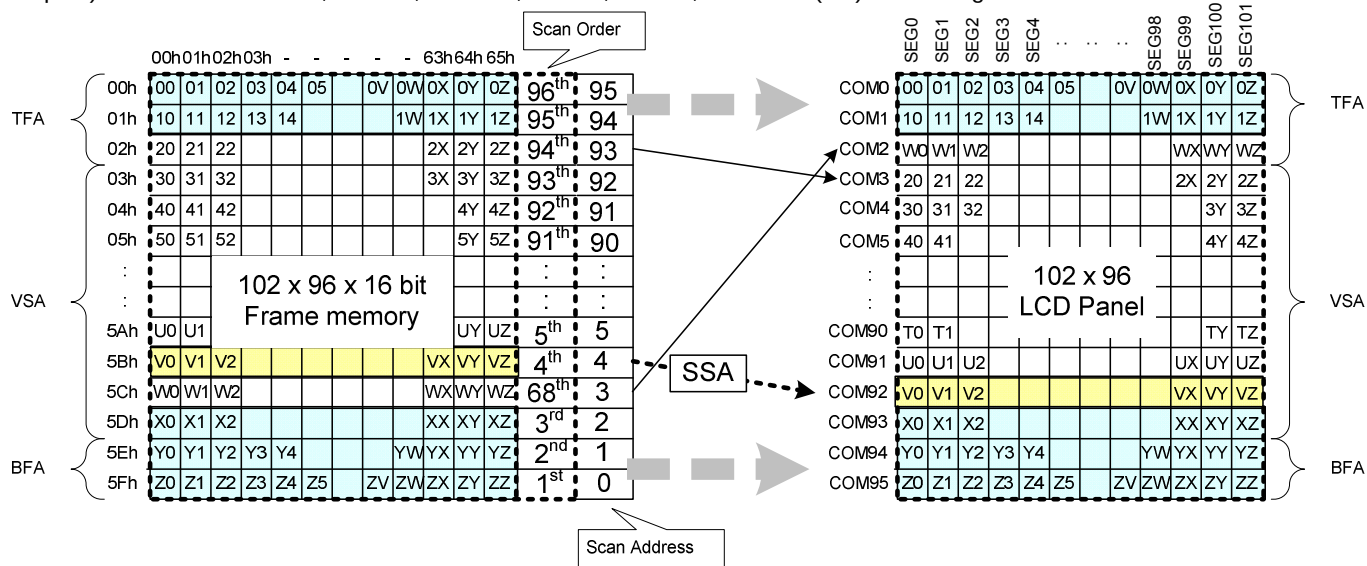
Figure 7.4 Rolling Scroll Definition

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) =96. In this case, 'rolling' scrolling is applied as shown below. All the memory contents will be used.

Example1) Panel size=102 x 96, TFA=3, VSA=91, BFA=2, SSA=4, MADCTR (ML) =0: Rolling Scroll



Example2) Panel size=102 x 96, TFA =3, VSA=91, BFA=2, SSA=4, MADCTR (ML) =1: Rolling Scroll



Vertical Scroll Example

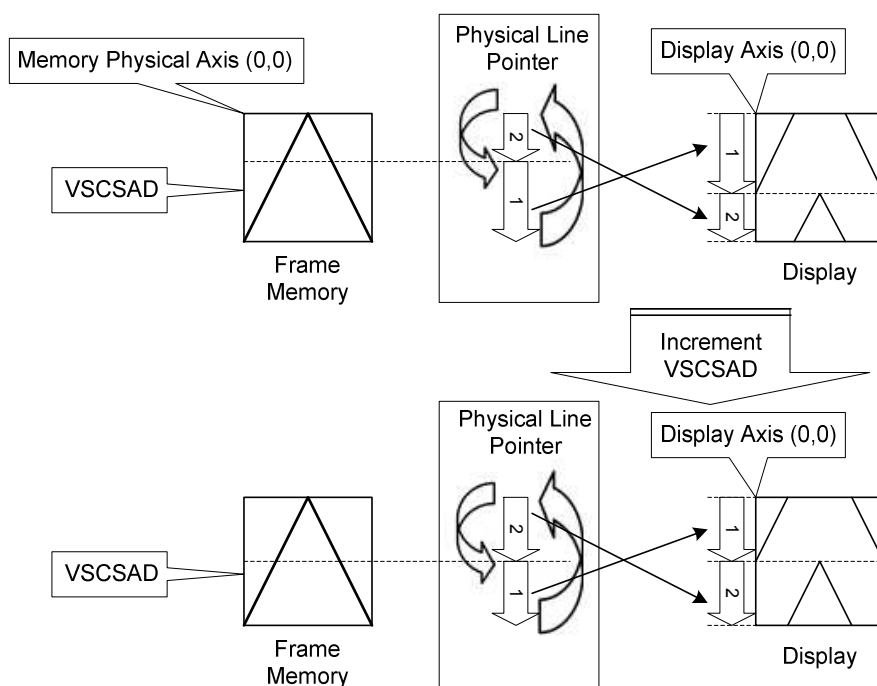
There are 2 types of vertical scrolling, which are determined by the commands "Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

Case 1: $TFA + VSA + BFA < 96$

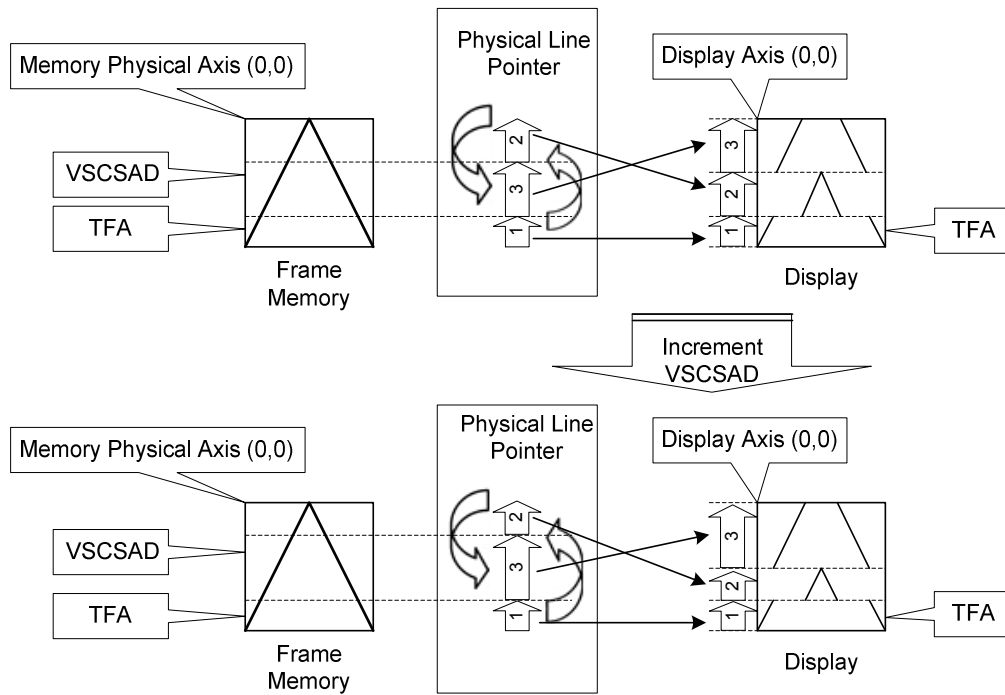
N/A. Do not set $TFA + VSA + BFA < 96$. In that case, unexpected picture will be shown.

Case 2: $TFA + VSA + BFA = 96$ (Rolling Scrolling)

Example1) When MADCTR parameter ML="0", $TFA=0$, $VSA=96$, $BFA=0$ and $VSCSAD=40$.



Example2) When MADCTR parameter ML="1", TFA=10, VSA=86, BFA=0 and VSCSAD=30.



7.4 Gray-Scale Display

ST7625 incorporates a 4FRC & 31 PWM function circuit to display a 64 gray-scale display.

7.5 Oscillation circuit

ST7625 has a built-in an oscillator circuit. It provides internal clock without using external resistor. This oscillator signal is used in the voltage converter and display timing generation circuit.

7.6 Display Timing Generator Circuit

This circuit generates some signals for displaying LCD. The display clock, which is generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 96-bits display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M), which enables the LCD driver to make an AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 7.5.

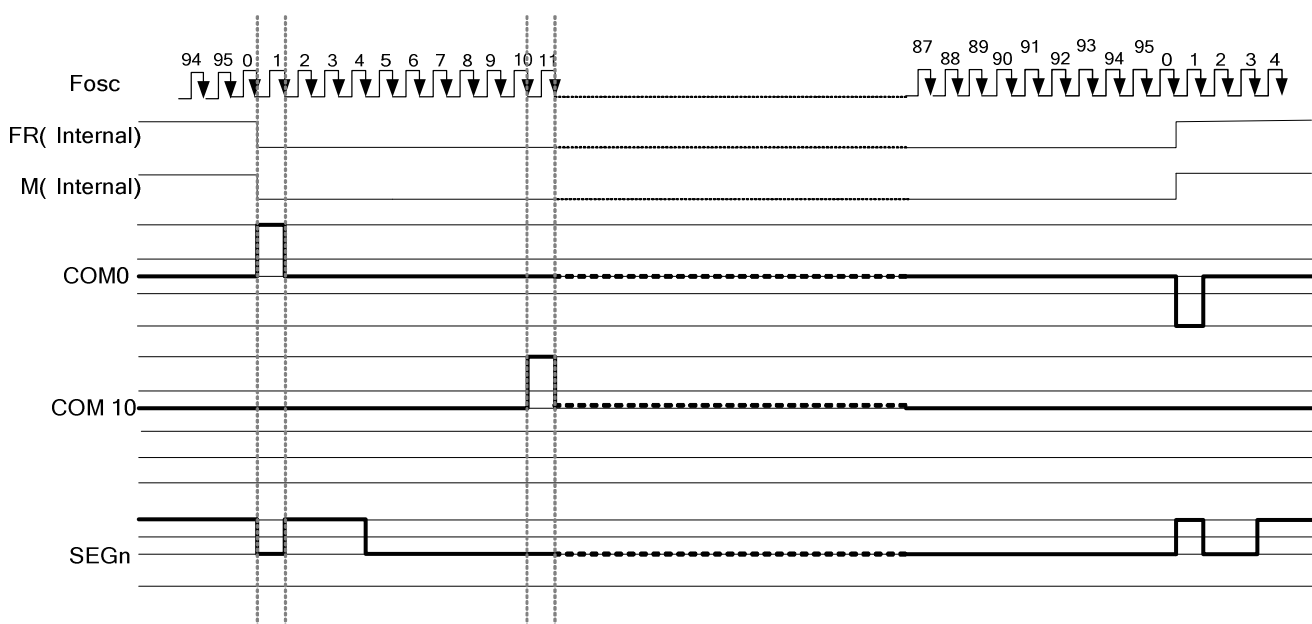


Figure 7.5 2-frame AC Driving Waveform (Duty Ratio: 1/96)

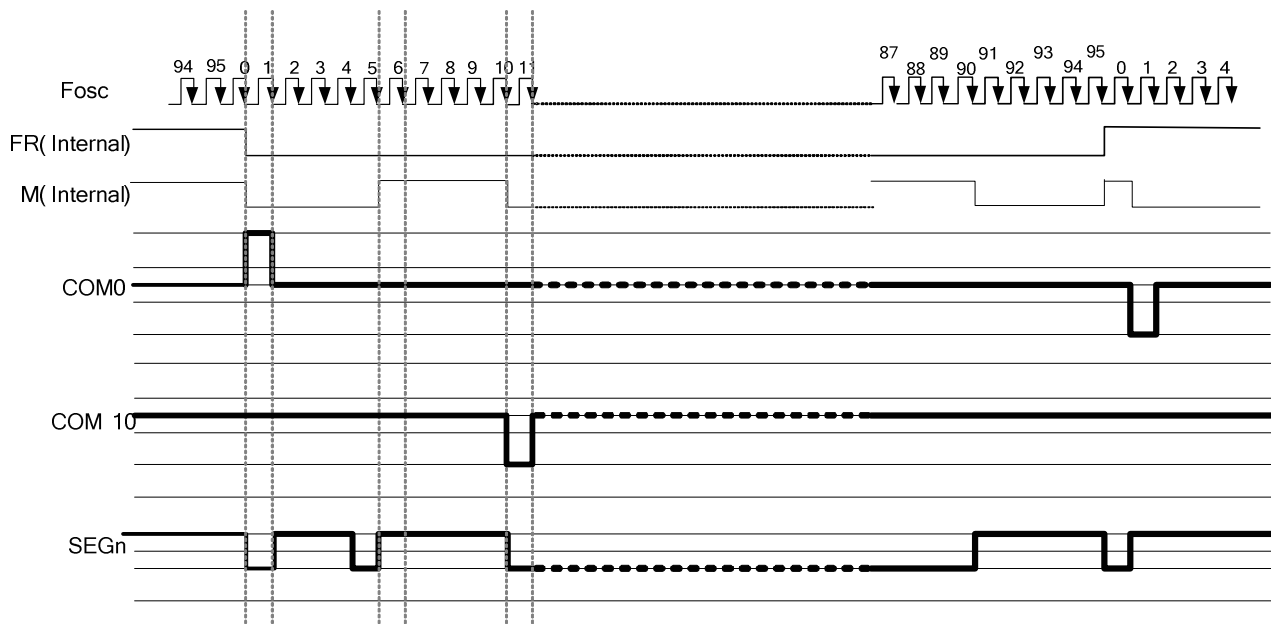


Figure 7.6 N-Line Inversion Driving Waveform (N=10, Duty Ratio=1/96)

7.7 POWER LEVEL DEFINITION

7.7.1 Power ON/OFF SEQUENCE

Definition: VDDI=VDD & VDD1; VDDA=VDD2, VDD3, VDD4 & VDD5

During power off, if LCD is in the Sleep Out mode, VDDA and VDDI must be powered down minimum 120m sec after /RST has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDDA can be powered down minimum 0msec after /RST has been released.

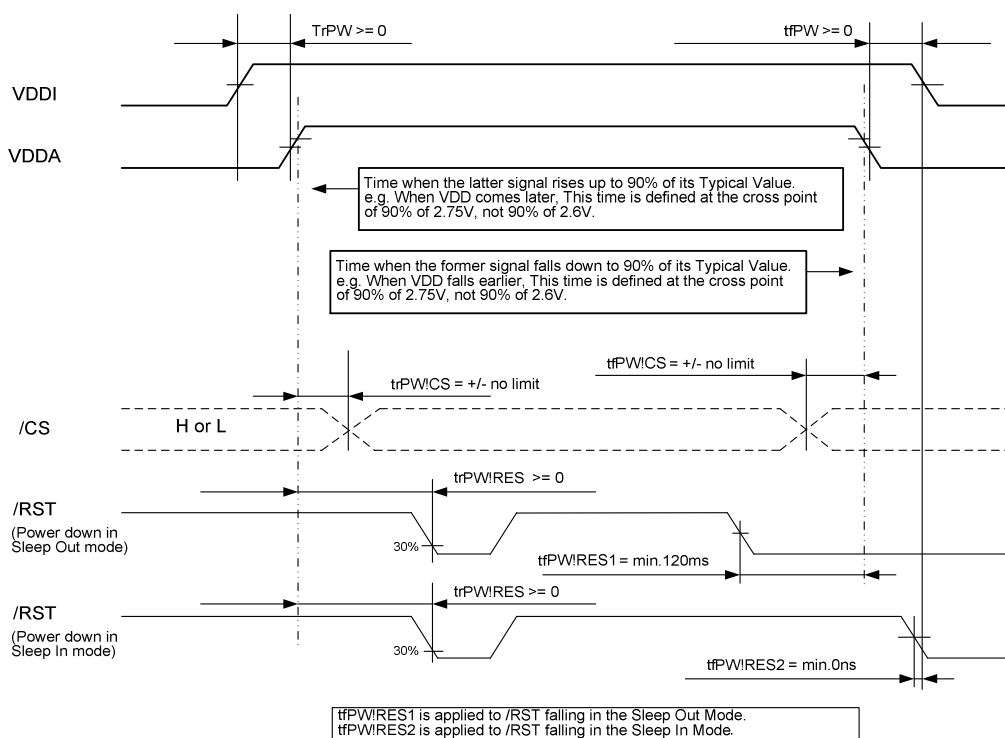
/CS can be applied at any timing or can be permanently grounded. /RST has priority over /CS.

If /RST line is not held stable by host during Power On Sequence as defined in Sections case1 and case2, then it will be necessary to apply a Hardware Reset (/RST) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below:

/RST line is held High or Unstable by Host at Power On

If /RST line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDDA and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

7.7.2 Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out:

In this mode, the display is able to show maximum 65K colors.

2. Partial Mode On, Idle Mode Off, Sleep Out:

In this mode part of the display is used with maximum 65K colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out:

In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out:

In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode:

In this mode, the DC:DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with Digital VDD power supply. Contents of the memory are safe.

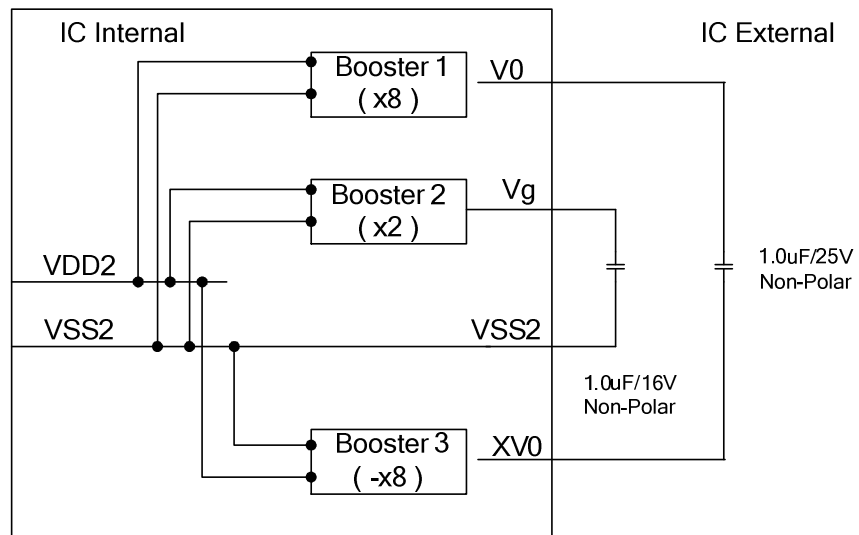
6. Power Off Mode:

In this mode, both Analog VDD and Digital VDD are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

7.8 Liquid Crystal Driver Power Circuit

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction.



DC/DC Booster Block Diagram

7.8.1 Voltage Regulator Circuits

There is a built-in voltage regulator circuits in ST7625 for generating V0. After internal voltage is regulated by voltage regulator circuit, V0 is generated. Detail explanation of V0 set is listed below:

7.8.1.1 SET V0 (Temperature = 24°C)

$$V0 = a + \{Vop[8:0] + VopOffset[8:0] + (EV[6:0] - 3Fh)\} \times b \quad (V)$$

Example:

Vop[8:0] = 011010010

VopOffset[8:0] = 000000011

EV[6:0] = 0111111

$$V0 = 3.6 + \{210 + 3 + (63 - 63)\} \times 0.04 = 12.12 \text{ (V)}$$

- a is a fixed constant value (see Table 7.8.1).
- b is a fixed constant value (see Table 7.8.1).
- Vop [8:0] is the programmed VOP value. The programming range for Vop[8:0] is 5 to 410 (019Ahex).
- The range of contrast is 128 steps for fine tuning VOP.

Table 7.8.1

SYMBOL	VALUE	UNIT
a	3.6	V
b	0.04	V

The Vop [8:0] value must be in the V0 programming range as given in Figure 7.7. Evaluating V0 equation, values outside the programming range indicated in many result. V0 range is 3.6 ~18.

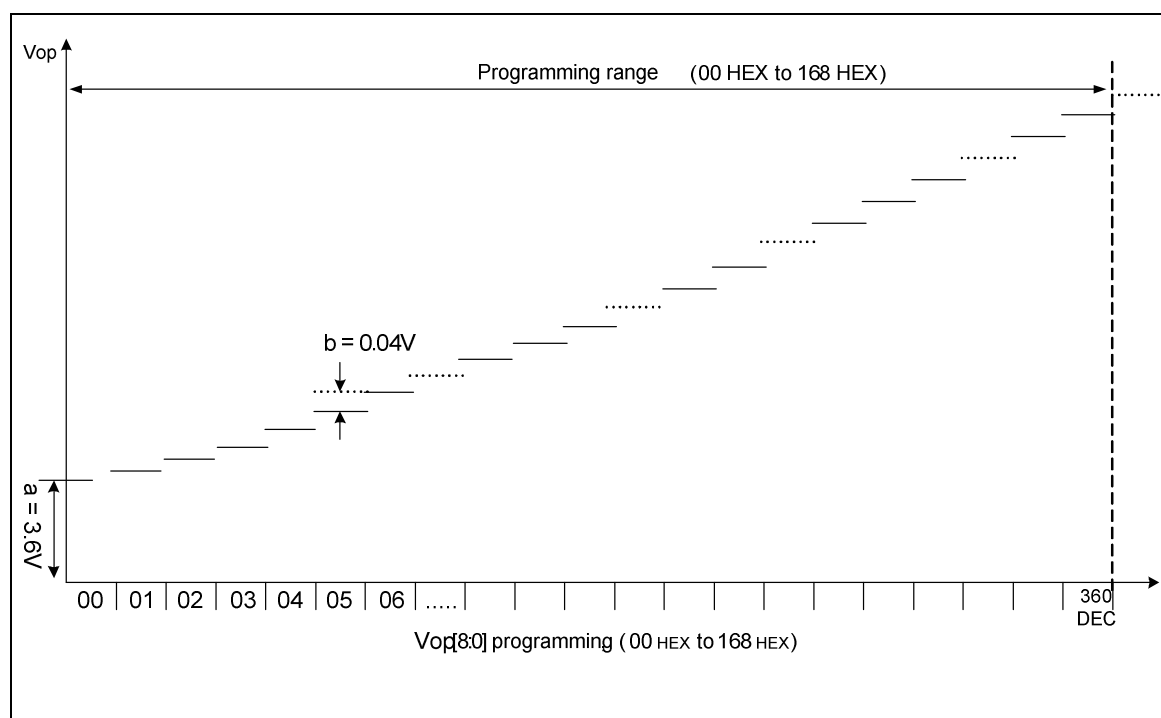


Figure 7.7 V0 programming range

As the programming range for the internally generated V0 voltage is above the limited V0 (18V), users have to ensure while setting the VPR register and selecting the temperature compensation that under all conditions and including all tolerances that the V0 voltage remains below 18V.

7.8.1.2 SET V0 with temperature compensation (Temperature $\neq 24^{\circ}\text{C}$)

There are 16-line slope in each temperature steps and customer can select one line slope of temperature compensation coefficient for each temperature step. Each temperature step is 8°C . Please see Figure 7.8 as below.

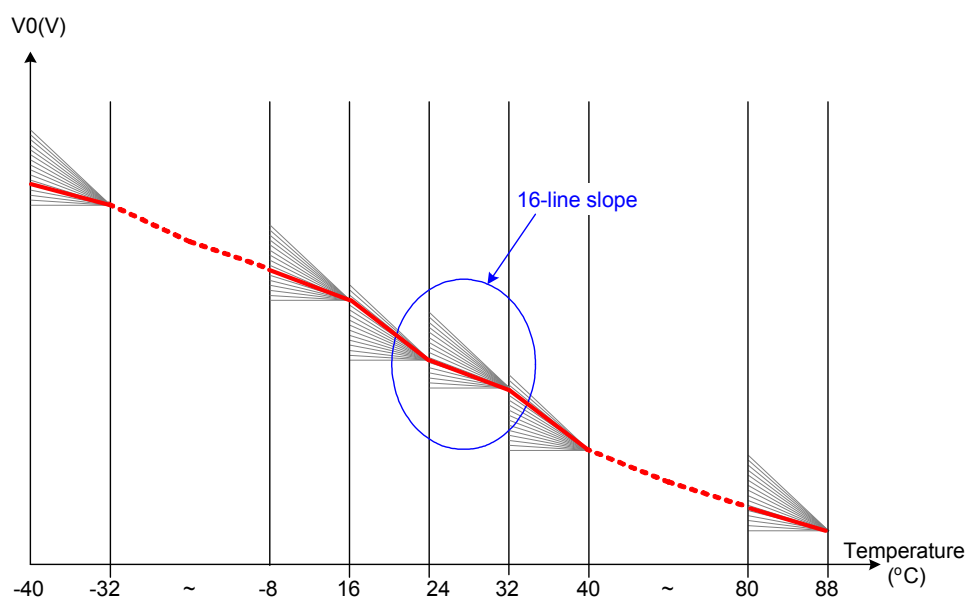
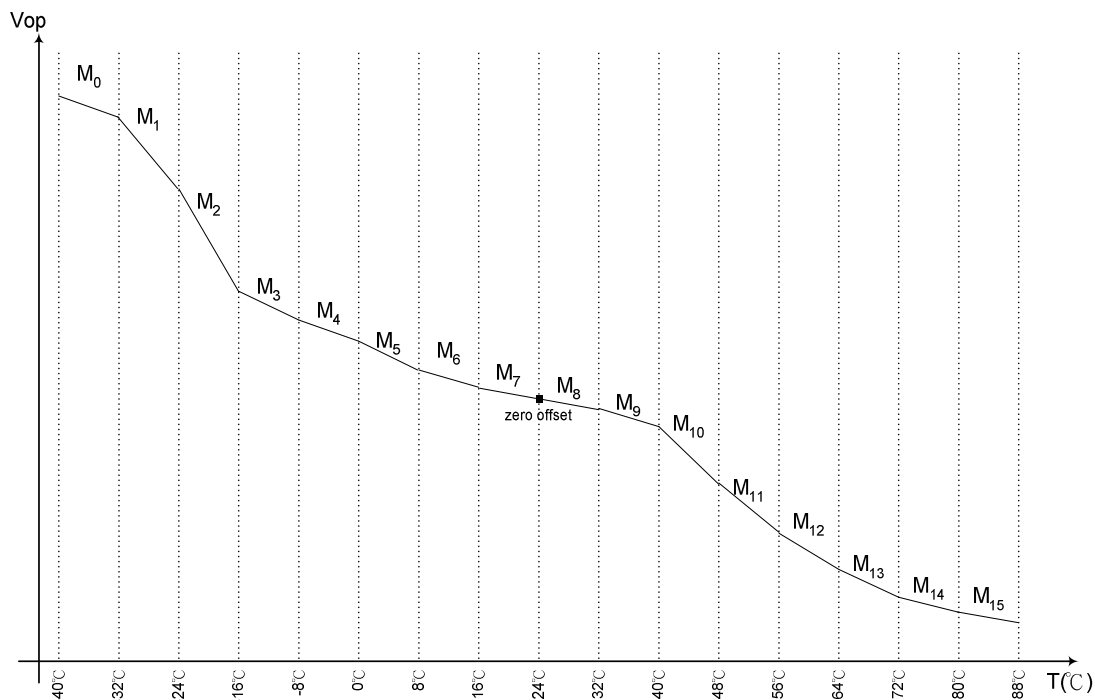


Figure 7.8

In command TEMPSEL each MTx, where x=0, 1, 2,..., E, F, has a value between 0 and 15. MTx = 0 results in 0V increment on V0, MTx = 1 results in Mx=5mV increment, ..., MTx = 15 results in Mx=15x5mV=75mV increment. Note that each MTx individually corresponds to a temperature interval; The relations between Mx and V0 quantity due to temperature V0(T) are described in the equations shown as follows:

Temperature range	Equation V0(V) at temperature=T°C
$-40^{\circ}\text{C} \leq T < -32^{\circ}\text{C}$	$V0(T) = V0(T_{24}) + (-32-T) \cdot M0 + (M1 + M2 + M3 + M4 + M5 + M6 + M7) \cdot 8$
$-32^{\circ}\text{C} \leq T < -24^{\circ}\text{C}$	$V0(T) = V0(T_{24}) + (-24-T) \cdot M1 + (M2 + M3 + M4 + M5 + M6 + M7) \cdot 8$
$-24^{\circ}\text{C} \leq T < -16^{\circ}\text{C}$	$V0(T) = V0(T_{24}) + (-16-T) \cdot M2 + (M3 + M4 + M5 + M6 + M7) \cdot 8$
$-16^{\circ}\text{C} \leq T < -8^{\circ}\text{C}$	$V0(T) = V0(T_{24}) + (-8-T) \cdot M3 + (M4 + M5 + M6 + M7) \cdot 8$
$-8^{\circ}\text{C} \leq T < 0^{\circ}\text{C}$	$V0(T) = V0(T_{24}) + (0-T) \cdot M4 + (M5 + M6 + M7) \cdot 8$
$0^{\circ}\text{C} \leq T < 8^{\circ}\text{C}$	$V0(T) = V0(T_{24}) + (8-T) \cdot M5 + (M6 + M7) \cdot 8$
$8^{\circ}\text{C} \leq T < 16^{\circ}\text{C}$	$V0(T) = V0(T_{24}) + (16-T) \cdot M6 + M7 \cdot 8$
$16^{\circ}\text{C} \leq T < 24^{\circ}\text{C}$	$V0(T) = V0(T_{24}) + (24-T) \cdot M7$
$24^{\circ}\text{C} \leq T < 32^{\circ}\text{C}$	$V0(T) = V0(T_{24}) - (T-24) \cdot M8$
$32^{\circ}\text{C} \leq T < 40^{\circ}\text{C}$	$V0(T) = V0(T_{24}) - (T-32) \cdot M9 - M8 \cdot 8$
$40^{\circ}\text{C} \leq T < 48^{\circ}\text{C}$	$V0(T) = V0(T_{24}) - (T-40) \cdot M10 - (M9 + M8) \cdot 8$
$48^{\circ}\text{C} \leq T < 56^{\circ}\text{C}$	$V0(T) = V0(T_{24}) - (T-48) \cdot M11 - (M10 + M9 + M8) \cdot 8$
$56^{\circ}\text{C} \leq T < 64^{\circ}\text{C}$	$V0(T) = V0(T_{24}) - (T-56) \cdot M12 - (M11 + M10 + M9 + M8) \cdot 8$
$64^{\circ}\text{C} \leq T < 72^{\circ}\text{C}$	$V0(T) = V0(T_{24}) - (T-64) \cdot M13 - (M12 + M11 + M10 + M9 + M8) \cdot 8$
$72^{\circ}\text{C} \leq T < 80^{\circ}\text{C}$	$V0(T) = V0(T_{24}) - (T-72) \cdot M14 - (M13 + M12 + M11 + M10 + M9 + M8) \cdot 8$
$80^{\circ}\text{C} \leq T < 88^{\circ}\text{C}$	$V0(T) = V0(T_{24}) - (T-80) \cdot M15 - (M14 + M13 + M12 + M11 + M10 + M9 + M8) \cdot 8$

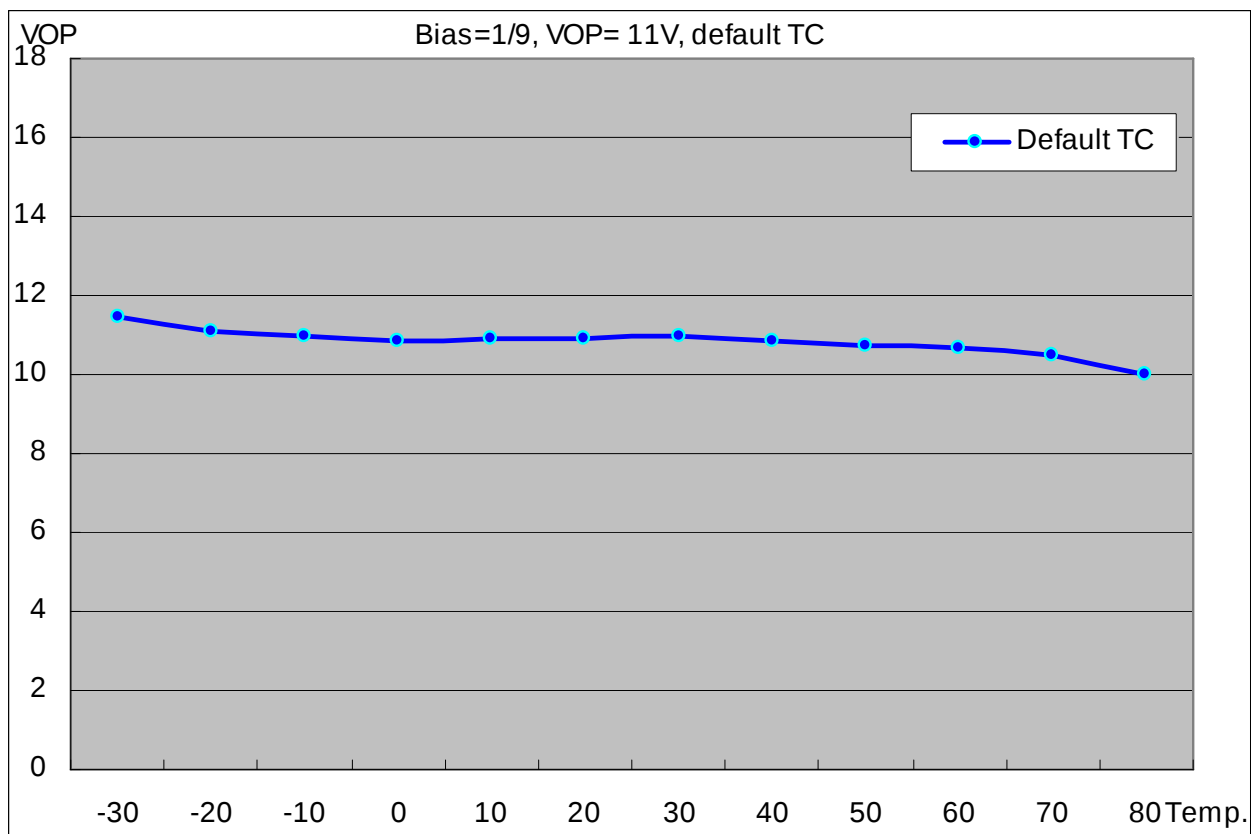


Note:

Please make sure to avoid any kind of heating source closing to ST7625 such as back light, to prevent the Vop value is not as anticipated because of temperature compensate circuit functioning.

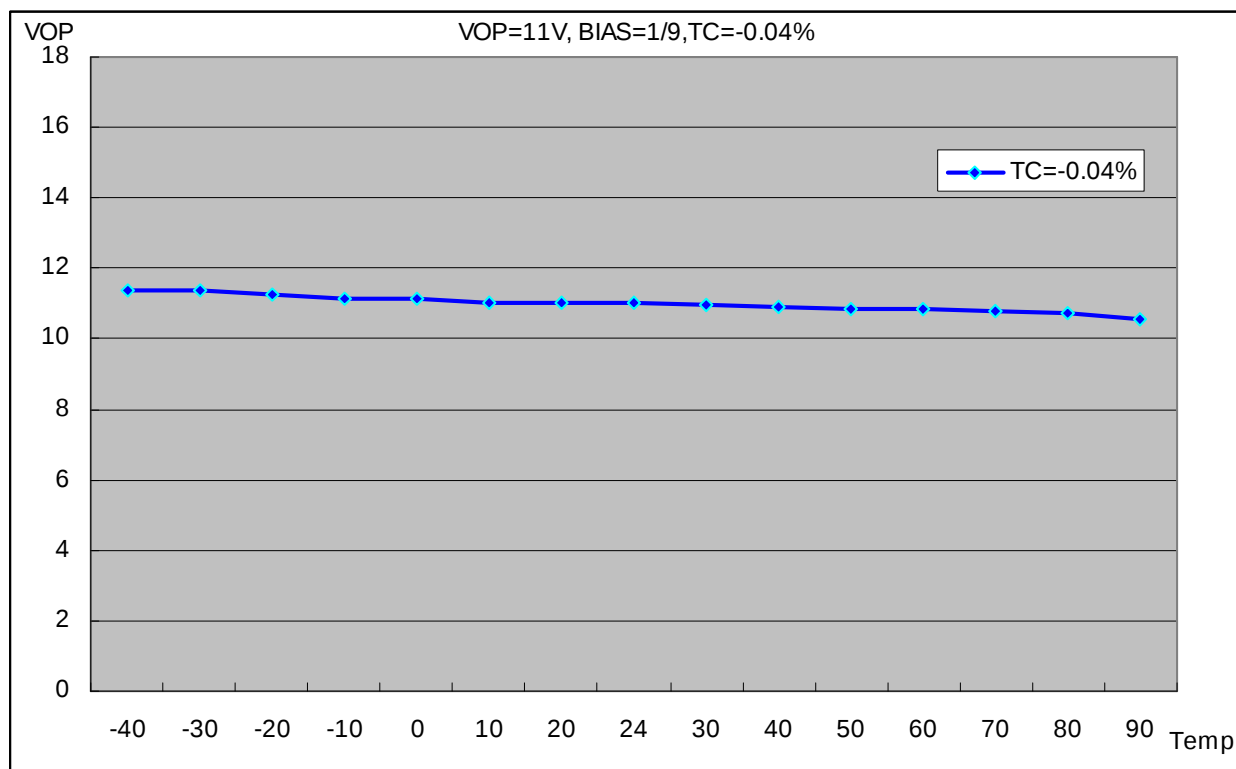
Setting example for default TC curve

Command	
0xF4	
Data	
1 st : 0xFF	2 nd : 0x36
3 rd : 0x04	4 th : 0x00
5 th : 0x33	6 th : 0x42
7 th : 0xC4	8 th : 0x59



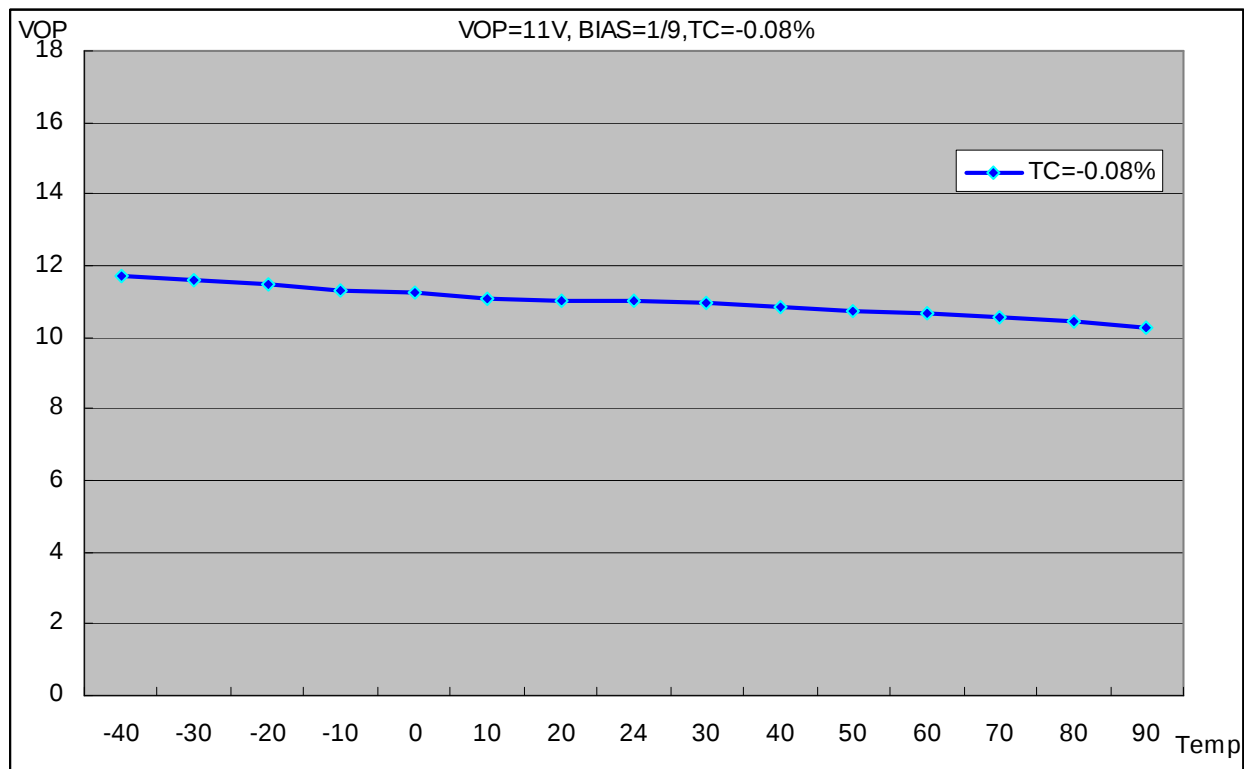
Setting example for TC curve=-0.04%

Command	
0xF4	
Data	
1 st : 0x11	2 nd : 0x11
3 rd : 0x11	4 th : 0x11
5 th : 0x11	6 th : 0x11
7 th : 0x11	8 th : 0x11



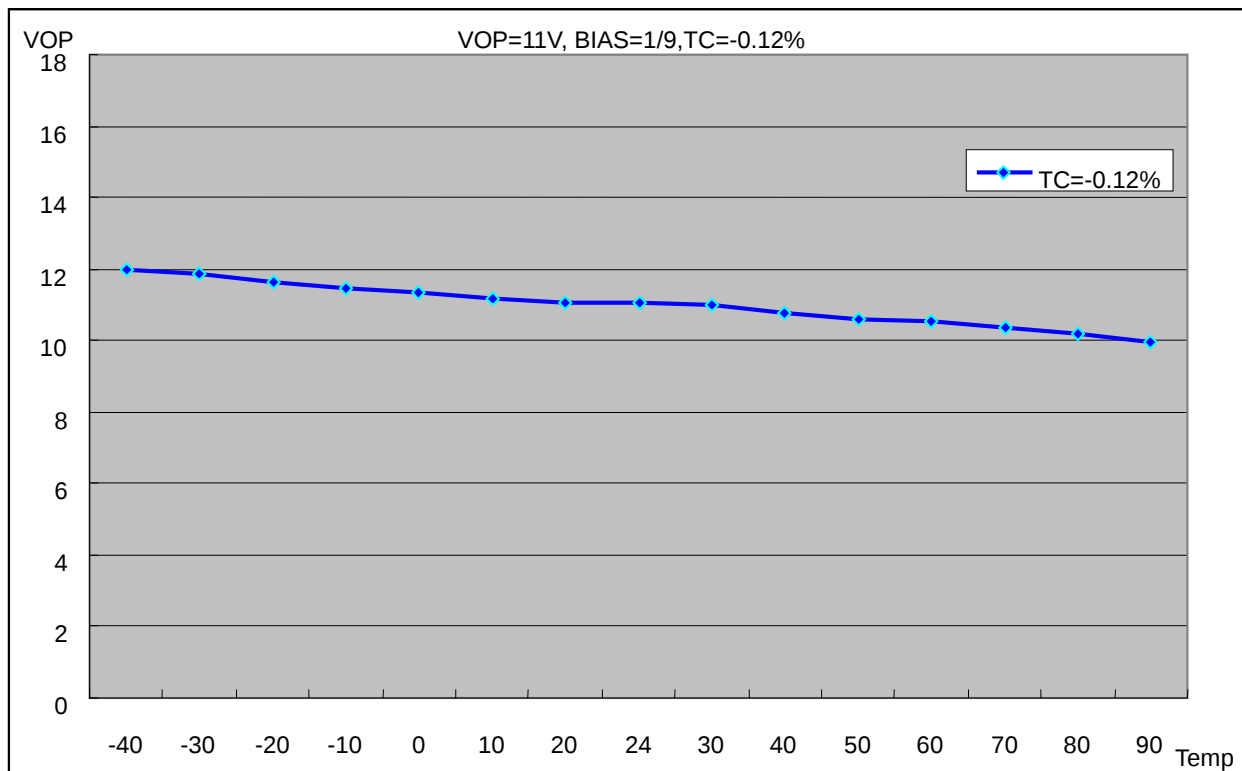
Setting example for TC curve=-0.08%

Command	
0xF4	
Data	
1 st : 0x22	2 nd : 0x22
3 rd : 0x22	4 th : 0x22
5 th : 0x22	6 th : 0x22
7 th : 0x22	8 th : 0x22



Setting example for TC curve = -0.12%

Command	
0xF4	
Data	
1 st : 0x33	2 nd : 0x33
3 rd : 0x33	4 th : 0x33
5 th : 0x33	6 th : 0x33
7 th : 0x33	8 th : 0x33



7.8.1.3 V0 fine tuning

ST7625 has 2 commands for fine tuning V0. These commands are VopOffsetInc and VopOffsetDec. When writing VopOffsetInc into IC for each time, V0 would increase 40mV; when writing VopOffsetDec into IC for each time, V0 would decrease 40mV.

Example:

Vop[8:0]=011010010

Vopoffset[8:0]=000000011

EV[6:0]=0111111

VopOffsetInc x2

→ $V0 = 3.6 + \{ 210 + 3 + (63 - 63) \} \times 0.04 + 0.04 \times 2 = 12.2 \text{ (V)}$

7.8.2 Voltage Follower Circuits

There is a built-in voltage follower circuits in ST7625 for generating Vg and Vm. These voltages are decided by bias ratio selection circuitry which is set by users with software code. The selection of 1/5 to 1/12 bias ratios can match the optimum display performance of LCD panel. Bias driving rule is listed below:

LCD bias	Vg	Vm
1/N bias	$(2/N) \times V0$	$(1/N) \times V0$

N=5 to 12

7.8.3 OTP Setting Flow

OTP Setting Flow

ST7625 provide the Write and Read function to write the Electronic Control value and Built-in resistance ratio into and read them from the built-in OTP. Using the Write and Read functions, you can store these values appropriate to each LCD panel. This function is very convenient for user in setting from some different panel's voltage. But using this function must attention the setting procedure. Please see the following diagram.

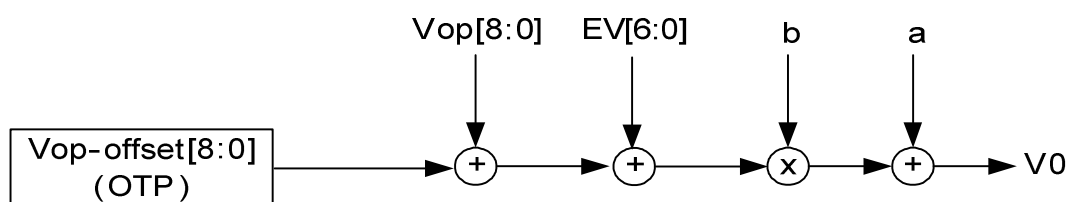


Figure 7.9 V0 value control for different modules by loading OTP offset

Note1: This setting flow is used for LCM assembler.

Note2: OTP shouldn't be written without preceding loading correctly from OTP to avoid some errors during IC operation.

Note3: When writing value to OTP, the voltage of VPP must be within 7.5V~7.75V; the current of Ivpp must be more than 4 mA.

Note4: If the OTP is exposed to a high temperature for hours, data in the memory cell may probably be lost before the data retention guarantee period. To retain data in the memory cell, keep the memory cell below 90 °C. The data retention guarantee period is specified including the retention period.

7.8.4 Frequency Temperature Gradient Compensation Coefficient

ST7625 will auto-switch frame rate on different temperature shown in Figure 7.10. TA, TB and TC are frame rate switching temperatures which can be defined by customer with command TMRNG. FA, FB, FC and FD are switched frame rate which also can be defined by customer with command FRMSEL. The frame rate range is from 37.5Hz to 170Hz.

When the temperature is in increasing state, frame rate changes to the higher step at TA/TB/TC+TH(°C). When the temperature is in decreasing state, frame rate changes to the lower step at TA/TB/TC. For example: TC=10°C and TH=5°C, FC switches to FD at 15°C but FD switches to FC at 10°C. Please take Figure 7.10 for reference.

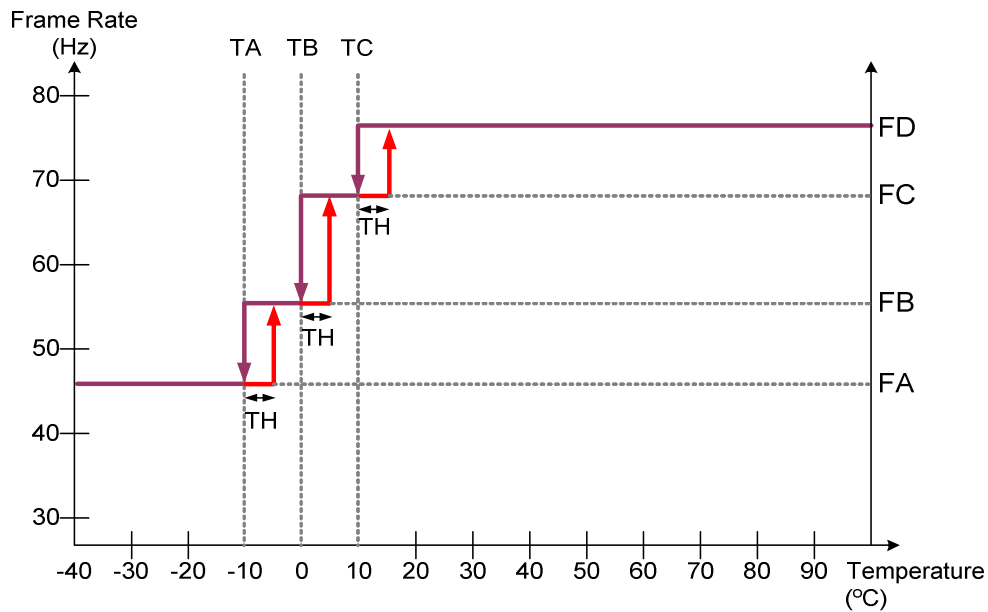


Figure 7.10

8. RESET value

Item	After Power On	After Software Reset	After Hardware Reset
Frame memory (RAM data)	Random	No Change	No Change
Sleep In/Out	In	In	In
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
All Pixel Off mode	Disable	Disable	Disable
All Pixel On mode	Disable	Disable	Disable
Contrast (EV)	3Fh	3Fh	3Fh
Display On/Off	Display Off	Display Off	Display Off
Column: Start Address (XS)	00h	00h	00h
Column: End Address (XE)	65h	65h	65h
Row: Start Address (YS)	00h	00h	00h
Row: End Address (YE)	5Fh	5Fh	5Fh
Partial: Start Address (PS)	00h	00h	00h
Partial: End Address (PE)	5Fh	5Fh	5Fh
Scroll: Top Fixed Area (TFA)	00h	00h	00h
Scroll: Scroll Area (VSA)	65h	65h	65h
Scroll: Bottom Fixed Area (BFA)	00h	00h	00h
Memory Data Access Control MY/MX/MV/ML/RGB)	0/0/0/0/0	No Change	0/0/0/0/0
Scroll Start Address (SSA)	00h	00h	00h
Idle Mode On/Off	Off	Off	Off
Interface Color Pixel Format (P)	05h (16Bit/Pixel)	No change	05h (16Bit/Pixel)
Drive Duty	5Fh	5Fh	5Fh
First Common	00h	00h	00h
FOSC Divider	No division	No division	No division
Common scan direction	0→47, 48→95	0→47, 48→95	0→47, 48→95
Vop	0D2h	0D2h	0D2h
Bias	1/9 Bias	1/9 Bias	1/9 Bias
Booster setting	8x	8x	8x
Booster Efficiency	01	01	01
Vg source	From 2VDD2	From 2VDD2	From 2VDD2
EPCTIN	0	0	0
OTP selection	Disable	Disable	Disable
Frame Frequency in Normal Color (FA/FB/FC/FD)	46Hz/61.5Hz/72/Hz/77Hz	46Hz/61.5Hz/72/Hz/77Hz	46Hz/61.5Hz/72/Hz/77Hz
Temperature Range (TA/TB/TC)	-10℃/0℃/10℃	-10℃/0℃/10℃	-10℃/0℃/10℃
Temperature Hysteresis (TH for frame rate)	5℃	5℃	5℃

9. INSTRUCTIONS

9.1 INSTRUCTION table

Command Table-1														
Hex	Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Ref
(00h)	NOP	0	1	0	0	0	0	0	0	0	0	0	No Operation	9.1.1
(01h)	SWRESET	0	1	0	0	0	0	0	0	0	0	1	Software reset	9.1.2
(09h)	RDDST	0	1	0	0	0	0	0	1	0	0	1	Read Display Status	9.1.3
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	(D31-D24)	
-		1	0	1	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16	(D23-D16)	
-		1	0	1	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	(D15-D8)	
-		1	0	1	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	(D7-D0)	
(10h)	SLPIN	0	1	0	0	0	0	1	0	0	0	0	Sleep in & booster off	9.1.4
(11h)	SLPOUT	0	1	0	0	0	0	1	0	0	0	1	Sleep out & booster on	9.1.5
(12h)	PTLON	0	1	0	0	0	0	1	0	0	1	0	Partial mode on	9.1.6
(13h)	NORON	0	1	0	0	0	0	1	0	0	1	1	Partial off (Normal)	9.1.7
(20h)	INVOFF	0	1	0	0	0	1	0	0	0	0	0	Display inversion off (normal)	9.1.8
(21h)	INVON	0	1	0	0	0	1	0	0	0	0	1	Display inversion on	9.1.9
(22h)	APOFF	0	1	0	0	0	1	0	0	0	1	0	All pixel off (Only for test purpose)	9.1.10
(23h)	APON	0	1	0	0	0	1	0	0	0	1	1	All pixel on (Only for test purpose)	9.1.11
(25h)	WRCNTR	0	1	0	0	0	1	0	0	1	0	1	Write contrast	9.1.12
-		1	1	0	0	EV6	EV5	EV4	EV3	EV2	EV1	EV0	EV = 0 to 127	
(28h)	DISPOFF	0	1	0	0	0	1	0	1	0	0	0	Display off	9.1.13
(29h)	DISPON	0	1	0	0	0	1	0	1	0	0	1	Display on	9.1.14
(2Ah)	CASET	0	1	0	0	0	1	0	1	0	1	0	Column address set	9.1.15
		1	1	0	0	XS6	XS5	XS4	XS3	XS2	XS1	XS0	X_ADR start: $0 \leq XS \leq 65h$	
		1	1	0	0	XE6	XE5	XE4	XE3	XE2	XE1	XE0	X_ADR end: $XS \leq XE \leq 65h$	
(2Bh)	RASET	0	1	0	0	0	1	0	1	0	1	1	Row address set	9.1.16
		1	1	0	0	YS6	YS5	YS4	YS3	YS2	YS1	YS0	Y_ADR start: $0 \leq YS \leq 5Fh$	
		1	1	0	0	YE6	YE5	YE4	YE3	YE2	YE1	YE0	Y_ADR end: $YS \leq YE \leq 5Fh$	
(2Ch)	RAMWR	0	1	0	0	0	1	0	1	1	0	0	Memory write	9.1.17
		1	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data	

ST7625

(2Eh)	RAMRD	0	1	0	0	0	1	0	1	1	1	0	Memory Read	9.1.18
		1	1	0	-	-	-	-	-	-	-	-	Dummy read	
		1	1	0	D7	D6	D5	D4	D3	D2	D1	D0		
(30h)	PTLAR	0	1	0	0	0	1	1	0	0	0	0	Partial Area	9.1.19
		1	1	0	--	PS6	PS5	PS4	PS3	PS2	PS1	PS0		
		1	1	0	--	PE6	PE5	PE4	PE3	PE2	PE1	PE0		
(33h)	SCRLAR	0	1	0	0	0	1	1	0	0	1	1	Scroll Area	9.1.20
-		1	1	0	0	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	TFA= 0~95	
-		1	1	0	0	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	VSA= 0~95	
-		1	1	0	0	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	BFA= 0~95	
(36h)	MADCTR	0	1	0	0	0	1	1	0	1	1	0	Memory data access control	9.1.21
-		1	1	0	MY	MX	MV	ML	RGB	-	-	-	-	
(37h)	VSCSAD	0	1	0	0	0	1	1	0	1	1	1	Scroll start address of RAM	9.1.22
		1	1	0	0	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	SSA = 0~95	
(38h)	IDMOFF	0	1	0	0	0	1	1	1	0	0	0	Idle mode off	9.1.23
(39h)	IDMON	0	1	0	0	0	1	1	1	0	0	1	Idle mode on	9.1.24
(3Ah)	COLMOD	0	1	0	0	0	1	1	1	0	1	0	Interface pixel format	9.1.25
-		1	1	0	-	-	-	-	-	P2	P1	P0	Interface format	

Note 1: Commands 10H, 12H, 13H, 20H, 21H, 25H, 28H, 29H, 30H, 36H (Bit ML only), 38H and 39H are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects.

During Sleep In mode, these commands are updated immediately.

Read status (09H) is updated immediately both in Sleep In mode and Sleep Out mode.

Command Table-2

Hex	Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Ref
(B0h)	DutySet	0	1	0	1	0	1	1	0	0	0	0	Display Duty setting	9.1.26
		1	1	0	0	Du6	Du5	Du4	Du3	Du2	Du1	Du0		
(B1h)	FirstCom	0	1	0	1	0	1	1	0	0	0	1	First Com. Page address	9.1.27
		1	1	0	--	F6	F5	F4	F3	F2	F1	F0		
(B3h)	OscDiv	0	1	0	1	0	1	1	0	0	1	1	FOSC divider	9.1.28
		1	1	0	-	-	-	-	-	-	CLD1	CLD0		
(B5h)	NLInvSet	0	1	0	1	0	1	1	0	1	0	1	N-line control	9.1.29
		1	1	0	M	N6	N5	N4	N3	N2	N1	N0		
(B7h)	SEGScanDir	0	1	0	1	0	1	1	0	1	1	1	Seg Scan Direction for Glass layout	9.1.30
		1	1	0	0	SMX	0	0	SBGR	0	0	0		
(B8h)	RmwIn	0	1	0	1	0	1	1	1	0	0	0	read modify write control IN	9.1.31
(B9h)	RmwOut	0	1	0	1	0	1	1	1	0	0	1	read modify write control Out	9.1.32
(C0h)	VopSet	0	1	0	1	1	0	0	0	0	0	0	Vop setting	9.1.33
		1	1	0	Vop7	Vop6	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0		
		1	1	0	-	-	-	-	-	-	-	Vop8		
(C1h)	VopOfsetInc	0	1	0	1	1	0	0	0	0	0	1	+40mv/setp	9.1.34
(C2h)	VopOfsetDec	0	1	0	1	1	0	0	0	0	1	0	-40mv/setp	9.1.35
(C3h)	BiasSel	0	1	0	1	1	0	0	0	0	1	1	Bias selection	9.1.36
		1	1	0	-	-	-	-	-	Bias2	Bias1	Bias0		
(C4h)	BstBmpXSel	0	1	0	1	1	0	0	0	1	0	0	Booster setting	9.1.37
		1	1	0	-	-	-	-	-	BST2	BST 1	BST0		
(C5h)	BstEffSel	0	1	0	1	1	0	0	0	1	0	1	Booster efficiency selection	9.1.38
		1	1	0	-	-	-	-	-	-	BTF1	BTF0		
(C7h)	VopOffset	0	1	0	1	1	0	0	0	1	1	1	Vop offset fuse bit adjust	9.1.39
		1	1	0	VOS7	VOS6	VOS5	VOS4	VOS3	VOS2	VOS1	VOS0		
		1	1	0	-	-	-	-	-	-	-	VOS8		
(CBh)	VgSorSel	0	1	0	1	1	0	0	1	0	1	1	FVg with Booster x2 control	9.1.40
		1	1	0	-	-	-	-	-	-	-	2BT0		

(D0h)	ANASET	0	1	0	1	1	0	1	0	0	0	0	Analog circuit setting	9.1.41
		1	1	0	0	0	0	1	1	1	0	1		
(D7h)	AutoLoadSet	0	1	0	1	1	0	1	0	1	1	1	Mask ROM data auto re-load control	9.1.42
		1	1	0	0	0	0	ARD	1	1	1	1		
(DEh)	RDTstStatus	0	1	0	1	1	0	1	1	1	1	0	Read IC status	9.1.43
		1	0	1	-	-	-	-	-	-	-	-	Dummy Read	
		1	0	1	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	OTP read control	
(E0h)	EPCTIN	0	1	0	1	1	1	0	0	0	0	0	Control OTP WR/RD	9.1.44
		1	1	0	0	0	EWR	0	0	0	0	0	OTP ROM Write Control	
(E1h)	EPCTOUT	0	1	0	1	1	1	0	0	0	0	1	OTP control cancel	9.1.45
(E2h)	EPMWR	0	1	0	1	1	1	0	0	0	1	0	Write to OTP	9.1.46
(E3h)	EPMRD	0	1	0	1	1	1	0	0	0	1	1	Read from OTP	9.1.47
(E4h)	OTPSEL	0	1	0	1	1	1	0	0	1	0	0	Select OTP	9.1.48
		1	1	0	MS1	MS0	0	1	1	0	0	0		
(E5h)	ROMSET	0	1	0	1	1	1	0	0	1	0	1	Programmable rom setting	9.1.49
		1	1	0	0	0	0	0	1	0	0	1		
(EBh)	HPMSET	0	1	0	1	1	1	0	1	0	1	1	High power mode setting	9.1.50
		1	1	0	0	0	0	0	0	0	0	1		
		1	1	0	0	0	0	0	0	0	0	0		
(F0h)	FRMSEL	0	1	0	1	1	1	1	0	0	0	0	Frame Freq. in Temp range A,B,C and D	9.1.51
		1	1	0	-	-	-	DIVA	FA3	FA2	FA1	FA0		
		1	1	0	-	-	-	DIVB	FB3	FB2	FB1	FB0		
		1	1	0	-	-	-	DIVC	FC3	FC2	FC1	FC0		
		1	1	0	-	-	-	DIVD	FD3	FD2	FD1	FD0		
(F1h)	FRM8SEL	0	1	0	1	1	1	1	0	0	0	1	Frame Freq. in Temp range A,B,C and D (idle)	9.1.52
		1	1	0	-	-	-	F8A4	F8A3	F8A2	F8A1	F8A0		
		1	1	0	-	-	-	F8B4	F8B3	F8B2	F8B1	F8B0		
		1	1	0	-	-	-	F8C4	F8C3	F8C2	F8C1	F8C0		
		1	1	0	-	-	-	F8D4	F8D3	F8D2	F8D1	F8D0		
(F2h)	TMPRNG	0	1	0	1	1	1	1	0	0	1	0	Temp range A,B and C	9.1.53
		1	1	0	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0		
		1	1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0		
		1	1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0		

(F3h)	TMPHYS	0	1	0	1	1	1	1	0	0	1	1	Hysteresis value set	9.1.54
		1	1	0	-	-	-	-	TH3	TH2	TH1	TH0		
(F4h)	TEMPSEL	0	1	0	1	1	1	1	0	1	0	0	TEMPSEL	9.1.55
		1	1	0	MT13	MT12	MT11	MT10	MT03	MT02	MT01	MT00		
		1	1	0	MT33	MT32	MT31	MT30	MT23	MT22	MT21	MT20		
		1	1	0	MT53	MT52	MT51	MT50	MT43	MT42	MT41	MT40		
		1	1	0	MT73	MT72	MT71	MT70	MT63	MT62	MT61	MT60		
		1	1	0	MT93	MT92	MT91	MT90	MT83	MT82	MT81	MT80		
		1	1	0	MTB3	MTB2	MTB1	MTB0	MTA3	MTA2	MTA1	MTA0		
		1	1	0	MTD3	MTD2	MTD1	MTD0	MTC3	MTC2	MTC1	MTC0		
		1	1	0	MTF3	MTF2	MTF1	MTF0	MTE3	MTE2	MTE1	MTE0		
(F7h)	THYS	0	1	0	1	1	1	1	0	1	1	1	Temperature detection threshold	9.1.56
		1	1	0	THYS 7	THYS 6	THYS 5	THYS 4	THYS 3	THYS 2	THYS 1	THYS 0		
(F9h)	Frame Set	0	1	0	1	1	1	1	1	0	0	1	Set Frame1 RGB value	9.1.57
		1	1	0	-	-	-	P14	P13	P12	P11	P10		
		1	1	0	-	-	-	P24	P23	P22	P21	P20		
		:	:	:	:	:	:	:	:	:	:	:		
		1	1	0	-	-	-	P154	P153	P152	P151	P150		
		1	1	0	-	-	-	P164	P163	P162	P161	P160		

9.1.1 NOP(00H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NOP	0	1	0	0	0	0	0	0	0	0	0	(00h)
Parameter	No Parameter											

Description	This command is empty command. It does not have effect on the display module. However it can be used to terminate RAM data write as described in RAMWR (Memory Write) and parameter write commands.	
Restriction	-	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	N/A
	S/W Reset	N/A
	H/W Reset	N/A
Flow Chart	-	

9.1.2 SWRESET: Software Reset (01H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SWRESET	0	1	0	0	0	0	0	0	0	0	1	(01h)
Parameter	No Parameter											

Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values and all segment & common outputs are set to Vm (display off: blank display). (See default tables in each command description) Note: The Frame Memory contents are not affected by this command.													
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier's factory default values to the registers during 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command. Software Reset command cannot be sent during Sleep Out sequence.													
Register Availability	<table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table><tr><td>Status</td><td>Default Value</td></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table>		Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A				
Status	Default Value													
Power On Sequence	N/A													
S/W Reset	N/A													
H/W Reset	N/A													
Flow Chart	SWRESET Display whole blank screen Set Commands to S/W Default Value Sleep In Mode Legend Command Parameter Display Action Mode Sequential transfer													

9.1.3 RDDST: Read Display Status (09H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDST	0	1	0	0	0	0	0	1	0	0	1	(09h)
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	-
3rd parameter	1	0	1	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16	-
4th parameter	1	0	1	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	-
5th parameter	1	0	1	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	-

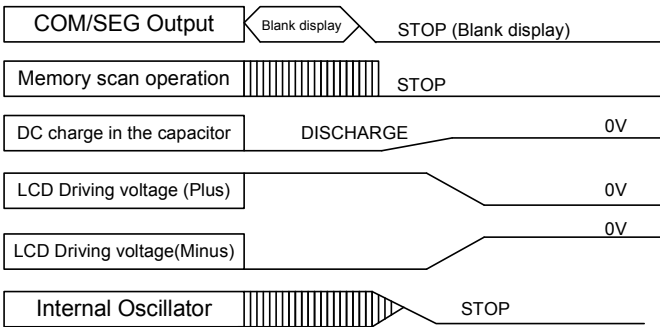
NOTE: “-“ Don’t care

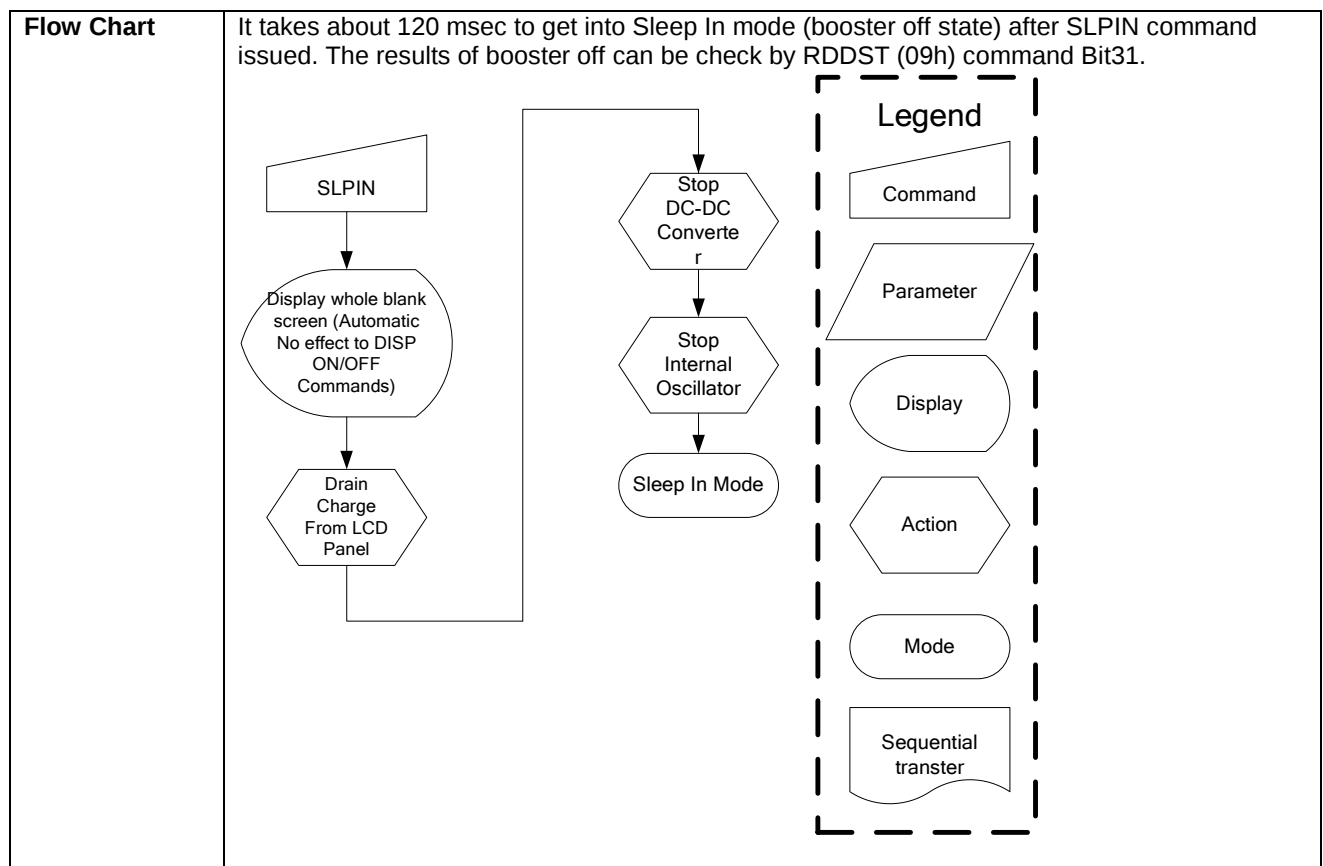
Description	This command indicates the current status of the display as described in the table below:		
Bit	Description	Value	
ST31	Booster Voltage Status	“1”=Booster on, “0”=off	
ST30	Row Address Order (MY)	“1”=Decrement, “0”=Increment	
ST29	Column Address Order (MX)	“1”=Decrement, “0”=Increment	
ST28	Row/Column Order (MV)	“1”= Row/column exchange (MV=1) “0”= Normal (MV=0)	
ST27	Scan Address Order (ML)	“1”=Decrement, “0”=Increment	
ST26	RGB/BGR Order (RGB)	“1”=BGR, “0”=RGB	
ST25	Not Used	“0”	
ST24	Not Used	“0”	
ST23	Not Used	“0”	
ST22	Interface Color Pixel Format Definition	“010” = 8-bit / pixel, “011” = 12-bit / pixel type A “100” = 12-bit / pixel type B “101” = 16-bit / pixel, “110” = 18-bit / pixel, “111” = 24-bit / pixel	
ST21			
ST20			
ST19	Idle Mode On/Off	“1” = On, “0” = Off	
ST18	Partial Mode On/Off	“1” = On, “0” = Off	
ST17	Sleep In/Out	“1” = Out, “0” = In	
ST16	Display Normal Mode On/Off	“1” = Normal Display, “0” = Partial Display	
ST15	Vertical Scrolling Status	“1” = Scroll on, “0” = Scroll off	
ST14	Not Used	“0”	
ST13	Inversion Status	“1” = On, “0” = Off	
ST12	All Pixels On	“1” = mode On, “0” = mode Off	
ST11	All Pixels Off	“1” = mode On, “0” = mode Off	
ST10	Display On/Off	“1” = On, “0” = Off	
ST9	Internal Use	--	
ST8	Not Used	“0”	
ST7	Not Used	“0”	
ST6	Not Used	“0”	
ST5	Internal Use	--	
ST4	Not Used	“0”	
ST3	Not Used	“0”	
ST2	Not Used	“0”	
ST1	Not Used	“0”	
ST0	Not Used	“0”	

Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value (ST31 to ST0)
	Power On Sequence	0000 0000 0101 0001 0000 0000 0000 0000
	S/W Reset	0xxx xx00 0xxx 0001 0000 0000 0000 0000
	H/W Reset	0000 0000 0101 0001 0000 0000 0000 0000
Flow Chart	Serial I/F Mode <pre> graph TD A[/Read 09h/] --> B[/Dummy Clock/] B --> C[/Send 2nd parameter/] C --> D[/Send 3rd parameter/] D --> E[/Send 4th parameter/] E --> F[/Send 5th parameter/] </pre> Parallel I/F Mode <pre> graph TD A[/Read 09h/] --> B[/Dummy Read/] B --> C[/Send 2nd parameter/] C --> D[/Send 3rd parameter/] D --> E[/Send 4th parameter/] E --> F[/Sendth parameter/] </pre> Legend <pre> graph TD subgraph Legend direction TB L1[/Command/] L2[/Parameter/] L3([Display]) L4{{Action}} L5([Mode]) L6[Sequential transfer] end </pre>	

9.1.4 SLPIN: Sleep In (10H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SLPIN	0	1	0	0	0	0	1	0	0	0	0	(10h)
Parameter	No Parameter											

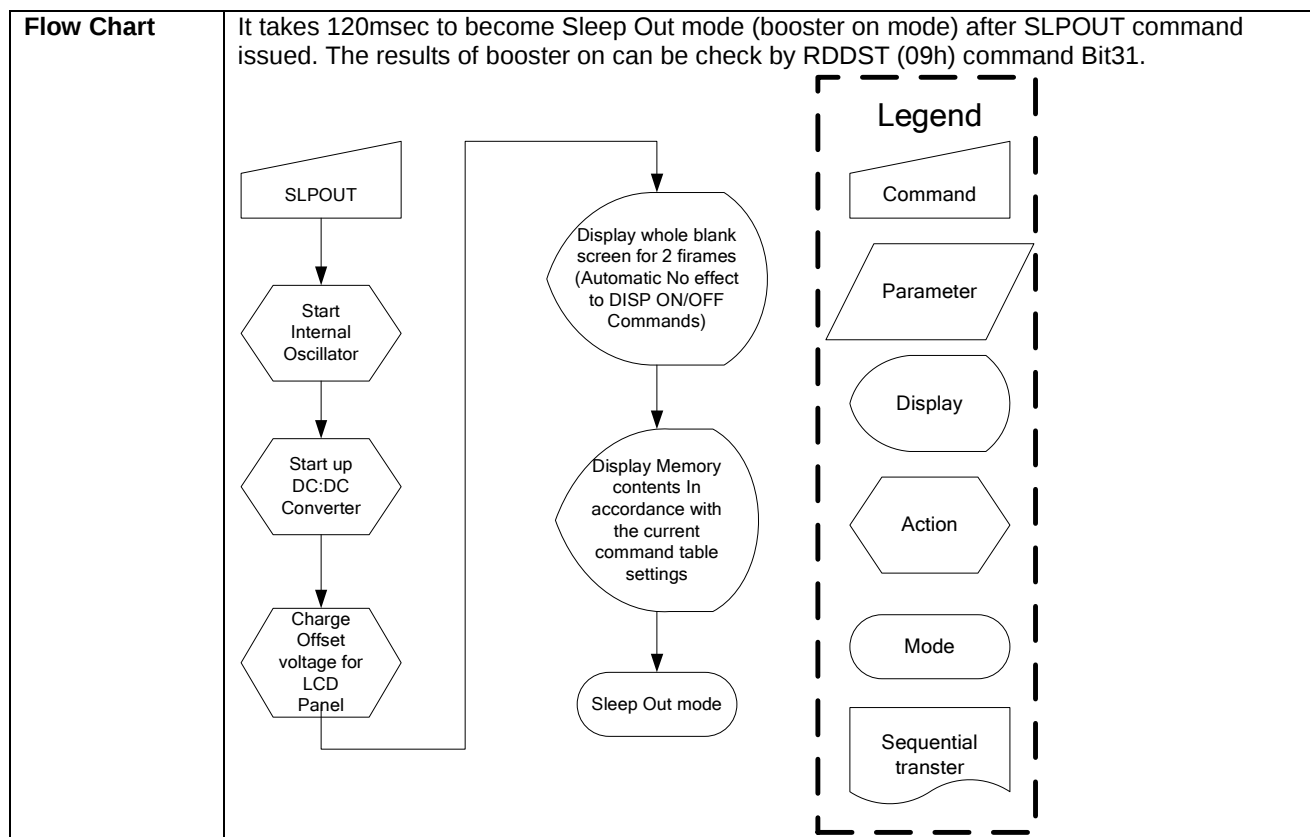
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.  MCU interface and memory are still working and the memory keeps its contents	
	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending the next command. This is for allowing time to stabilize supply voltages and clock circuits. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
Default	Power On Sequence	Sleep in mode
	S/W Reset	Sleep in mode
Default	H/W Reset	Sleep in mode



9.1.5 SLPOUT: Sleep Out (11H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SLPOUT	0	1	0	0	0	0	1	0	0	0	1	(11h)
Parameter	No Parameter											

Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started. (If DISPON 29h is set) COM/SEG Output STOP (Blank display) Memory Contents Memory scan operation DC charge in the capacitor 0V CHARGE LCD Driving voltage (Plus) 0V LCD Driving voltage (Minus) 0V Internal Oscillator STOP		
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10h). It will be necessary to wait 5msec before sending the next command. This is for allowing time to stabilize supply voltages and clock circuits. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.		
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value	
	Power On Sequence	Sleep in mode	
	S/W Reset	Sleep in mode	
	H/W Reset	Sleep in mode	



9.1.6 PTLON: Partial Display Mode On (12H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PTLON	0	1	0	0	0	0	1	0	0	1	0	(12h)
Parameter	No Parameter											

Description	This command turns on Partial mode. The partial mode window is described by the Partial Area command (30H) Exit from PTLON by Normal Display Mode On command (13H) There is no abnormal visual effect during mode change between Normal mode On <=> Partial mode On.		
Restriction	This command has no effect when Partial mode is active.		
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value	
	Power On Sequence	Partial mode off	
	S/W Reset	Partial mode off	
	H/W Reset	Partial mode off	
Flow Chart	See Partial Area (30h)		

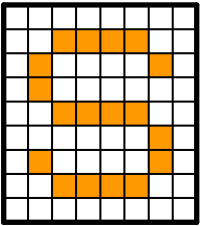
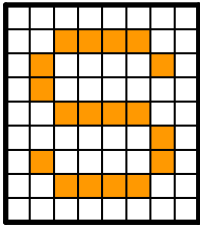
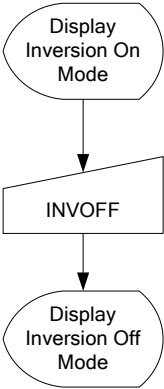
9.1.7 NORON: Normal Display Mode On (13H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NORON	0	1	0	0	0	0	1	0	0	1	1	(13h)
Parameter	No Parameter											

Description	This command returns the display to normal mode. Normal display mode on means Partial mode off, Scroll mode Off. Exit from NORON by the Partial mode On command (12h) There is no abnormal visual effect during mode change between Normal mode On <=> Partial mode On.		
Restriction	This command has no effect when Normal Display mode is active.		
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value	
	Power On Sequence	Normal Mode On	
	S/W Reset	Normal Mode On	
	H/W Reset	Normal Mode On	
Flow Chart	See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command		

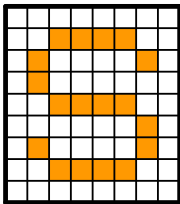
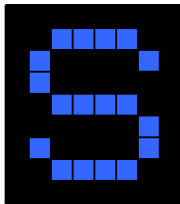
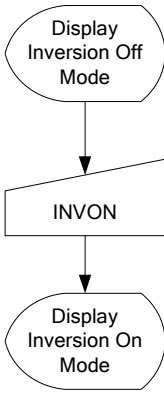
9.1.8 INVOFF: Display Inversion Off (20H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
INVOFF	0	1	0	0	0	1	0	0	0	0	0	(20h)
Parameter	No Parameter											

Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. (Example) Memory  → Display 												
Restriction	This command has no effect when module is already inversion off mode.												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Display Inversion off</td></tr> <tr> <td>S/W Reset</td><td>Display Inversion off</td></tr> <tr> <td>H/W Reset</td><td>Display Inversion off</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	Display Inversion off	S/W Reset	Display Inversion off	H/W Reset	Display Inversion off				
Status	Default Value												
Power On Sequence	Display Inversion off												
S/W Reset	Display Inversion off												
H/W Reset	Display Inversion off												
Flow Chart	 <pre> graph TD A([Display Inversion On Mode]) --> B[/INVOFF/] B --> C([Display Inversion Off Mode]) </pre> Legend Command Parameter Display Action Mode Sequential transfer												

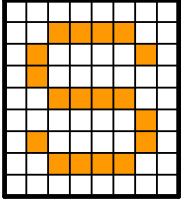
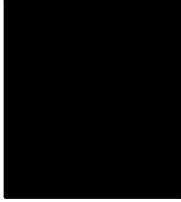
9.1.9 INVON: Display Inversion On (21H)

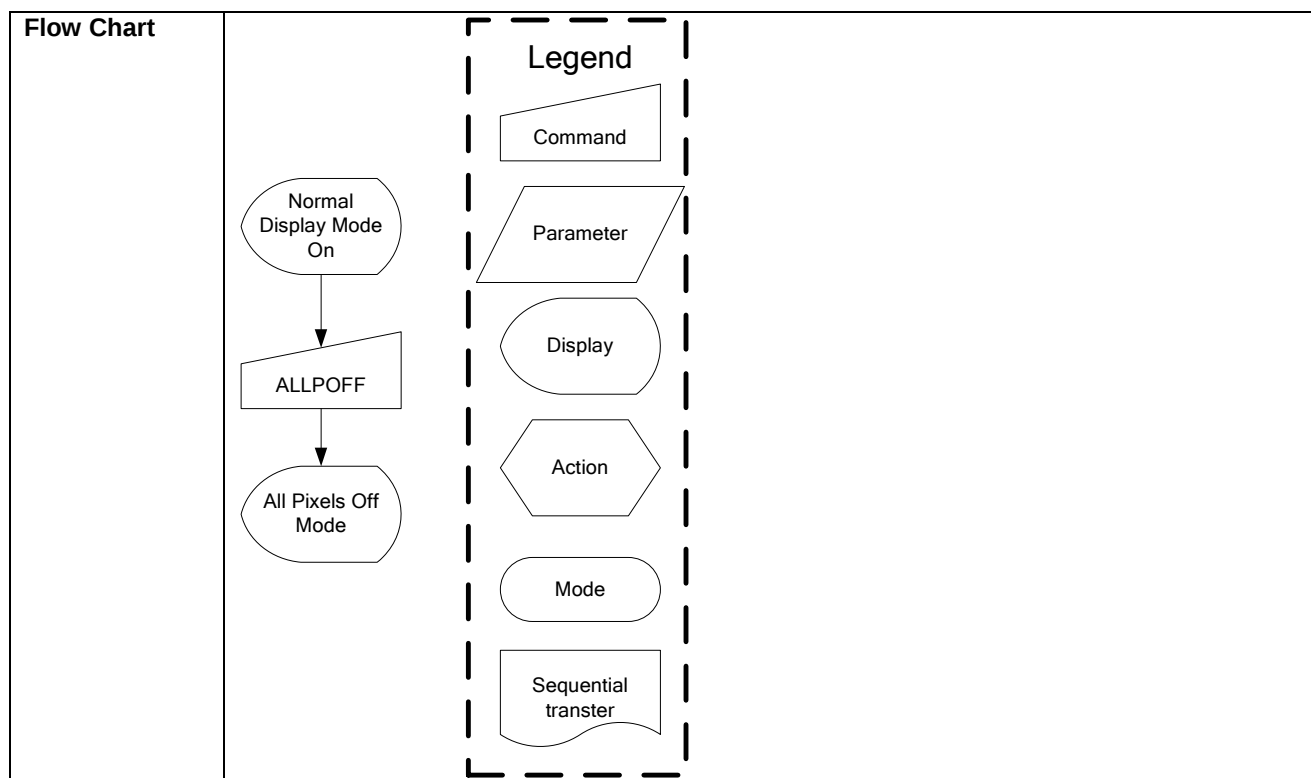
Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
INVON	0	1	0	0	0	1	0	0	0	0	1	(21h)
Parameter	No Parameter											

Description	This command is used to enter into display inversion mode This command makes no change of contents of frame memory. This command does not change any other status. To exit from Display Inversion On, the Display Inversion Off command (20h) should be written. (Example) Memory  → Display 		
Restriction	This command has no effect when module is already Inversion On mode.		
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value	
	Power On Sequence	Display Inversion off	
	S/W Reset	Display Inversion off	
	H/W Reset	Display Inversion off	
Flow Chart	 Legend Command Parameter Display Action Mode Sequential transter		

9.1.10 APOFF: All Pixels Off (22H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
APOFF	0	1	0	0	0	1	0	0	0	1	0	(22h)
Parameter	No Parameter											

Description	This command is only used for test purpose e.g. pixel response time (on/off) measurements on the passive matrix display. Therefore, it is possible that this command is not used for final product software. All driver outputs become “Low” data state and display becomes black. This command makes no change of contents of display memory. This command does not change any other status. Exit commands are “All Pixels On”, “Normal Display Mode On” and “Partial Display On”. The display is showing the contents of the frame memory after “Normal Display Mode On” and “Partial Display On” commands. (Example) Memory  → Display 	
Restriction	This command has no effect when module is already All Pixel Off mode.	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	All pixel off mode disable
	S/W Reset	All pixel off mode disable
	H/W Reset	All pixel off mode disable



9.1.11 APON: All Pixels On (23H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
APON	0	1	0	0	0	1	0	0	0	1	1	(23h)
Parameter	No Parameter											

Description	This command is only used for test purpose e.g. pixel response time (on/off) measurements on the passive matrix display. Therefore, it is possible that this command is not used for final product software. All driver outputs become “High” data state and display becomes white. This command makes no change of contents of display memory. This command does not change any other status. Exit commands are “All Pixels On”, “Normal Display Mode On” and “Partial Display On”. The display is showing the contents of the frame memory after “Normal Display Mode On” and “Partial Display On” commands. (Example) Memory → Display												
Restriction	This command has no effect when module is already All Pixel On mode.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>All pixel on mode disable</td></tr> <tr> <td>S/W Reset</td><td>All pixel on mode disable</td></tr> <tr> <td>H/W Reset</td><td>All pixel on mode disable</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	All pixel on mode disable	S/W Reset	All pixel on mode disable	H/W Reset	All pixel on mode disable				
Status	Default Value												
Power On Sequence	All pixel on mode disable												
S/W Reset	All pixel on mode disable												
H/W Reset	All pixel on mode disable												
Flow Chart	<pre> graph TD A([Normal Display Mode On]) --> B[/ALLPON/] B --> C([All Pixels On Mode]) </pre> Legend Command Parameter Display Action Mode Sequential transter												

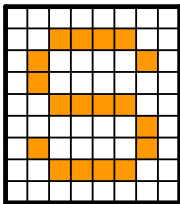
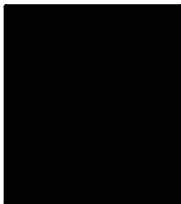
9.1.12 WRCNTR: Write Contrast (25H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
WRCNTR	0	1	0	0	0	1	0	0	1	0	1	(25h)
Parameter	1	1	0		EV6	EV5	EV4	EV3	EV2	EV1	EV0	

Description	This command is used to fine tuning the contrast of the current display. This contrast values can affect segment and common outputs. Parameter range: 0-127dec. MSB is EV6 and LSB is EV0. Default value: 63dec (3Fh)													
Restriction	-													
Register Availability	<table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table><tr><td>Status</td><td>Default Value</td></tr><tr><td>Power On Sequence</td><td>3Fh</td></tr><tr><td>S/W Reset</td><td>3Fh</td></tr><tr><td>H/W Reset</td><td>3Fh</td></tr></table>		Status	Default Value	Power On Sequence	3Fh	S/W Reset	3Fh	H/W Reset	3Fh				
Status	Default Value													
Power On Sequence	3Fh													
S/W Reset	3Fh													
H/W Reset	3Fh													
Flow Chart	WRCNTR ↓ EV[7:0] ↓ New Contrast Value Loaded Legend Command Parameter Display Action Mode Sequential transter													

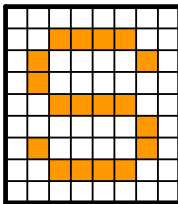
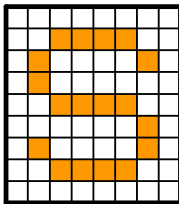
9.1.13 DISPOFF: Display Off (28H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DISPOFF	0	1	0	0	0	1	0	1	0	0	0	(28h)
Parameter	No Parameter											

Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disables and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. Exit from this command by Display On (29h) (Example) Memory  → Display 														
Restriction	This command has no effect when module is already in Display Off mode.														
Register Availability	<table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability														
Normal Mode On, Idle Mode Off, Sleep Out	Yes														
Normal Mode On, Idle Mode On, Sleep Out	Yes														
Partial Mode On, Idle Mode Off, Sleep Out	Yes														
Partial Mode On, Idle Mode On, Sleep Out	Yes														
Sleep In	Yes														
Default	<table><tr><td>Status</td><td>Default Value</td></tr><tr><td>Power On Sequence</td><td>Display off</td></tr><tr><td>S/W Reset</td><td>Display off</td></tr><tr><td>H/W Reset</td><td>Display off</td></tr></table>		Status	Default Value	Power On Sequence	Display off	S/W Reset	Display off	H/W Reset	Display off					
Status	Default Value														
Power On Sequence	Display off														
S/W Reset	Display off														
H/W Reset	Display off														
Flow Chart	Display On Mode ↓ DISPOFF ↓ Display Off Mode Legend Command Parameter Display Action Mode Sequential transfer														

9.1.14 DISPON: Display On (29H)

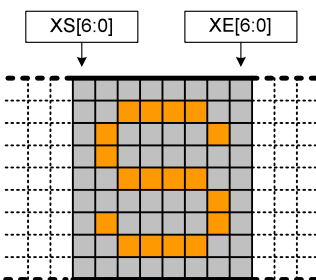
Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DISPON	0	1	0	0	0	1	0	1	0	0	1	(29h)
Parameter	No Parameter											

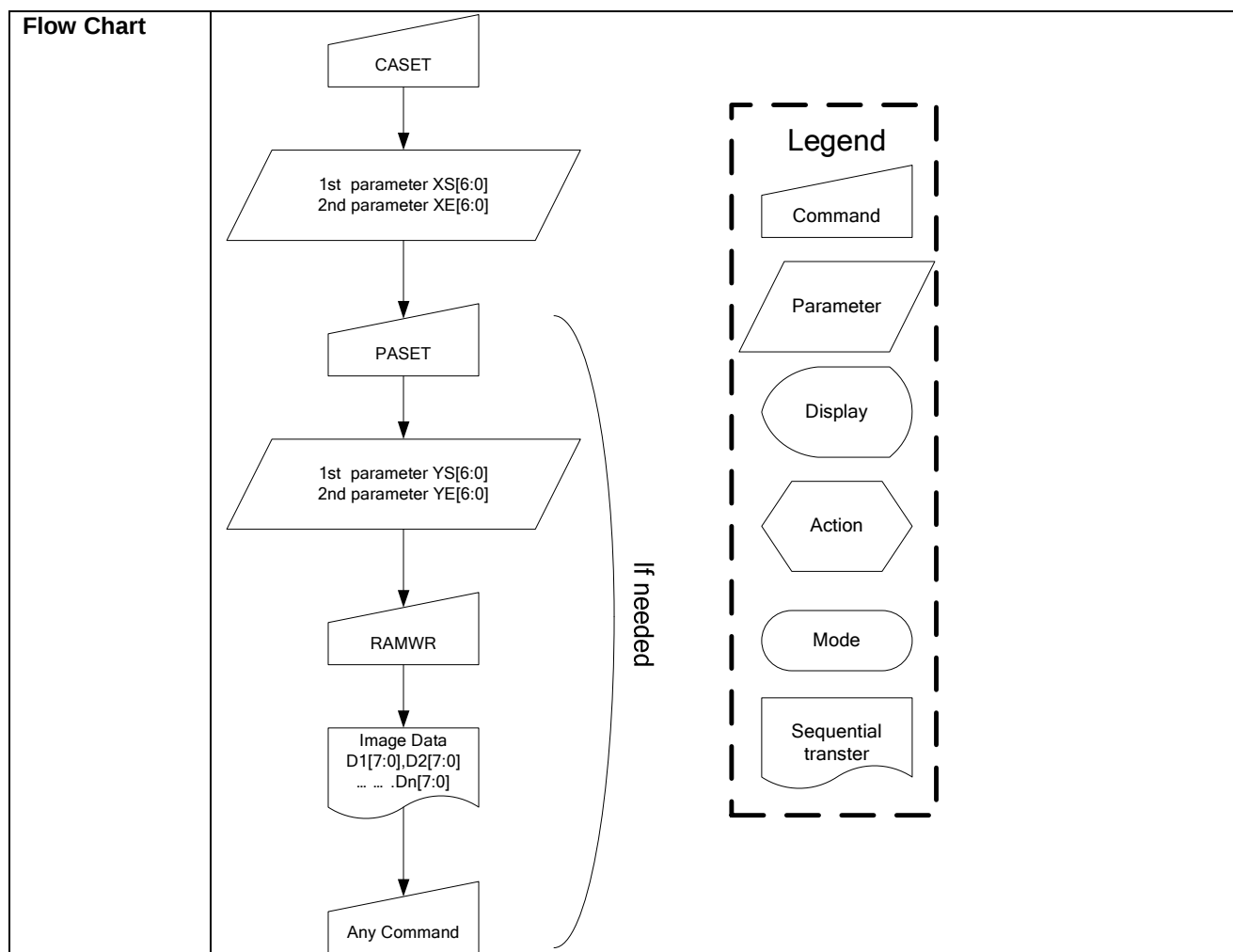
Description	Turn on the display screen according to the current display data RAM content and the display timing and setting. This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status. (Example) Memory  → Display 														
Restriction	This command has no effect when module is already in Display On mode.														
Register Availability	<table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability														
Normal Mode On, Idle Mode Off, Sleep Out	Yes														
Normal Mode On, Idle Mode On, Sleep Out	Yes														
Partial Mode On, Idle Mode Off, Sleep Out	Yes														
Partial Mode On, Idle Mode On, Sleep Out	Yes														
Sleep In	Yes														
Default	<table><tr><td>Status</td><td>Default Value</td></tr><tr><td>Power On Sequence</td><td>Display off</td></tr><tr><td>S/W Reset</td><td>Display off</td></tr><tr><td>H/W Reset</td><td>Display off</td></tr></table>		Status	Default Value	Power On Sequence	Display off	S/W Reset	Display off	H/W Reset	Display off					
Status	Default Value														
Power On Sequence	Display off														
S/W Reset	Display off														
H/W Reset	Display off														
Flow Chart	Display Off Mode ↓ DISPON ↓ Display On Mode Legend Command Parameter Display Action Mode Sequential transfer														

9.1.15 CASET: Column Address Set (2AH)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
CASET	0	1	0	0	0	1	0	1	0	1	0	(2Ah)
1st Parameter	1	1	0	-	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
2nd Parameter	1	1	0	-	XE6	XE5	XE4	XE3	XE2	XE1	XE0	

NOTE: “-“ Don’t care

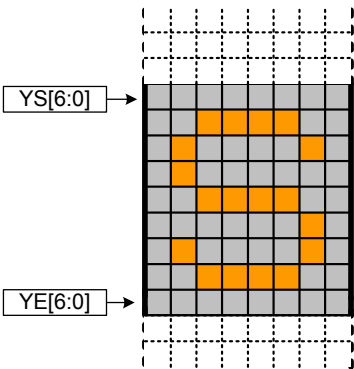
Description	This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The value of XS [6:0] and XE [6:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.			
	(Example) 			
Restriction	XS [6:0] always must be equal to or less than XE [6:0] When XS [6:0] or XE [6:0] is greater than 65h (when MV=0) or 5Fh (when MV=1), data of out of range will be ignored. (Parameter range: 0 ≤ XS [7:0] ≤ XE [7:0] ≤ 101(65h)) : MV="0" (Parameter range: 0 ≤ XS [7:0] ≤ XE [7:0] ≤ 95(5Fh) : MV="1"			
Register Availability	Status		Availability	
	Normal Mode On, Idle Mode Off, Sleep Out		Yes	
	Normal Mode On, Idle Mode On, Sleep Out		Yes	
	Partial Mode On, Idle Mode Off, Sleep Out		Yes	
	Partial Mode On, Idle Mode On, Sleep Out		Yes	
	Sleep In		Yes	
Default	Status		Default Value	
		XS [6:0]	XE [6:0] (MV=0)	XE [6:0] (MV=1)
	Power On Sequence	00h (00d)	65h (101d)	
	S/W Reset	00h (00d)	65h (101d)	5Fh (95d)
	H/W Reset	00h (00d)	65h (101d)	

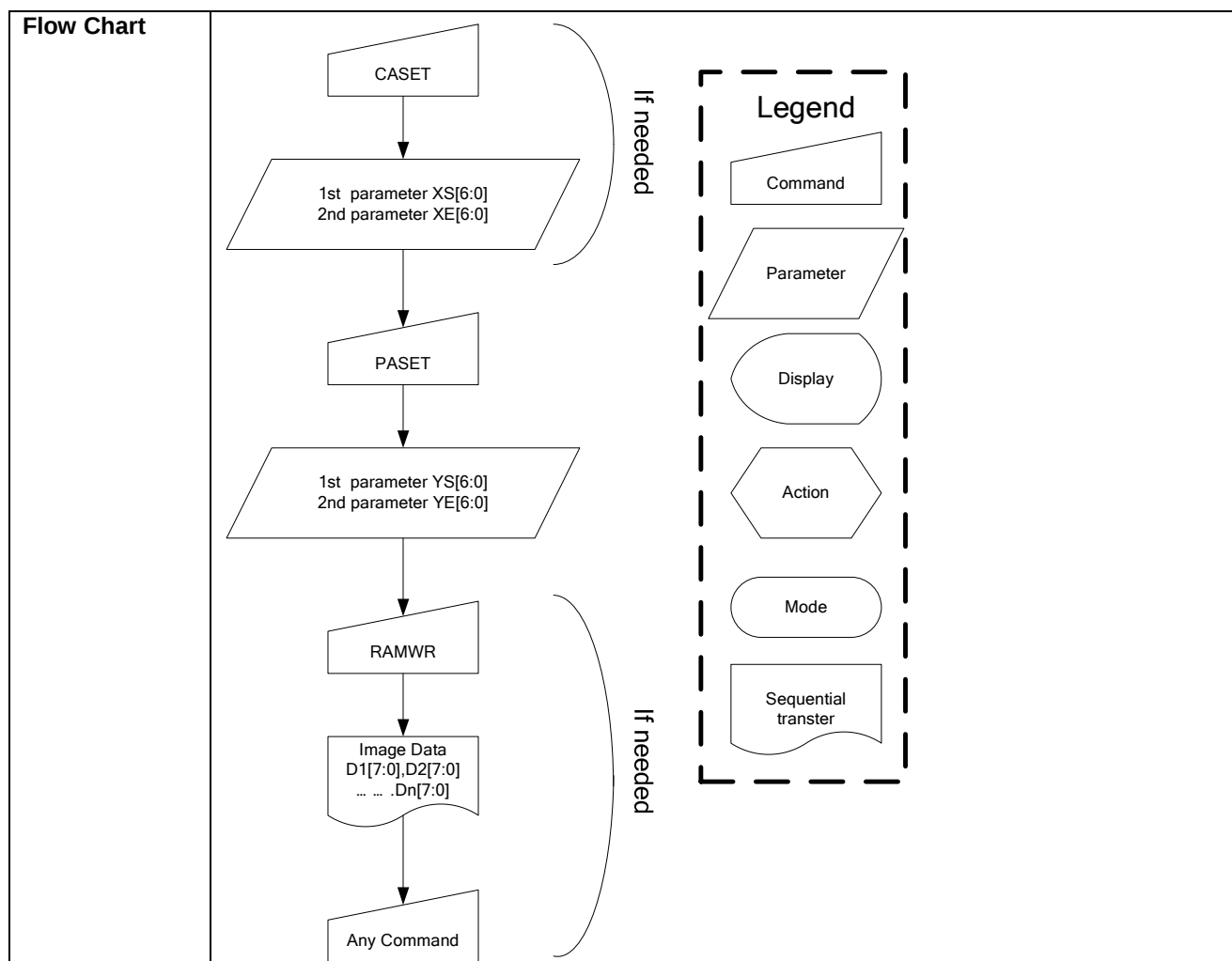


9.1.16 RASET: Row Address Set (2BH)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RASET	0	1	0	0	0	1	0	1	0	1	1	(2Bh)
1st Parameter	1	1	0	-	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
2nd Parameter	1	1	0	-	YE6	YE5	YE4	YE3	YE2	YE1	YE0	

NOTE: “-“ Don’t care

Description	This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The value of YS [6:0] and YE [6:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory. (Example) 											
	YS [6:0] always must be equal to or less than YE [6:0] When YS [6:0] or YE [6:0] is greater than 5Fh (when MV=0) or 65h (when MV=1), data of out of range will be ignored. (Parameter range: 0≤YS [6:0] ≤YE [6:0] ≤95 (5Fh)) : MV = “0” (Parameter range: 0≤YS [6:0] ≤YE [6:0] ≤101 (65h)) : MV = “1”											
Register Availability	Status						Availability					
	Normal Mode On, Idle Mode Off, Sleep Out						Yes					
	Normal Mode On, Idle Mode On, Sleep Out						Yes					
	Partial Mode On, Idle Mode Off, Sleep Out						Yes					
	Partial Mode On, Idle Mode On, Sleep Out						Yes					
	Sleep In						Yes					
Default	Status						Default Value					
							YS [6:0]	YE [6:0] (MV=0)	YE [6:0] (MV=1)			
	Power On Sequence						00h (00d)	5Fh (95d)				
	S/W Reset						00h (00d)	5Fh (95d)	65h (101d)			
	H/W Reset						00h (00d)	5Fh (95d)				



9.1.17 RAMWR: Memory Write (2CH)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RAMWR	0	1	0	0	0	1	0	1	1	0	0	(2Ch)
Write Data 1 D1[7:0]	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0	-
:	1	1	0	:	:	:	:	:	:	:	:	-
Write Data n Dn[7:0]	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0	-

Description	This command is used to transfer data MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions. The Start Column/Start Row positions are different in accordance with MADCTR setting. Then D [7:0] is stored in frame memory and the column register and the row register incremented as in Figure 7.3. Frame Write can be canceled by sending any other command.													
Restriction	In all color modes, there is no restriction on length of parameters.													
Register Availability	<table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table><tr><td>Status</td><td>Default Value</td></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>S/W Reset</td><td>Contents of memory is remained</td></tr><tr><td>H/W Reset</td><td>Contents of memory is remained</td></tr></table>	Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is remained	H/W Reset	Contents of memory is remained					
Status	Default Value													
Power On Sequence	Contents of memory is set randomly													
S/W Reset	Contents of memory is remained													
H/W Reset	Contents of memory is remained													
Flow Chart	RAMWR ↓ Image Data D1[7:0],D2[7:0]Dn[7:0] ↓ Any Command Legend Command Parameter Display Action Mode Sequential transter													

9.1.18 RAMRD : Memory Read (2EH)

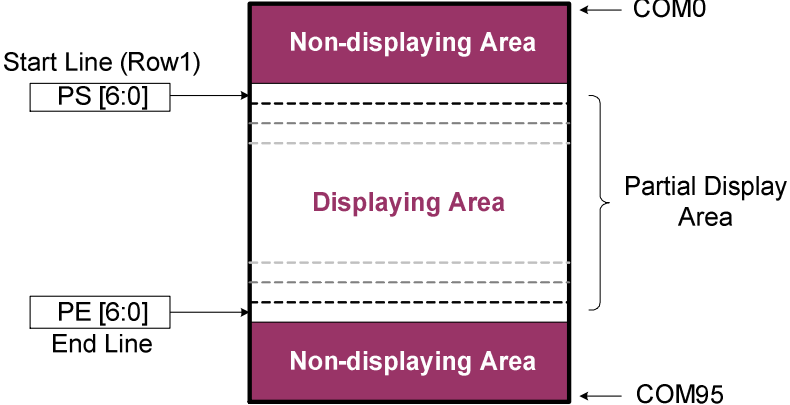
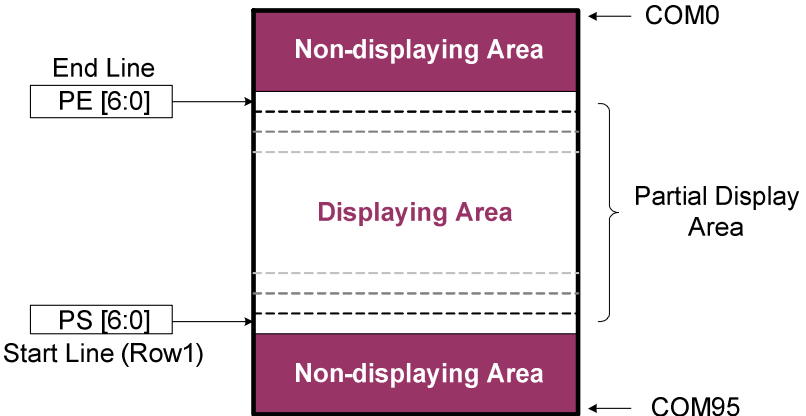
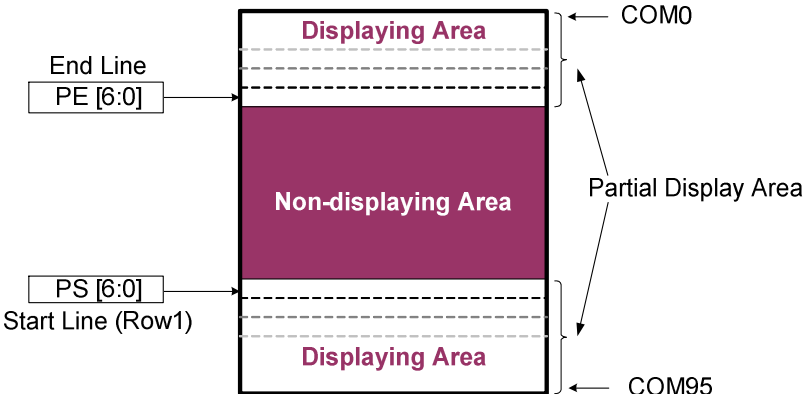
Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RAMRD	0	1	0	0	0	1	0	1	1	0	0	(2Eh)
Dummy Read	1	0	1	x	x	x	x	x	x	x	x	x
Read Data 1 D1[7:0]	1	0	1	D7	D6	D5	D4	D3	D2	D1	D0	00H ~ FFH
...	1	0	1	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00H ~ FFH
Read Data n Dn[7:0]	1	0	1	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00H ~ FFH

Description	This command is used to transfer data from frame memory to MCU. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTR setting. Then D[7:0] is read back from the frame memory and the column register and the page register incremented. Frame Read can be stopped by sending any other command.													
Restriction	In all color modes, the Frame Read is always 16bit so there is no restriction on length of parameters. Note: Memory Read is only possible via the Parallel Interface.													
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Booster Off</td><td>Yes</td></tr></table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In or Booster Off	Yes													
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>S/W Reset</td><td>Contents of memory is not cleared</td></tr><tr><td>H/W Reset</td><td>Contents of memory is not cleared</td></tr></table>		Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is not cleared	H/W Reset	Contents of memory is not cleared				
Status	Default Value													
Power On Sequence	Contents of memory is set randomly													
S/W Reset	Contents of memory is not cleared													
H/W Reset	Contents of memory is not cleared													
Flow Chart	RAMRD Dummy Image Data D1[7:0],D2[7:0]Dn[7:0] Any Command Legend Command Parameter Display Action Mode Sequential transfer													

9.1.19 PTLAR: Partial Area (30H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PTLAR	0	1	0	0	0	1	1	0	0	0	0	(30h)
1st Parameter	1	1	0	-	PS6	PS5	PS4	PS3	PS2	PS1	PS0	-
2nd Parameter	1	1	0	-	PE6	PE5	PE4	PE3	PE2	PE1	PE0	-

NOTE: “-“ Don’t care

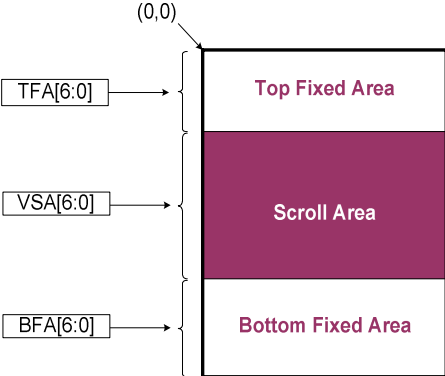
Description	This command defines the partial mode’s display area. There are 2 parameters associated with this command, the first defines the Start Line (PS) and the second the End Line (PE), as illustrated in the figures below. PSL and PEL refer to the Frame Memory Line counter. If End Line > Start Line when MADCTR ML=0:  If End Line > Start Line when MADCTR ML=1:  If End Line < Start Line when MADCTR ML=0:  * Row1: Frame memory row address 1. If End Line = Start Line then the Partial Area will be one line deep.
Restriction	PSL[6:0] and PEL[6:0] is based on line unit. PSL[6:0]=00h, 01h, 02h, 03h, ... , 5Fh

Register Availability	PEL[6:0]= 00h, 01h, 02h, 03h, ... , 5Fh		
	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value	
		PSL [6:0]	PEL [6:0]
	Power On Sequence	00h (00d)	5Fh (95d)
	S/W Reset	00h (00d)	5Fh (95d)
	H/W Reset	00h (00d)	5Fh (95d)
Flow Chart	2. Leave Partial Mode		
	1. TO Enter Partial Mode: <pre> graph TD PLTAR[PLTAR] --> SR[SR[15:0]] SR --> ER[ER[15:0]] ER --> PTLON[PTLON] PTLON --> PM[Partial Mode] </pre> 2. Leave Partial Mode <pre> graph TD PM[Partial Mode] --> DISPOFF[DISPOFF] DISPOFF --> NORON[NORON] NORON --> PMOFF[Partial Mode OFF] PMOFF --> RAMRW[RAMRW] RAMRW --> ID[Image Data D1[7:0], D2[7:0] Dn[7:0]] ID --> DISPON[DISPON] </pre> (Optional) To prevent Tearing Effect Image displayed Legend - Command - Parameter - Display - Action - Mode - Sequential transfer		

9.1.20 SCRLAR: Scroll Area (33H)

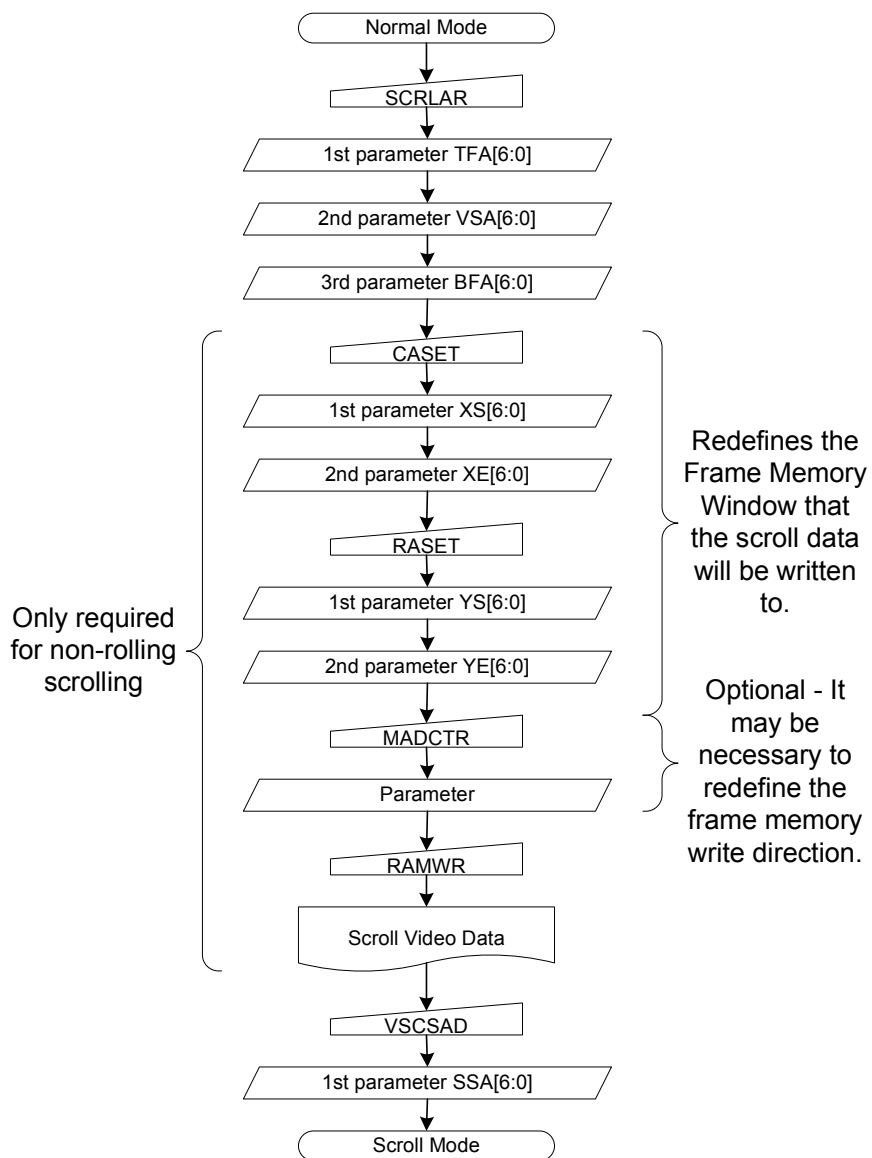
Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SCRLAR	0	1	0	0	0	1	1	0	0	1	1	(33h)
1st parameter	1	1	0	-	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	-
2nd parameter	1	1	0	-	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	-
3rd parameter	1	1	0	-	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	-

NOTE: “-“ Don't care

Description	This command just defines the Vertical Scrolling Area of the display and not performs vertical scroll. When MADCTR BL=0 The 1st parameter TFA [6:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display). The 2nd parameter VSA [6:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address) The first line appears immediately after the bottom most line of the Top Fixed Area. The 3rd parameter BFA [6:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer.				
					
Restriction	The condition is (TFA+VSA+BFA) = 96, otherwise Scrolling mode is undefined. In Vertical Scroll Mode, MADCTR parameter MV should be set to '0'-this only affects the Frame Memory Write. TFA[6:0], VSA[6:0] and BFA[6:0] is based on line unit. TFA[6:0]= 00h, 01h, 02h, 03h, ... , 5Fh VSA[6:0]= 00h, 01h, 02h, 03h, ... , 5Fh BFA[6:0]= 00h, 01h, 02h, 03h, ... , 5Fh				
Register Availability	Status		Availability		
	Normal Mode On, Idle Mode Off, Sleep Out		Yes		
	Normal Mode On, Idle Mode On, Sleep Out		Yes		
	Partial Mode On, Idle Mode Off, Sleep Out		Yes		
	Partial Mode On, Idle Mode On, Sleep Out		Yes		
	Sleep In		Yes		
Default	Status		Default Value		
			TFA [6:0]	VSA [6:0]	BFA [6:0]
	Power On Sequence		00h	5Fh (95d)	00h
	S/W Reset		00h	5Fh (95d)	00h
	H/W Reset		00h	5Fh (95d)	00h

Flow Chart

1. TO Enter Vertical Scroll Mode:



Legend

Command

Parameter

Display

Action

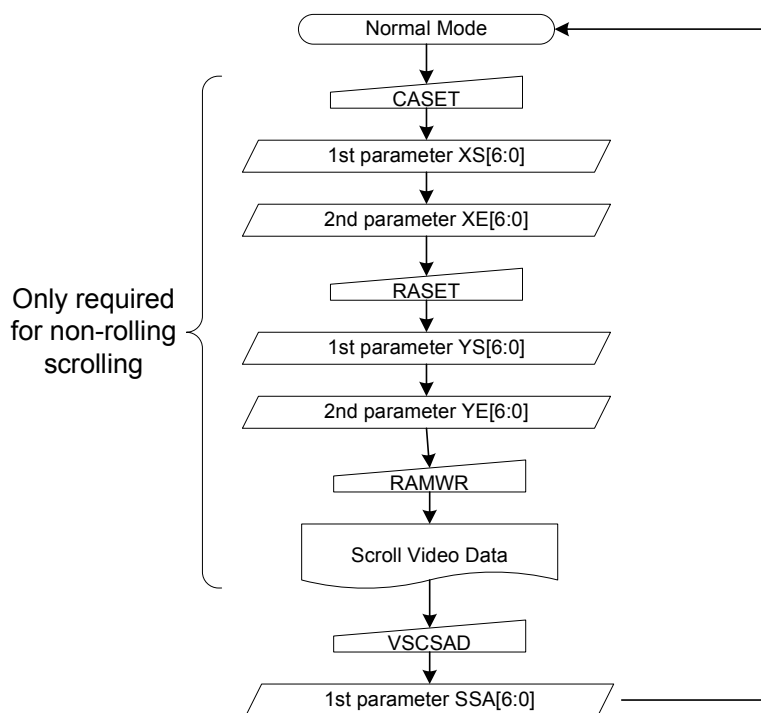
Mode

Sequential transfer

NOTE: The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.

Flow Chart

2. Continuous Scroll:



Legend

Command

Parameter

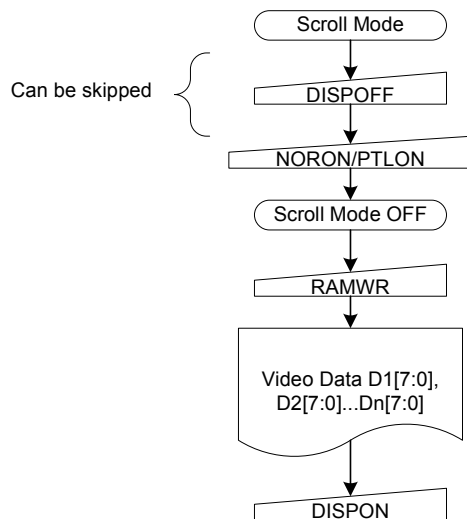
Display

Action

Mode

Sequential transfer

3. To Exit Vertical Scroll Mode:

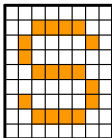
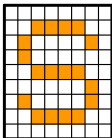
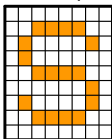
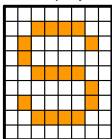
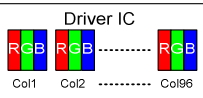
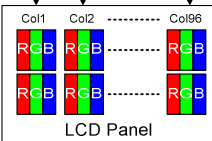
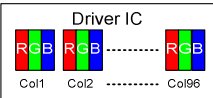
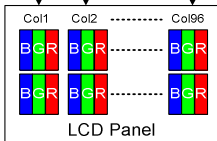


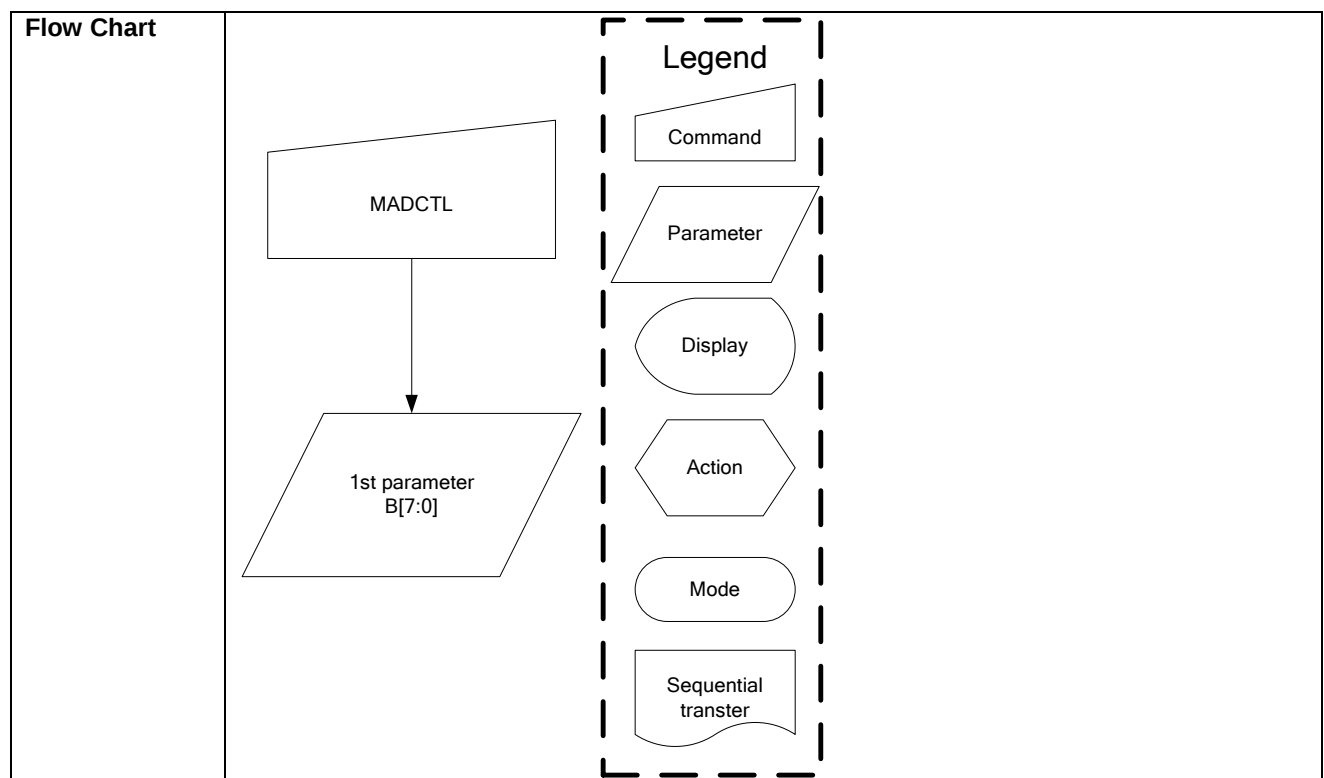
NOTE: Scroll Mode can be exit by both the Normal Display Mode On(13h) and Partial Mode On (12h) commands.

9.1.21 MADCTR: Memory Data Access Control (36H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
MADCTR	0	1	0	0	0	1	1	0	1	1	0	(36h)
Parameter	1	1	0	MY	MX	MV	ML	RGB	-	-	-	-

NOTE: “-“ Don't care

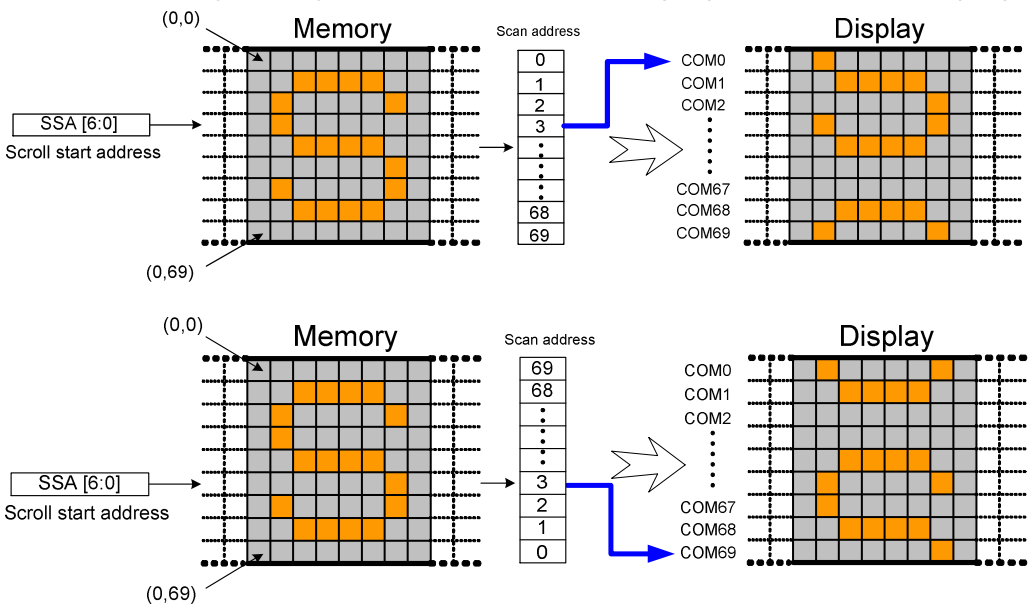
Description	This command defines read/write scanning direction of frame memory. This command makes no change on the other driver status. Note: ML affects to Partial Area (30h), Vertical Scrolling Definition (33h), Vertical Scrolling Start address (37h), Partial On (12h) commands																	
	Bit Assignment																	
	<table><tr><td>Bit</td><td>NAME</td><td>DESCRIPTION</td></tr><tr><td>MY</td><td>ROW ADDRESS ORDER</td><td rowspan="3">These 3bits controls MCU to memory write/read direction. (See Section 7.3.2 “MCU to memory write/read direction”)</td></tr><tr><td>MX</td><td>COLUMN ADDRESS ORDER</td></tr><tr><td>MV</td><td>ROW/COLUMN ORDER</td></tr><tr><td>ML</td><td>LINE ADDRESS ORDER</td><td>LCD refresh direction control</td></tr><tr><td>RGB</td><td>RGB-BGR ORDER</td><td>Color selector switch control 0=RGB color filter panel, 1=BGR color filter panel) The contents of the frame memory are not changed.</td></tr></table>	Bit	NAME	DESCRIPTION	MY	ROW ADDRESS ORDER	These 3bits controls MCU to memory write/read direction. (See Section 7.3.2 “MCU to memory write/read direction”)	MX	COLUMN ADDRESS ORDER	MV	ROW/COLUMN ORDER	ML	LINE ADDRESS ORDER	LCD refresh direction control	RGB	RGB-BGR ORDER	Color selector switch control 0=RGB color filter panel, 1=BGR color filter panel) The contents of the frame memory are not changed.	
	Bit	NAME	DESCRIPTION															
	MY	ROW ADDRESS ORDER	These 3bits controls MCU to memory write/read direction. (See Section 7.3.2 “MCU to memory write/read direction”)															
	MX	COLUMN ADDRESS ORDER																
	MV	ROW/COLUMN ORDER																
	ML	LINE ADDRESS ORDER	LCD refresh direction control															
	RGB	RGB-BGR ORDER	Color selector switch control 0=RGB color filter panel, 1=BGR color filter panel) The contents of the frame memory are not changed.															
	ML: Line(Scan) Address Order Memory  ML="0" Display  Sent 1st Sent 2nd Sent 3rd ... Sent last Memory  ML="1" Display  Sent last ... Sent 3rd Sent 2nd Sent 1st																	
RGB: RGB-BGR Order RGB="0" Driver IC  Col1 Col2 Col96 LCD Panel  RGB="1" Driver IC  Col1 Col2 Col96 LCD Panel 																		
Restriction		D2, D1 and D0 of the 1 st parameter are set to '000' internally.																
Register Availability	Status		Availability															
	Normal Mode On, Idle Mode Off, Sleep Out		Yes															
	Normal Mode On, Idle Mode On, Sleep Out		Yes															
	Partial Mode On, Idle Mode Off, Sleep Out		Yes															
	Partial Mode On, Idle Mode On, Sleep Out		Yes															
	Sleep In		Yes															
Default	Status		Default Value															
	Power On Sequence		MY=0,MX=0,MV=0,ML=0,RGB=0															
	S/W Reset		Not changed															
	H/W Reset		MY=0,MX=0,MV=0,ML=0,RGB=0															



9.1.22 VSCSAD: Vertical Scroll Start Address of RAM (37h)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
VSCSAD	0	1	0	0	0	1	1	0	1	1	1	(37h)
Parameter	1	1	0	-	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	

NOTE: “-“ Don’t care

Description	This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below: This command Start the scrolling. Exit from V-scrolling mode by commands Partial mode On (12h) or Normal mode On (13h).  NOTE: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. SSA refers to the Frame Memory line Pointer												
Restriction	Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h)-otherwise undesirable image will be displayed on the Panel. SSA [6:0] is based on line unit. SSA [6:0] = 00h, 01h, 02h, 03h, ... , 5Fh												
Register Availability	<table> <tr> <th>Status</th><th>Availability</th></tr> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	No	Partial Mode On, Idle Mode On, Sleep Out	No	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	No												
Partial Mode On, Idle Mode On, Sleep Out	No												
Sleep In	Yes												
Default	<table> <tr> <th>Status</th><th>Default Value</th></tr> <tr> <td>Power On Sequence</td><td>00</td></tr> <tr> <td>S/W Reset</td><td>00</td></tr> <tr> <td>H/W Reset</td><td>00</td></tr> </table>	Status	Default Value	Power On Sequence	00	S/W Reset	00	H/W Reset	00				
Status	Default Value												
Power On Sequence	00												
S/W Reset	00												
H/W Reset	00												
Flow Chart	See Vertical Scrolling Definition (33h) description.												

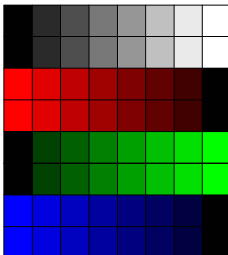
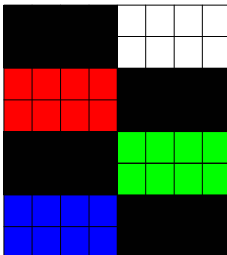
9.1.23 IDMOFF: Idle Mode Off (38H)

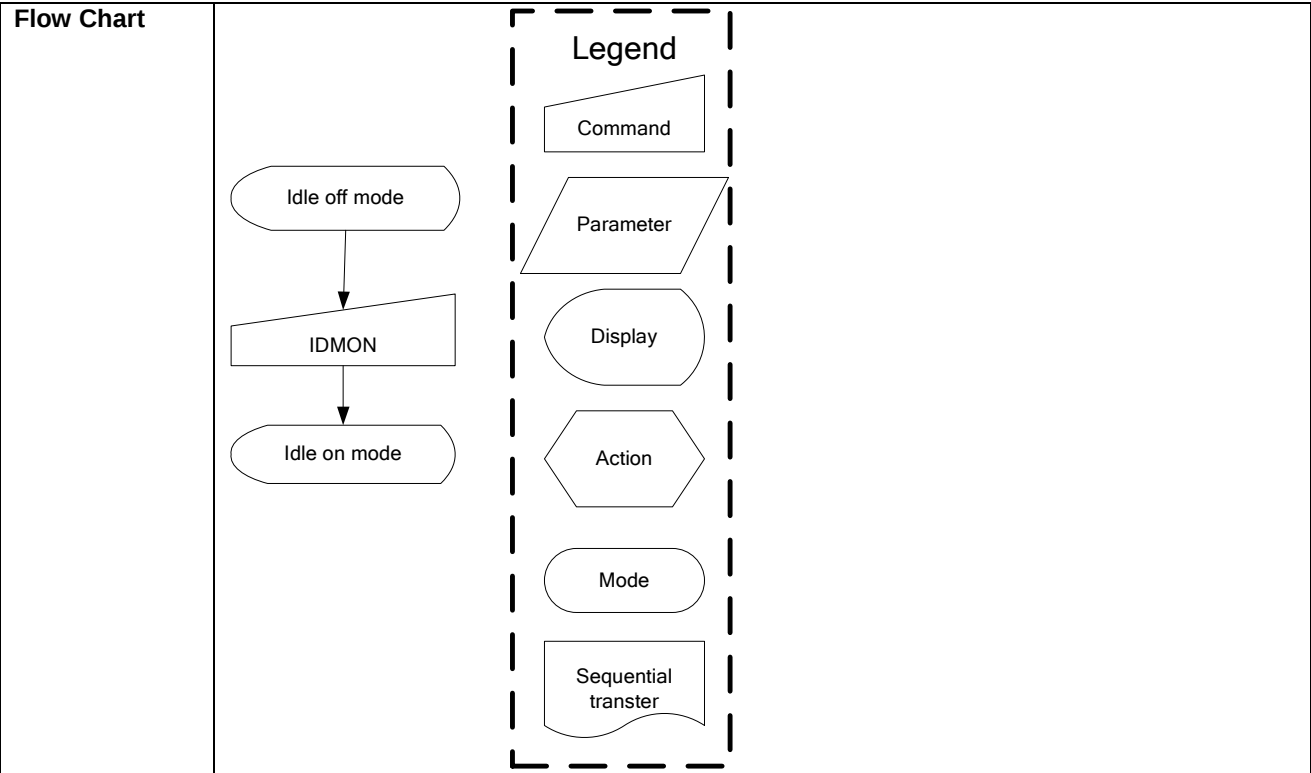
Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
IDMOFF	0	1	0	0	0	1	1	1	0	0	0	(38h)
Parameter	No Parameter											

Description	This command is used to recover from Idle mode on. There will be no abnormal visible effect on the display mode change transition. In the idle off mode, 1. LCD can display maximum 65536 colors. 2. Normal frame frequency is applied.		
Restriction	This command has no effect when module is already in idle off mode.		
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value	
	Power On Sequence	Idle mode off	
	S/W Reset	Idle mode off	
	H/W Reset	Idle mode off	
Flow Chart	Idle on mode ↓ IDMOFF ↓ Idle off mode Legend Command Parameter Display Action Mode Sequential transfer		

9.1.24 IDMON: Idle Mode On (39H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
IDMON	0	1	0	0	0	1	1	1	0	0	1	(39h)
Parameter	No Parameter											

Description	This command is used to enter into Idle mode on. There will be no abnormal visible effect on the display mode change transition. In the idle on mode, 1. Color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed. 2. 8-Color mode frame frequency is applied. 3. Exit from IDMON by Idle Mode Off (38h) command (Example)																
	Memory 								Display 								
	“X”: don't care																
	Color	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
	Black	0	X	X	X	X	0	X	X	X	X	X	0	X	X	X	X
	Blue	0	X	X	X	X	0	X	X	X	X	X	1	X	X	X	X
	Red	1	X	X	X	X	0	X	X	X	X	X	0	X	X	X	X
	Magenta	1	X	X	X	X	0	X	X	X	X	X	1	X	X	X	X
	Green	0	X	X	X	X	1	X	X	X	X	X	0	X	X	X	X
	Cyan	0	X	X	X	X	1	X	X	X	X	X	1	X	X	X	X
Yellow	1	X	X	X	X	1	X	X	X	X	X	0	X	X	X	X	
White	1	X	X	X	X	1	X	X	X	X	X	1	X	X	X	X	
Restriction	This command has no effect when module is already in idle on mode.																
Register Availability	Status					Availability											
	Normal Mode On, Idle Mode Off, Sleep Out					Yes											
	Normal Mode On, Idle Mode On, Sleep Out					Yes											
	Partial Mode On, Idle Mode Off, Sleep Out					Yes											
	Partial Mode On, Idle Mode On, Sleep Out					Yes											
	Sleep In					Yes											
Default	Status					Default Value											
	Power On Sequence					Idle mode off											
	S/W Reset					Idle mode off											
	H/W Reset					Idle mode off											



9.1.25 COLMOD: Interface Pixel Format (3AH)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
COLMOD	0	1	0	0	0	1	1	1	0	1	0	(3Ah)
Parameter	1	1	0	-	-	-	-	-	P2	P1	P0	-

Description	This command is used to define the format of RGB picture data, which is to be transferred via the MCU Interface. The formats are shown in the table:																																						
	<table><tr><td>Interface Format</td><td>P2</td><td>P1</td><td>P0</td></tr><tr><td>Not Defined</td><td>0</td><td>0</td><td>0</td></tr><tr><td>Not Defined</td><td>0</td><td>0</td><td>1</td></tr><tr><td>8Bit/ Pixel /256</td><td>0</td><td>1</td><td>0</td></tr><tr><td>12Bit/Pixel /4K (Type A)</td><td>0</td><td>1</td><td>1</td></tr><tr><td>12Bit/Pixel /4K (Type B)</td><td>1</td><td>0</td><td>0</td></tr><tr><td>16Bit/Pixel/65K</td><td>1</td><td>0</td><td>1</td></tr><tr><td>18Bit/Pixel/262K</td><td>1</td><td>1</td><td>0</td></tr><tr><td>24Bit/Pixel/16M</td><td>1</td><td>1</td><td>1</td></tr></table>	Interface Format	P2	P1	P0	Not Defined	0	0	0	Not Defined	0	0	1	8Bit/ Pixel /256	0	1	0	12Bit/Pixel /4K (Type A)	0	1	1	12Bit/Pixel /4K (Type B)	1	0	0	16Bit/Pixel/65K	1	0	1	18Bit/Pixel/262K	1	1	0	24Bit/Pixel/16M	1	1	1		
Interface Format	P2	P1	P0																																				
Not Defined	0	0	0																																				
Not Defined	0	0	1																																				
8Bit/ Pixel /256	0	1	0																																				
12Bit/Pixel /4K (Type A)	0	1	1																																				
12Bit/Pixel /4K (Type B)	1	0	0																																				
16Bit/Pixel/65K	1	0	1																																				
18Bit/Pixel/262K	1	1	0																																				
24Bit/Pixel/16M	1	1	1																																				
Restriction	There is no visible effect until the Frame Memory is written to.																																						
Register Availability	<table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																										
Status	Availability																																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																																						
Sleep In	Yes																																						
Default	<table><tr><td>Status</td><td>Default Value</td></tr><tr><td>Power On Sequence</td><td>05h (16Bit/Pixel/65K)</td></tr><tr><td>S/W Reset</td><td>No Change</td></tr><tr><td>H/W Reset</td><td>05h (16Bit/Pixel/65K)</td></tr></table>	Status	Default Value	Power On Sequence	05h (16Bit/Pixel/65K)	S/W Reset	No Change	H/W Reset	05h (16Bit/Pixel/65K)																														
Status	Default Value																																						
Power On Sequence	05h (16Bit/Pixel/65K)																																						
S/W Reset	No Change																																						
H/W Reset	05h (16Bit/Pixel/65K)																																						
Flow Chart	16 Bit/Pixel Mode COLMOD 011 12 Bit/Pixel Mode Legend Command Parameter Display Action Mode Sequential transfer																																						

9.1.26 DutySet: Display Duty setting (B0H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DutySet	0	1	0	1	0	1	1	0	0	0	0	(B0h)
Parameter	1	1	0	0	Du6	Du5	Du4	Du3	Du2	Du1	Du0	-

NOTE: “-“ Don't care

Description	This command is used to set display duty. Command set = display duty numbers - 1.								
	Example:								
	Duty	Du6	Du5	Du4	Du3	Du2	Du1	Du0	Command set= Display duty numbers-1
	Example: 1/96 duty	1	0	1	1	1	1	1	96-1=95
Restriction	Display duty must > 4 (1/4 duty)								
Register Availability	Status					Availability			
	Normal Mode On, Idle Mode Off, Sleep Out					Yes			
	Normal Mode On, Idle Mode On, Sleep Out					Yes			
	Partial Mode On, Idle Mode Off, Sleep Out					Yes			
	Partial Mode On, Idle Mode On, Sleep Out					Yes			
	Sleep In					Yes			
Default	Status				Default Value (Du[6:0])				
	Power On Sequence				01011101b (5Fh)				
	S/W Reset				01011101b (5Fh)				
	H/W Reset				01011111b (5Fh)				
Flow Chart	DutySet Du[6:0] Legend Command Parameter Display Action Mode Sequential transfer								

9.1.27 FirstCom: First Com. Page address (B1H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
FirstCom	0	1	0	1	0	1	1	0	0	0	1	(B1h)
Parameter	1	1	0	--	F6	F5	F4	F3	F2	F1	F0	-

NOTE: "-- Don't care

Description	This command defines the first output COM number that mapping to the RAM page address 0. For detail setting value, please see the table as below.							
	F6	F5	F4	F3	F2	F1	F0	Line address
	0	0	0	0	:	:	0	0
	0	0	0	0	:	:	1	1
	0	0	0	1	:	:	0	2
	0	0	0	1	:	:	1	3
	:	:	:	:	:	:	:	:
	1	0	1	1	1	1	1	95
	Example: If FirstCom=8, common 8 would output the data of RAM page address 0.							
	Restriction							
Register Availability	Status				Availability			
	Normal Mode On, Idle Mode Off, Sleep Out				Yes			
	Normal Mode On, Idle Mode On, Sleep Out				Yes			
	Partial Mode On, Idle Mode Off, Sleep Out				Yes			
	Partial Mode On, Idle Mode On, Sleep Out				Yes			
	Sleep In				Yes			
Default	Status				Default Value (F[6:0])			
	Power On Sequence				00h			
	S/W Reset				00h			
	H/W Reset				00h			
Flow Chart	FirstCom F[6:0] Legend Command Parameter Display Action Mode Sequential transfer							

9.1.28 OscDiv: FOSC Divider (B3H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
OscDiv	0	1	0	1	0	1	1	0	0	1	1	(B3h)
Parameter	1	1	0	-	-	-	-	-	-	CLD1	CLD0	-

NOTE: “-“ Don't care

Description	This command is used to specify the CL dividing ratio. CLD1, CLD0: CL dividing ratio. They are used to change number of dividing stages of external or internal clock.		
	CLD1	CLD0	CL dividing ratio
	0	0	Not divide
	0	1	2 divisions
	1	0	4 divisions
	1	1	8 divisions
Restriction			
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value (CLD[0:1])	
	Power On Sequence	00b	
	S/W Reset	00b	
	H/W Reset	00b	
Flow Chart	OscDiv CLD[2:0] Legend Command Parameter Display Action Mode Sequential transfer		

9.1.29 NLInvSet: N-Line control (B5H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NLInvSet	0	1	0	1	0	1	1	0	1	0	1	(B5h)
Parameter	1	1	0	M	N6	N5	N4	N3	N2	N1	N0	-

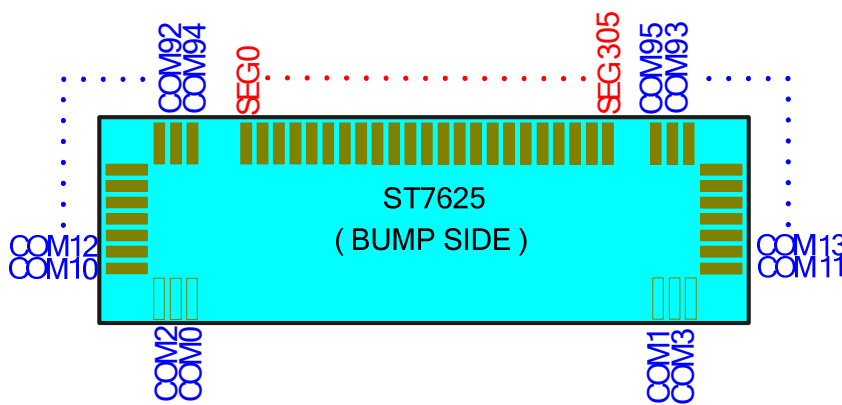
NOTE: “-“ Don't care

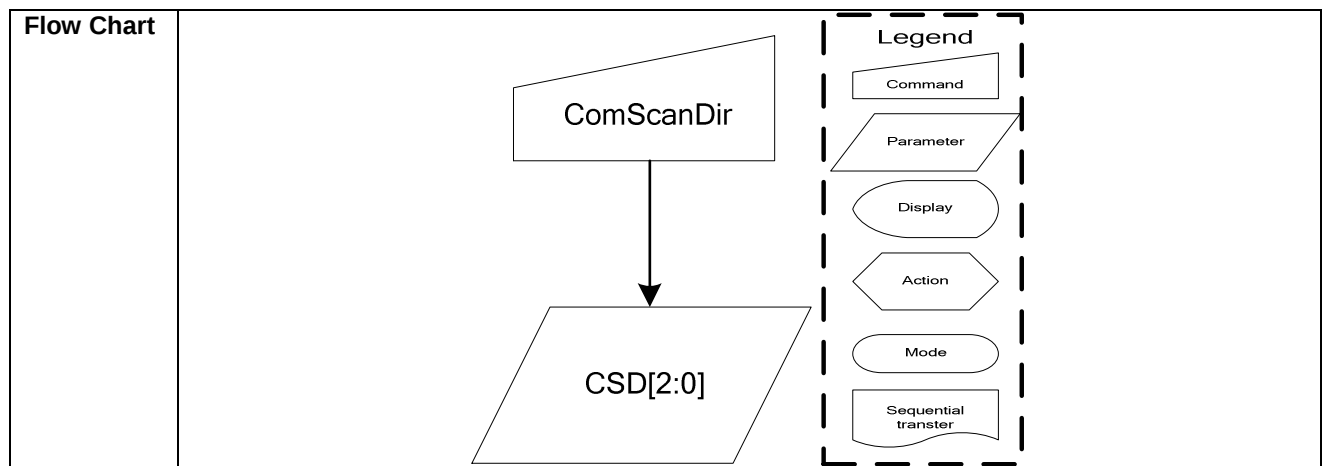
Description	This command is used to set the inverted line number with range of 2 to (duty-1) to improve display quality. When M=0, inversion occurs in every frame; when M=1, inversion is independent from frames. If N[6:0]=0, N-line inversion function is disable. Line inversion numbers=N[6:0] +1. Example: If N[6:0]=7, inversion occurs per 8 line.		
Restriction			
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default			
	Status	Default Value	
		M	N[6:0]
	Power On Sequence	0b	0000000b
	S/W Reset	0b	0000000b
	H/W Reset	0b	0000000b
Flow Chart	NLInvSet M N[6:0] Legend Command Parameter Display Action Mode Sequential transfer		

9.1.30 SEGScanDir: Seg Scan Direction for glass layout (B7H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
ComScanDir	0	1	0	1	0	1	1	0	1	1	1	(B7h)
Parameter	1	1	0	0	SMX	0	0	SBGR	0	0	0	-

NOTE: “-“ Don’t care

Description	Function		0	1												
	SMX	Inverse the MX setting	Keep MX	Inverse MX												
	SBGR	Inverse the BGR setting	Keep BGR	Inverse BGR												
 Common scan direction configuration																
Restriction																
Register Availability	<table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>				Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability															
Normal Mode On, Idle Mode Off, Sleep Out	Yes															
Normal Mode On, Idle Mode On, Sleep Out	Yes															
Partial Mode On, Idle Mode Off, Sleep Out	Yes															
Partial Mode On, Idle Mode On, Sleep Out	Yes															
Sleep In	Yes															
Default	<table><tr><td>Status</td><td>Default Value (CSD[1:0])</td></tr><tr><td>Power On Sequence</td><td>00b</td></tr><tr><td>S/W Reset</td><td>00b</td></tr><tr><td>H/W Reset</td><td>00b</td></tr></table>				Status	Default Value (CSD[1:0])	Power On Sequence	00b	S/W Reset	00b	H/W Reset	00b				
Status	Default Value (CSD[1:0])															
Power On Sequence	00b															
S/W Reset	00b															
H/W Reset	00b															



9.1.31 RMWIN: Read Modify Write control in(B8H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RMWIN	0	1	0	1	0	1	1	1	0	0	0	(B8h)
Parameter	No Parameter											

NOTE: “-“ Don't care

Description	Read modify write control IN											
Restriction	Can only be used in 65K color mode.											
Register Availability	Status						Availability					
	Normal Mode On, Idle Mode Off, Sleep Out						Yes					
	Normal Mode On, Idle Mode On, Sleep Out						Yes					
	Partial Mode On, Idle Mode Off, Sleep Out						Yes					
	Partial Mode On, Idle Mode On, Sleep Out						Yes					
	Sleep In						Yes					
Default	Status						Default Value					
	Power On Sequence						--					
	S/W Reset						--					
	H/W Reset						--					

9.1.32 RMWOUT: Read Modify Write control out(B9H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RMWOUT	0	1	0	1	0	1	1	1	0	0	1	(B9h)
Parameter	No Parameter											

NOTE: “-“ Don’t care

Description	Read modify write control OUT											
Restriction												
Register Availability	Status						Availability					
	Normal Mode On, Idle Mode Off, Sleep Out						Yes					
	Normal Mode On, Idle Mode On, Sleep Out						Yes					
	Partial Mode On, Idle Mode Off, Sleep Out						Yes					
	Partial Mode On, Idle Mode On, Sleep Out						Yes					
	Sleep In						Yes					
Default	Status						Default Value					
	Power On Sequence						--					
	S/W Reset						--					
	H/W Reset						--					

9.1.33 VopSet: Vop set (C0H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
VopSet	0	1	0	1	1	0	0	0	0	0	0	(C0h)
1 st parameter	1	1	0	Vop7	Vop6	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0	-
2 nd parameter	1	1	0	-	-	-	-	-	-	-	Vop8	

NOTE: “-“ Don't care

Description	The command is used to program the optimum LCD supply voltage V0.		
Restriction			
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value (Vop=12V)	
		Vop8	Vop[7:0]
	Power On Sequence	0	11010010b (D2h)
	S/W Reset	0	11010010b (D2h)
	H/W Reset	0	11010010b (D2h)
Flow Chart	VopSet 1st & 2nd parameter Vop[8:0] Legend Command Parameter Display Action Mode Sequential transfer		

9.1.34 VopOffsetInc: Vop Increase 1 (C1H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
VopOffsetInc	0	1	0	1	1	0	0	0	0	0	1	(C1h)

NOTE: “-“ Don't care

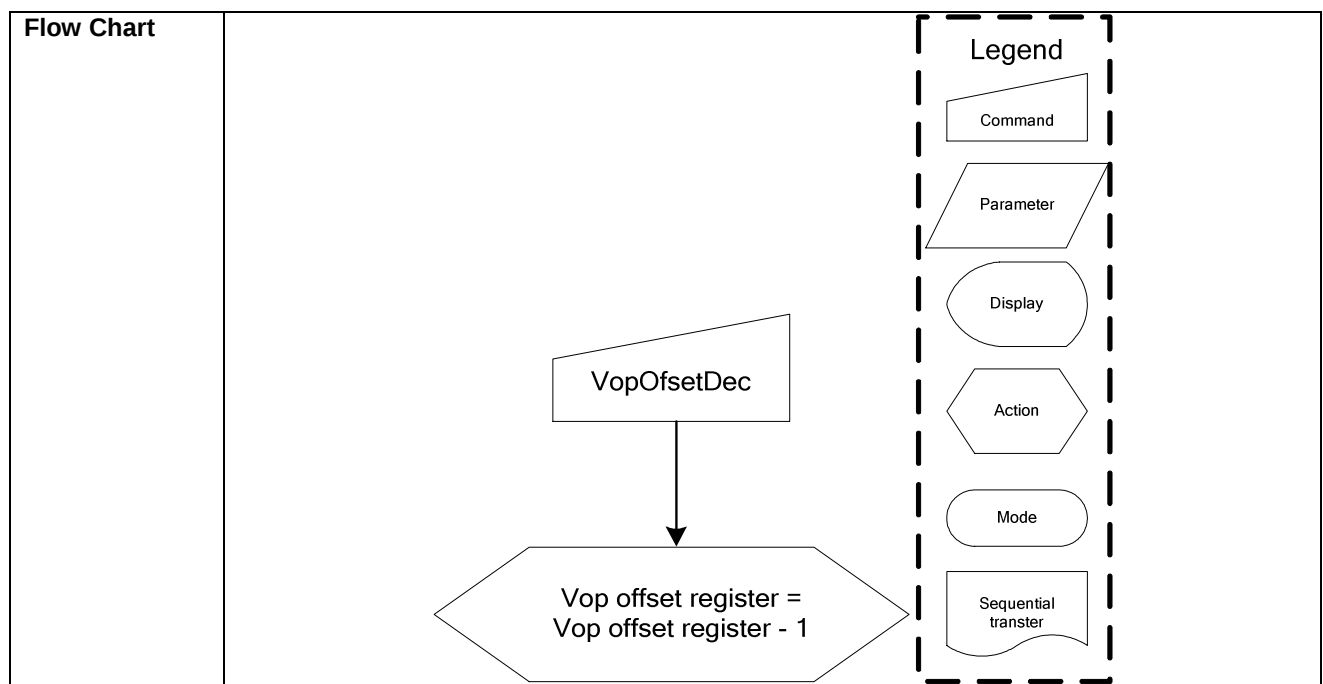
Description	With the VopOffsetInc and VopOffsetDec command the VLCD voltage and therewith the contrast of the LCD can be adjusted. This command increases the value of Vop offset register by 1. If you set the electronic control value to 1111111, the control value is set to 0000000 after this command has been executed.		
Restriction			
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value	
	Power On Sequence	--	
	S/W Reset	--	
	H/W Reset	--	
Flow Chart	VopOffsetInc Vop offset register = Vop offset register + 1 Legend Command Parameter Display Action Mode Sequential transfer		

9.1.35 VopOffsetDec: Vop Decrease 1 (C2H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
VopOffsetDec	0	1	0	1	1	0	0	0	0	1	0	(C2h)

NOTE: “-“ Don't care

Description	With the VopOffsetInc and VopOffsetDec command the VLCD voltage and therewith the contrast of the LCD can be adjusted. This command decreases the value of Vop offset register by 1. If you set the electronic control value to 0000000, the control value is set to 1111111 after this command has been executed.		
	Electronic Control Value	Decimal Equivalent	V0 Offset
	0111111	63	+2520 mV
	0111110	62	+2480 mV
	0111101	61	+2440 mV
	...	...	...
	0000010	2	+80 mV
	0000001	1	+40 mV
	0000000	0	0 mV
	1111111	-1	-40 mV
	1111110	-2	-80 mV
	...	...	...
	1000010	-62	-2480 mV
	1000001	-63	-2520 mV
	1000000	-64	-2560mV
Table 9.1.1 Possible Vop[6:0] values			
Restriction			
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value	
	Power On Sequence	--	
	S/W Reset	--	
	H/W Reset	--	



9.1.36 BiasSel: Bias Selection(C3H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
BiasSel	0	1	0	1	1	0	0	0	0	1	1	(C3h)
Parameter	1	1	0	-	-	-	-	-	Bias2	Bias1	Bias0	-

NOTE: “-“ Don't care

Description	Select LCD bias ratio of the voltage required for driving the LCD.			
	Bais2	Bais1	Bais0	LCD bias
	0	0	0	1/12
	0	0	1	1/11
	0	1	0	1/10
	0	1	1	1/9
	1	0	0	1/8
	1	0	1	1/7
	1	1	0	1/6
	1	1	1	1/5
Restriction				
Register Availability	Status	Availability		
	Normal Mode On, Idle Mode Off, Sleep Out	Yes		
	Normal Mode On, Idle Mode On, Sleep Out	Yes		
	Partial Mode On, Idle Mode Off, Sleep Out	Yes		
	Partial Mode On, Idle Mode On, Sleep Out	Yes		
	Sleep In	Yes		
Default	Status	Default Value (Bias[2:0])		
	Power On Sequence	110b		
	S/W Reset	110b		
	H/W Reset	110b		
Flow Chart	BiasSel ↓ BS[2:0] Legend Command Parameter Display Action Mode Sequential transfer			

9.1.37 BstPmpXSel: Booster Set (C4H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
BstPmpXSel	0	1	0	1	1	0	0	0	1	0	0	(C4h)
Parameter	1	1	0	-	-	-	-	-	BST2	BST 1	BST0	-

NOTE: “-“ Don't care

Description	Booster setting			
	BST2	BST1	BST0	
	0	0	0	x1 boosting circuit (Booster off)
	0	0	1	x2 boosting circuit
	0	1	0	x3 boosting circuit
	0	1	1	x4 boosting circuit
	1	0	0	x5 boosting circuit
	1	0	1	x6 boosting circuit
	1	1	0	x7 boosting circuit
	1	1	1	x8 boosting circuit
Restriction				
Register Availability	Status		Availability	
	Normal Mode On, Idle Mode Off, Sleep Out		Yes	
	Normal Mode On, Idle Mode On, Sleep Out		Yes	
	Partial Mode On, Idle Mode Off, Sleep Out		Yes	
	Partial Mode On, Idle Mode On, Sleep Out		Yes	
	Sleep In		Yes	
Default	Status		Default Value (BST[2:0])	
	Power On Sequence		111b	
	S/W Reset		111b	
	H/W Reset		111b	
Flow Chart	BstPmpXSel Bst[2:0] Legend Command Parameter Display Action Mode Sequential transfer			

9.1.38 BstEffSel: Booster Efficiency selection (C5H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
BstEffSel	0	1	0	1	1	0	0	0	1	0	1	(C5h)
Parameter	1	1	0	-	-	-	-	-	-	BTF1	BTF0	-

NOTE: “-“ Don't care

Description	Booster Efficiency set	
	BTF1	BTF0 Frequency (Hz)
	0	0 Level 1
	0	1 Level 2 (default)
	1	0 Level 3
By Booster Stages (2X, 3X, 4X, 5X, 6X, 7X, 8X) and Booster Efficiency (Level1~3) commands, we could easily set the best Booster performance with suitable current consumption. If the Booster Efficiency is set to higher level (level3 is higher than level1). The Boost Efficiency is better than lower level, and it needs a few more power consumption current.		
Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value (BTF[1:0])
	Power On Sequence	01b
	S/W Reset	01b
	H/W Reset	01b
Flow Chart	<pre> graph TD BstEffSel[Command] --> BTF10[/Parameter/] </pre>	

9.1.39 VopOffset: Vop offset fuse bit adjust(C7H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
VopOffset	0	1	0	1	1	0	0	0	1	1	1	(C7h)
Parameter1	1	1	0	VOS7	VOS6	VOS5	VOS4	VOS3	VOS2	VOS1	VOS0	-
Parameter2	1	1	0	-	-	-	-	-	-	-	VOS8	-

NOTE: “-“ Don't care

Description	The command is used to the Vop offset for V0.		
Restriction			
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value	
		VOS8	VOS[7:0]
	Power On Sequence	0	0
	S/W Reset	0	0
	H/W Reset	0	0
Flow Chart	VopOffset 1st & 2nd parameter VOS[8:0] Legend Command Parameter Display Action Mode Sequential transfer		

9.1.40 VgSorSel: FVg with Bst2x control(CBH)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
VgSorSel	0	1	0	1	1	0	0	1	0	1	1	(CBh)
Parameter	1	1	0	-	-	-	-	-	-	-	2BT0	-

NOTE: “-“ Don’t care

Description	2BT0=0: Vg source comes from VDD2 ; 2BT0=1: Vg source comes from 2-times charge pump.		
Restriction			
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value (2BT0)	
	Power On Sequence	1	
	S/W Reset	1	
	H/W Reset	1	
Flow Chart	VgSorSel 2BT0 Legend Command Parameter Display Action Mode Sequential transfer		

9.1.41 ANASET: Analog circuit setting (D0H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
AutoLoadSet	0	1	0	1	1	0	1	0	0	0	0	(D0h)
Parameter	1	1	0	0	0	0	1	1	1	0	1	-

NOTE: “-“ Don’t care

Description	Analog circuit setting. Such as follower selection, level shifter power selection.		
Restriction			
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value	
	Power On Sequence	1Dh	
	S/W Reset	1Dh	
	H/W Reset	1Dh	
Flow Chart	ANASET 1DH Legend Command Parameter Display Action Mode Sequential transfer		

9.1.42 AutoLoadSet : Mask rom data auto re-load control(D7H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
AutoLoadSet	0	1	0	1	1	0	1	0	1	1	1	(D7h)
Parameter	1	1	0	0	0	0	ARD	1	1	1	1	-

NOTE: “-“ Don't care

Description	Mask rom data auto re-load control ARD : OTP auto recovery enable control, 1: Disable OTP auto recovery, 0: Enable OTP auto recovery		
Restriction			
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value	
		ARD	
	Power On Sequence	0	
	S/W Reset	0	
	H/W Reset	0	
Flow Chart	AutoLoadSet D[4](ARD) Legend Command Parameter Display Action Mode Sequential transfer		

9.1.43 RDTstStatus : Read IC status(DEH)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDTstStatus	0	1	0	1	1	0	1	1	1	1	0	(DEh)
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	
Parameter	1	0	1	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	-

NOTE: “-“ Don’t care

Description	Read IC status. Contact of OTP/ RDA / PWR_VOP read control (selection Byte by StusOutByteSel[3:0] control)		
Restriction			
Register Availability	Status		Availability
	Normal Mode On, Idle Mode Off, Sleep Out		Yes
	Normal Mode On, Idle Mode On, Sleep Out		Yes
	Partial Mode On, Idle Mode Off, Sleep Out		Yes
	Partial Mode On, Idle Mode On, Sleep Out		Yes
	Sleep In		Yes
Default	Status	Default Value	
	Power On Sequence	-	
	S/W Reset	-	
	H/W Reset	-	
Flow Chart	Serial I/F Mode Read 04h Dummy Clock Send 2nd parameter		Parallel I/F Mode Read 04h Dummy Read Send 2nd parameter
	Host Display Legend Command Parameter Display Action Mode Sequential transfer		

9.1.44 EPCTIN: Control OTP WR/RD(E0H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
EPCTIN	0	1	0	1	1	1	0	0	0	0	0	(E0h)
Parameter	1	1	0	0	0	EWR	0	0	0	0	0	-

NOTE: “-“ Don’t care

Description	EWR: when setting “1” → The Write Enable of OTP will be opened. EWR: when setting “0” → The Read Enable of OTP will be opened.		
Restriction			
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value (WR/XRD)	
	Power On Sequence	0	
	S/W Reset	0	
	H/W Reset	0	
Flow Chart	EPCTIN ↓ EWR Legend Command Parameter Display Action Mode Sequential transfer		

9.1.45 EPCOUT: OTP control cancel(E1H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
EPCOUT	0	1	0	1	1	1	0	0	0	0	1	(E1h)

NOTE: “-“ Don't care

Description	IC exits the OTP control circuit when executing this command.		
Restriction			
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value	
	Power On Sequence	--	
	S/W Reset	--	
	H/W Reset	--	
Flow Chart	MTPSEL MS[1:0] EPCTIN EWR=1 EPMWR EPCOUT Legend Command Parameter Display Action Mode Sequential transfer		

9.1.46 EPMWR: Write to OTP(E2H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
EPCOUT	0	1	0	1	1	1	0	0	0	1	0	(E2h)

NOTE: “-“ Don’t care

Description	IC activates trigger to start OTP programming when executing this command.		
Restriction			
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value	
	Power On Sequence	--	
	S/W Reset	--	
	H/W Reset	--	
Flow Chart	MTPSEL ↓ MS[1:0] ↓ EPCTIN ↓ EWR=1 ↓ EPMWR ↓ EPCOUT Legend Command Parameter Display Action Mode Sequential transfer		

9.1.47 EPMRD: Read from OTP(E3H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
EPMRD	0	1	0	1	1	1	0	0	0	1	1	(E3h)

NOTE: “-“ Don't care

Description	IC activates trigger to start OTP data download to circuit when executing this command.		
Restriction			
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value	
	Power On Sequence		
	S/W Reset		
	H/W Reset		
Flow Chart	MTPSEL MS[1:0] EPCTIN EWR=1 EPMWR EPCOUT Legend Command Parameter Display Action Mode Sequential transfer		

9.1.48 OTPSEL: SEL OTP(E4H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
OTPSEL	0	1	0	1	1	1	0	0	1	0	0	(E4h)
Parameter	1	1	0	MS1	MS0	0	1	1	0	0	0	-

NOTE: “-“ Don’t care

Description	This command defines OTP selection for EEPROM control. Please see the table as below:		
	MS1	MS0	Mode
	0	0	Disable
	0	1	OTP
	1	0	Disable
Restriction			
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value (MS[1:0])	
	Power On Sequence	00	
	S/W Reset	00	
	H/W Reset	00	
Flow Chart			

9.1.49 ROMSET: Programmable rom setting(E5H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
OTPSEL	0	1	0	1	1	1	0	0	1	0	1	(E5h)
Parameter	1	1	0	0	0	0	0	1	0	0	1	-

NOTE: “-“ Don’t care

Description	Set the OTP writing timing. Value 0x09 is the best value for ST7625		
Restriction			
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value (MS[1:0])	
	Power On Sequence	0F	
	S/W Reset	0F	
	H/W Reset	0F	
Flow Chart	ROMSET 09H Legend Command Parameter Display Action Mode Sequential transfer		

9.1.50 HPMSET : High Power Mode Setting (EBH)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	0	1	0	1	1	EBH
1st parameter	1	1	0	0	0	0	0	0	0	0	1	
2nd parameter	1	1	0	0	0	0	0	0	0	0	0	

Description	High power mode for volatage compensation.																
Restriction																	
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>			Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes		
Status	Availability																
Normal Mode On, Idle Mode Off, Sleep Out	Yes																
Normal Mode On, Idle Mode On, Sleep Out	Yes																
Partial Mode On, Idle Mode Off, Sleep Out	Yes																
Partial Mode On, Idle Mode On, Sleep Out	Yes																
Sleep In	Yes																
Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>1st Paramter</th><th>2nd Parameter</th></tr><tr><td>Power On Sequence</td><td>00h</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td><td>00h</td></tr></table>			Status	Default Value		1 st Paramter	2 nd Parameter	Power On Sequence	00h	00h	S/W Reset	00h	00h	H/W Reset	00h	00h
Status	Default Value																
	1 st Paramter	2 nd Parameter															
Power On Sequence	00h	00h															
S/W Reset	00h	00h															
H/W Reset	00h	00h															
Flow Chart	HPMSEL 1st parameter : 01H 2nd parameter : 00H Legend Command Parameter Display Action Mode Sequential transfer																

9.1.51 FRMSEL: Frame Freq. in Temp. Range (F0H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	1	0	0	0	0	F0H
1st parameter	1	1	0	-	-	-	DIVA	FA3	FA2	FA1	FA0	Range A
2nd parameter	1	1	0	-	-	-	DIVB	FB3	FB2	FB1	FB0	Range B
3rd parameter	1	1	0	-	-	-	DIVC	FC3	FC2	FC1	FC0	Range C
4th parameter	1	1	0	-	-	-	DIVD	FD3	FD2	FD1	FD0	Range D

Description	Select Frame Freq. in normal display mode.			
	1 st parameter : Frame freq. value set in temperature range 30(-30℃) to TA			
	2 nd parameter : Frame freq. value set in temperature P range TA to TB			
	3 rd parameter : Frame freq. value set in temperature range TB to TC			
	4 th parameter : Frame freq. value set in temperature range TC to 145(90℃)			
	For command setting to frame rate value look-up-table, please see the following table:			
		DIVx	Fx[3:0] (Hex)	Frame Rate (Hz)
	1	0	75	
		1	76	
		2	77	
		3	80	
		4	84	
		5	88	
		6	92	
		7	97	
		8	102	
		9	108	
A		115		
B		123		
C		133		
D		144		
E		155		
F		170		
0	0~F	(Frame Rate)/2		
Restriction				

Register Availability	<table><tr><td colspan="3">Status</td><td>Availability</td></tr><tr><td colspan="3">Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td colspan="3">Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td colspan="3">Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td colspan="3">Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td colspan="3">Sleep In</td><td>Yes</td></tr></table>				Status			Availability	Normal Mode On, Idle Mode Off, Sleep Out			Yes	Normal Mode On, Idle Mode On, Sleep Out			Yes	Partial Mode On, Idle Mode Off, Sleep Out			Yes	Partial Mode On, Idle Mode On, Sleep Out			Yes	Sleep In			Yes
	Status			Availability																								
	Normal Mode On, Idle Mode Off, Sleep Out			Yes																								
	Normal Mode On, Idle Mode On, Sleep Out			Yes																								
	Partial Mode On, Idle Mode Off, Sleep Out			Yes																								
	Partial Mode On, Idle Mode On, Sleep Out			Yes																								
Sleep In			Yes																									
Default	<table><tr><td rowspan="2">Status</td><td colspan="4">Default Value</td></tr><tr><td>FA[4:0]</td><td>FB[4:0]</td><td>FC[4:0]</td><td>FD[4:0]</td></tr><tr><td>Power On Sequence</td><td>06h</td><td>0Bh</td><td>0Dh</td><td>12h</td></tr><tr><td>S/W Reset</td><td>06h</td><td>0Bh</td><td>0Dh</td><td>12h</td></tr><tr><td>H/W Reset</td><td>06h</td><td>0Bh</td><td>0Dh</td><td>12h</td></tr></table>				Status	Default Value				FA[4:0]	FB[4:0]	FC[4:0]	FD[4:0]	Power On Sequence	06h	0Bh	0Dh	12h	S/W Reset	06h	0Bh	0Dh	12h	H/W Reset	06h	0Bh	0Dh	12h
	Status	Default Value																										
		FA[4:0]	FB[4:0]	FC[4:0]	FD[4:0]																							
	Power On Sequence	06h	0Bh	0Dh	12h																							
	S/W Reset	06h	0Bh	0Dh	12h																							
H/W Reset	06h	0Bh	0Dh	12h																								
Flow Chart	FRMSL 1st parameter. FA[4:0] 2nd parameter. FB[4:0] 3rd parameter. FC[4:0] 4th parameter. FD[4:0]																											
	Legend Command Parameter Display Action Mode Sequential transfer																											

9.1.52 FRM8SEL: Frame Freq. in Temp. range (idle-8 color) (F1H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	1	0	0	0	1	F1H
1st parameter	1	1	0	-	-	-	F8A4	F8A3	F8A2	F8A1	F8A0	Range A
2nd parameter	1	1	0	-	-	-	F8B4	F8B3	F8B2	F8B1	F8B0	Range B
3rd parameter	1	1	0	-	-	-	F8C4	F8C3	F8C2	F8C1	F8C0	Range C
4th parameter	1	1	0	-	-	-	F8D4	F8D3	F8D2	F8D1	F8D0	Range D

Description	Select Frame Freq. in normal display mode.(idle;8 color mode) 1 st parameter : Frame freq. value set in TEMP range 30(-30℃) to TA 2 nd parameter : Frame freq. value set in TEMP range TA to TB 3 rd parameter : Frame freq. value set in TEMP range TB to TC 4 th parameter : Frame freq. value set in TEMP range TC to 145(90℃)																											
Restriction																												
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>				Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes												
Status	Availability																											
Normal Mode On, Idle Mode Off, Sleep Out	Yes																											
Normal Mode On, Idle Mode On, Sleep Out	Yes																											
Partial Mode On, Idle Mode Off, Sleep Out	Yes																											
Partial Mode On, Idle Mode On, Sleep Out	Yes																											
Sleep In	Yes																											
Default	<table><tr><th rowspan="2">Status</th><th colspan="4">Default Value</th></tr><tr><th>FA[4:0]</th><th>FB[4:0]</th><th>FC[4:0]</th><th>FD[4:0]</th></tr><tr><td>Power On Sequence</td><td>06h</td><td>0Bh</td><td>0Dh</td><td>12h</td></tr><tr><td>S/W Reset</td><td>06h</td><td>0Bh</td><td>0Dh</td><td>12h</td></tr><tr><td>H/W Reset</td><td>06h</td><td>0Bh</td><td>0Dh</td><td>12h</td></tr></table>				Status	Default Value				FA[4:0]	FB[4:0]	FC[4:0]	FD[4:0]	Power On Sequence	06h	0Bh	0Dh	12h	S/W Reset	06h	0Bh	0Dh	12h	H/W Reset	06h	0Bh	0Dh	12h
Status	Default Value																											
	FA[4:0]	FB[4:0]	FC[4:0]	FD[4:0]																								
Power On Sequence	06h	0Bh	0Dh	12h																								
S/W Reset	06h	0Bh	0Dh	12h																								
H/W Reset	06h	0Bh	0Dh	12h																								
Flow Chart	FRM8SL 1st parameter. F8A[4:0] 2nd parameter. F8B[4:0] 3rd parameter. F8C[4:0] 4th parameter. F8D[4:0] Legend Command Parameter Display Action Mode Sequential transfer																											

9.1.53 Tmprng: Temp. range set for Frame Freq. Adj. (F2H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	1	0	0	1	0	F2H
1st parameter	1	1	0	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0	Range A
2nd parameter	1	1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0	Range B
3rd parameter	1	1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0	Range C

Description	Temp. range set for automatic frame freq. adj. operation according the current temp. value. 1 st parameter: Temp. range A value set 2 nd parameter: Temp. range B value set 3 rd parameter: Temp. range C value set TA/TB/TC Temperature(°C) + 40 = TA/TB/TC[6:0] Example: If TA wants to be set at 24°C, TA[6:0]=24+40=64(40h),																					
Restriction	-40°C ≤TA≤TA+TH≤TB≤TB+TH≤TC≤87°C																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>			Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Partial Mode On, Idle Mode Off, Sleep Out	Yes																					
Partial Mode On, Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><th>TA[6:0]</th><th>TB[6:0]</th><th>TC[6:0]</th></tr><tr><td>Power On Sequence</td><td>1Eh</td><td>28h</td><td>32h</td></tr><tr><td>S/W Reset</td><td>1Eh</td><td>28h</td><td>32h</td></tr><tr><td>H/W Reset</td><td>1Eh</td><td>28h</td><td>32h</td></tr></table>			Status	Default Value			TA[6:0]	TB[6:0]	TC[6:0]	Power On Sequence	1Eh	28h	32h	S/W Reset	1Eh	28h	32h	H/W Reset	1Eh	28h	32h
Status	Default Value																					
	TA[6:0]	TB[6:0]	TC[6:0]																			
Power On Sequence	1Eh	28h	32h																			
S/W Reset	1Eh	28h	32h																			
H/W Reset	1Eh	28h	32h																			
Flow Chart	TMPRNG ↓ 1st parameter. TA[6:0] 2nd parameter.TB[6:0] 3rd parameter. TC[6:0] ↓ TMPHYS ↓ 1st patameter. TH[3:0] Legend Command Parameter Display Action Mode Sequential transfer																					

9.1.54 TMPHYS: Temp.Hysteresis Set for Frame Freq. Adj.(F3H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	1	0	0	1	1	F3H
1st parameter	1	1	0	-	-	-	-	TH3	TH2	TH1	TH0	

Description	Temp. hysteresis range set for frame freq. adj. Parameter TH[3:0] is used to set Temp. hysteresis range. The relationship between temp. state and temp. range value is shown below. <table><tr><td>TEMP Range Value</td><td>TEMP Rising State</td><td>TEMP Falling State</td></tr><tr><td>Freq. changing point A</td><td>TA[6:0]+TH[3:0]</td><td>TA[6:0]</td></tr><tr><td>Freq. changing point B</td><td>TB[6:0]+TH[3:0]</td><td>TB[6:0]</td></tr><tr><td>Freq. changing point C</td><td>TC[6:0]+TH[3:0]</td><td>TC[6:0]</td></tr></table> TH Temperature(℃) - 1 = TH[3:0] Example: If TH wants to set 5℃, TH[3:0]=5-1=4.		TEMP Range Value	TEMP Rising State	TEMP Falling State	Freq. changing point A	TA[6:0]+TH[3:0]	TA[6:0]	Freq. changing point B	TB[6:0]+TH[3:0]	TB[6:0]	Freq. changing point C	TC[6:0]+TH[3:0]	TC[6:0]
TEMP Range Value	TEMP Rising State	TEMP Falling State												
Freq. changing point A	TA[6:0]+TH[3:0]	TA[6:0]												
Freq. changing point B	TB[6:0]+TH[3:0]	TB[6:0]												
Freq. changing point C	TC[6:0]+TH[3:0]	TC[6:0]												
Restriction	Temp. hysteresis value should be smaller than the gap of temp. range.													
Register Availability	<table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table><tr><td>Status</td><td>Default Value(TH[3:0])</td></tr><tr><td>Power On Sequence</td><td>04h</td></tr><tr><td>S/W Reset</td><td>04h</td></tr><tr><td>H/W Reset</td><td>04h</td></tr></table>		Status	Default Value(TH[3:0])	Power On Sequence	04h	S/W Reset	04h	H/W Reset	04h				
Status	Default Value(TH[3:0])													
Power On Sequence	04h													
S/W Reset	04h													
H/W Reset	04h													
Flow Chart	TMPRNG ↓ 1st parameter. TA[6:0] 2nd parameter. TB[6:0] 3rd parameter. TC[6:0] ↓ TMPHYS ↓ 1st parameter. TH[3:0] Legend Command Parameter Display Action Mode Sequential transfer													

9.1.55 TEMPSEL: Temp. Set(F4H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
TEMPSEL	0	1	0	1	1	1	1	0	1	0	0	(F4h)
1 st parameter	1	1	0	MT13	MT12	MT11	MT10	MT03	MT02	MT01	MT00	MT1x: (-24 °C to -32 °C) MT0x: (-32 °C to -40 °C)
2 nd parameter	1	1	0	MT33	MT32	MT31	MT30	MT23	MT22	MT21	MT20	MT3x: (-8 °C to -16 °C) MT2x: (-16 °C to -24 °C)
3 rd parameter	1	1	0	MT53	MT52	MT51	MT50	MT43	MT42	MT41	MT40	MT5x: (8 °C to 0 °C) MT4x: (0 °C to -8 °C)
4 th parameter	1	1	0	MT73	MT72	MT71	MT70	MT63	MT62	MT61	MT60	MT7x: (24 °C to 16 °C) MT6x: (16 °C to 8 °C)
5 th parameter	1	1	0	MT93	MT92	MT91	MT90	MT83	MT82	MT81	MT80	MT9x: (40 °C to 32 °C) MT8x: (32 °C to 24 °C)
6 th parameter	1	1	0	MTB3	MTB2	MTB1	MTB0	MTA3	MTA2	MTA1	MTA0	MTBx: (56 °C to 48 °C) MTAx: (48 °C to 40 °C)
7 th parameter	1	1	0	MTD3	MTD2	MTD1	MTD0	MTC3	MTC2	MTC1	MTC0	MTDx: (72 °C to 64 °C) MTCx: (64 °C to 56 °C)
8 th parameter	1	1	0	MTF3	MTF2	MTF1	MTF0	MTE3	MTE2	MTE1	MTE0	MTFx: (87 °C to 80 °C) MTEx: (80 °C to 72 °C)

NOTE: “-“ Don’t care

Description	This command defines temperature gradient compensation coefficient. For this command detail description and operation, please see Figure 7.8.					
	Parameter n	MT n 3	MT n 2	MT n 1	MT n 0	Voltage / °C
	0	0	0	0	0	5 mv / °C
	1	0	0	0	1	0 mv / °C
	2	0	0	1	0	-5 mv / °C
	3	0	0	1	1	-10 mv / °C
	:	:	:	:	:	:
	:	:	:	:	:	:
	:	:	:	:	:	:
	12	1	1	0	0	-55 mv / °C
	13	1	1	0	1	-60 mv / °C
	14	1	1	1	0	-65 mv / °C
	15	1	1	1	1	-70 mv / °C
	Voltage/°C (+/- 5mV tolerance)					
Restriction	Please refer to the absolute maximum ratings for operating temperature range					
Register Availability	Status					Availability
	Normal Mode On, Idle Mode Off, Sleep Out					Yes
	Normal Mode On, Idle Mode On, Sleep Out					Yes
	Partial Mode On, Idle Mode Off, Sleep Out					Yes
	Partial Mode On, Idle Mode On, Sleep Out					Yes
	Sleep In					Yes

Default	Status	Default Value (MTn[3:0])	
	Power On Sequence	1 st parameter : FFh	
	S/W Reset	2 nd parameter : 36h	
	H/W Reset	3 rd parameter : 04h	
		4 th parameter : 00h	
Flow Chart		5 th parameter : 33h	
		6 th parameter : 42h	
		7 th parameter : C4h	
		8 th parameter : 59h	

The flow chart illustrates the relationship between the TEMPSEL command and the MTn[3:0] parameter. TEMPSEL is represented by a trapezoid (Command), and MTn[3:0] is represented by a parallelogram (Parameter). An arrow points from TEMPSEL to MTn[3:0]. A legend on the right defines the symbols used in the flow chart.

Legend

- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer

9.1.56 THYS : Temperature detection threshold(F7H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
THYS	0	1	0	1	1	1	1	0	1	1	1	(F7h)
Parameter	1	1	0	THYS7	THYS6	THYS5	THYS4	THYS3	THYS2	THYS1	THYS0	-

NOTE: “-“ Don’t care

Description	Temperature detection threshold setting.	
Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value D[7:0]
	Power On Sequence	06h
	S/W Reset	06h
	H/W Reset	06h
Flow Chart	THYS D[7:0] Legend Command Parameter Display Action Mode Sequential transfer	

9.1.57 Frame Set: Frame PWM Set (F9H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Frame Set	0	1	0	1	1	1	1	1	0	0	1	(F9h)
1 st parameter	1	1	0	-	-	-	P14	P13	P12	P11	P10	-
2 nd parameter	1	1	0	-	-	-	P24	P23	P22	P21	P20	-
:	:	:	:	:	:	:	:	:	:	:	:	-
15 th parameter	1	1	0	-	-	-	P154	P153	P152	P151	P150	-
16 th parameter	1	1	0	-	-	-	P164	P163	P162	P161	P160	-

NOTE: “-“ Don't care

Description	This command is used to set frame PWM.		
Restriction			
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value	
	Power On Sequence	Refer to the table on next page.	
	S/W Reset	Refer to the table on next page.	
	H/W Reset	Refer to the table on next page.	
Flow Chart	Frame Set 1st ~ 16th parameters Legend Command Parameter Display Action Mode Sequential transfer		

NOTE:

The default value of RGB level set

	RGB SET
RGB level0	00
RGB level1	01
RGB level2	02
RGB level3	04
RGB level4	06
RGB level5	07
RGB level6	09
RGB level7	0A
RGB level8	0B
RGB level9	0C
RGB level10	0D
RGB level11	0F
RGB level12	11
RGB level13	12
RGB level14	17
RGB level15	1A

All the modulation range of each level for each frame is from 00'H to 1F'H.

10. SPECIFICATIONS**10.1 ABSOLUTE MAXIMUM RATINGS**(V_{SS} = 0V)

Item	Symbol	Value	Unit
Supply voltage (1)	VDD, VDD1	- 0.3 ~ + 3.0	V
Supply voltage (1)	VDD2, VDD3, VDD4, VDD5	- 0.3 ~ + 3.6	V
Supply voltage (2)	VLCD (V0-VSS)	- 0.3 ~ + 18.0	V
Supply voltage (3)	VmAX (V0- XV0)	- 0.3 ~ + 18.0	V
Input voltage range	VIN	- 0.3 ~ VDD + 0.3	V
Output voltage range	VO	- 0.3 ~ VDD + 0.3	V
Operating temperature range	TOPR	- 30 ~ + 85	°C
Storage temperature range	TSTG	- 40 ~ + 125	°C

NOTE:

1. Voltages are all based on VSS = 0V.
2. Voltage relationship: V0. Vg. Vm. VSS. XV0 must always be satisfied.
3. External V0,XV0

10.2DC CHARACTERISTICS

10.2.1 Basic Characteristics

(V_{SS}=0V, T_a = -30 to 85°C)

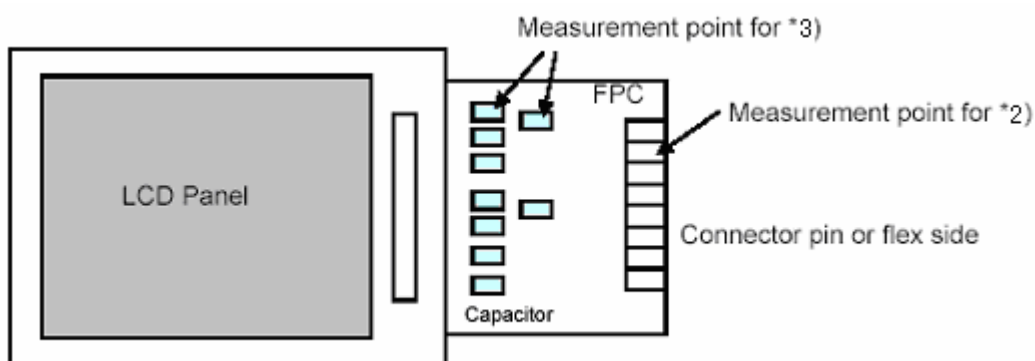
Parameter	Symbol	Conditions	Related Pins	MIN	TYP	MAX	Unit
Logic Operating voltage	V _{DDI}	-	*2) VDD, VDD1	1.65	1.8	3.0	V
Analog Operating voltage	V _{DDA}	-	*2) VDD2,3,4,5	2.4	2.75	3.3	
Driving voltage input	V _{LCD}	V ₀ – X _{V0}	*3) V ₀ , X _{V0}	-	-	18.0	
High level input voltage	V _{IH}		*1) *2)	0.7V _{DD}	-	V _{DD}	
Low level input voltage	V _{IL}	-	*1) *2)	V _{SS}	-	0.3V _{DD}	
High level output voltage	V _{OH}	I _{OH} = -1.0mA	*2) SI	0.8V _{DD}	-	V _{DD}	
Low level output voltage	V _{OL}	I _{OL} = +1.0mA		V _{SS}	-	0.2V _{DD}	
Input leakage current	I _{IL}	V _{IN} = V _{DD} or V _{SS}	*1), *2)	-1.0	-	+1.0	μA
Driver on resistance (SEG)	R _{ONSEG}	V _g = 2.4V, T _a = 25°C, ΔV=10%	S ₀ to S ₃₀₅	-	0.7		KΩ
Driver on resistance (COM)	R _{ONCOM}	V ₀ = 12.0V, T _a = 25°C, ΔV=10%	C ₀ to C ₉₅	-	0.5		
Frame Rate	FR	T _a =25°C, N-line=0x00, Duty=96, FR=0x12		-	77	-	Hz

NOTE:

*1) Applies to IF1, IF2, IF3, /CS, /RST, /WR, /RD, A0(SCL) and

D15-D2, D1 (A0), D0(SI) pins

*2) *3) When the measurements are performed with LCD module, Measurement Points are like below.



10.2.2 Current Consumption (Bare Die)

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern Normal	ISS	VDDI=1.8V, VDDA=2.8V, Vop=11V, Booster=8X, BIAS=1/9, Booster efficiency=01, Ta = 25°C.	—	500	—	μA	
Power Down	ISS		—	10	25	μA	

Note:

The Current Consumption is DC characteristics.

11. TIMING CHARACTERISTICS

11.1 Parallel Interface Characteristics bus (8080-series MCU)

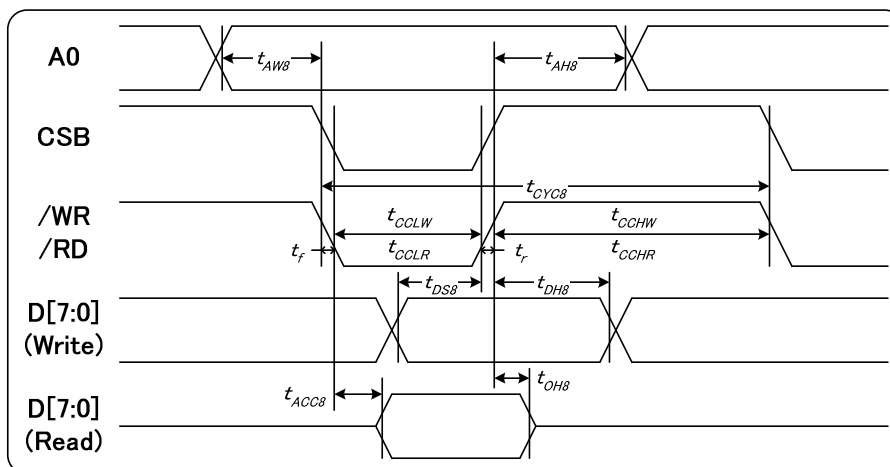


Figure 11.1 Parallel Interface Characteristics bus(8080-series MCU)

($V_{DD}=2.8V$, $T_a= 25^{\circ}C$, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		10	—	ns
Address setup time		tAW8		15	—	
System cycle time (WRITE)	WR	tCYC8		145	—	
/WR L pulse width (WRITE)		tCCLW		55	—	
/WR H pulse width (WRITE)		tCCHW		90	—	
System cycle time (READ)	RD (FM)	tCYC8	When read from frame memory	175	—	
/RD L pulse width (READ)		tCCLR		55	—	
/RD H pulse width (READ)		tCCHR		120	—	
WRITE data setup time	D0 to D7	tDS8		50	—	
WRITE data hold time		tDH8		10	—	
READ access time		tACC8	CL = 16 pF	—	45	
READ Output disable time		tOH8	CL = 16 pF	—	35	

(V_{DD}=1.8V, T_a= 25°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		10	—	ns
Address setup time		tAW8		20	—	
System cycle time (WRITE)	WR	tCYC8		245	—	
/WR L pulse width (WRITE)		tCCLW		100	—	
/WR H pulse width (WRITE)		tCCHW		145	—	
System cycle time (READ)	RD (FM)	tCYC8	When read from frame memory	250	—	
/RD L pulse width (READ)		tCCLR		70	—	
/RD H pulse width (READ)		tCCHR		180	—	
WRITE data setup time	D0 to D7	tDS8		70	—	
WRITE data hold time		tDH8		20	—	
READ access time		tACC8	CL = 16 pF	—	60	
READ Output disable time		tOH8	CL = 16 pF	—	40	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≤ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≤ (tCYC8 – tCCLR – tCCHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tCCLW and tCCLR are specified as the overlap between /CS being “L” and WR and RD being at the “L” level.

11.2 Parallel Interface Characteristics bus (6800-series MCU)

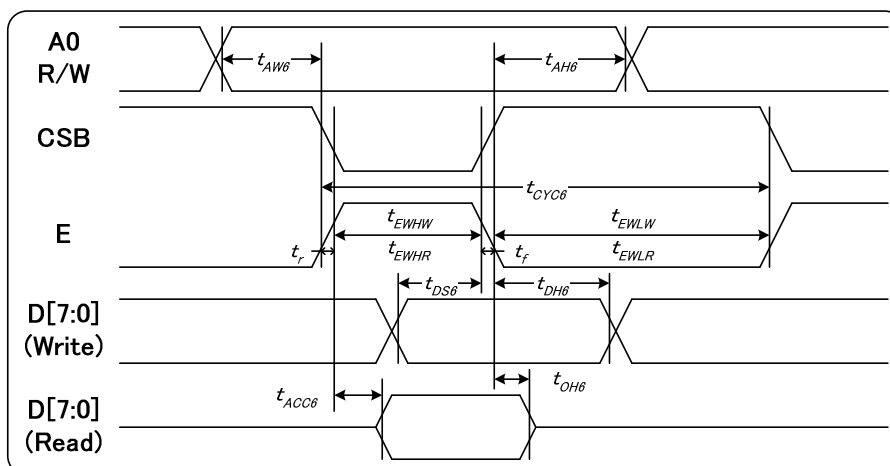


Figure 11.2 Parallel Interface characteristics (6800-Series MCU)

(V_{DD}=2.8V, T_a= 25°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		10	—	ns
Address setup time		tAW6		20	—	
System cycle time (WRITE)	E	tCYC6		155	—	
/WR L pulse width (WRITE)		tEWHW		95	—	
/WR H pulse width (WRITE)		tEWLW		60	—	
System cycle time (READ)	RD (FM)	tCYC6	When read from frame memory	175	—	
/RD L pulse width (READ)		tEWHR		110	—	
/RD H pulse width (READ)		tEWHR		65	—	
WRITE data setup time	D0 to D7	tDS6		50	—	
WRITE data hold time		tDH6		10	—	
READ access time		tACC8	CL = 16 pF	—	55	
READ Output disable time		tOH8	CL = 16 pF	—	50	

(V_{DD}=1.8V, T_a= 25°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		15	—	ns
Address setup time		tAW6		20	—	
System cycle time (WRITE)	E	tCYC6		210	—	
/WR L pulse width (WRITE)		tEWHW		130	—	
/WR H pulse width (WRITE)		tEWLW		80	—	
System cycle time (READ)	RD (FM)	tCYC6	When read from frame memory	300	—	
/RD L pulse width (READ)		tEWHR		200	—	
/RD H pulse width (READ)		tEWHR		100	—	
WRITE data setup time	D0 to D7	tDS6		55	—	
WRITE data hold time		tDH6		10	—	
READ access time		tACC8	CL = 16 pF	—	100	
READ Output disable time		tOH8	CL = 16 pF	—	80	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≤ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≤ (tCYC6 – tEWLR – tEWHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tEWLW and tEWLR are specified as the overlap between /CS being “L” and E.

11.3 Serial Interface Characteristics (3-pin Serial)

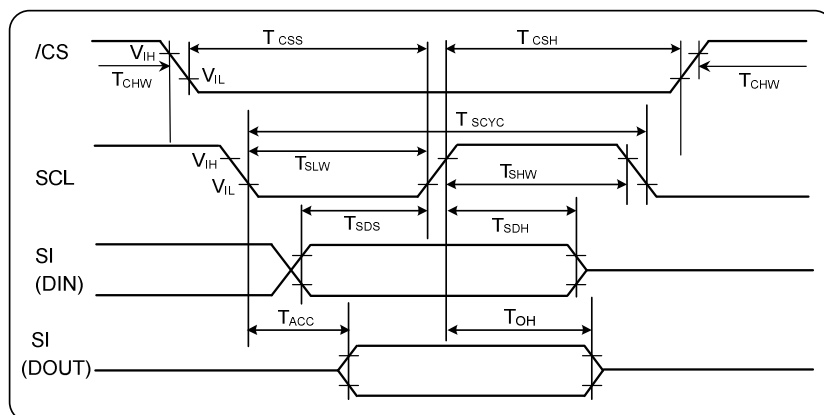


Figure 11.3 3-pin Serial Interface Characteristics

($V_{DD}=2.8V$, $T_a=25^{\circ}C$, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period (write)	SCL	tSCYCW		80	—	ns
SCL "H" pulse width (write)		tSHW		25	—	
SCL "L" pulse width (write)		tSLW		25	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		20	—	
READ access time		tACC	CL = 16 pF	—	70	
READ Output disable time		tOH	CL = 16 pF	—	70	
CS-SCL time	/CS	tCSS		25	—	
CS-SCL time		tCSH		25	—	

(V_{DD}=1.8V, T_a= 25°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period (write)	SCL	tSCYCW		100	—	ns
SCL "H" pulse width (write)		tSHW		35	—	
SCL "L" pulse width (write)		tSLW		35	—	
Data setup time	SI	tSDS		30	—	
Data hold time		tSDH		30	—	
READ access time		tACC	CL = 16 pF	—	90	
READ Output disable time		tOH	CL = 16 pF	—	70	
CS-SCL time	/CS	tCSS		35	—	
CS-SCL time		tCSH		35	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

11.4 Serial Interface Characteristics (4-pin Serial)

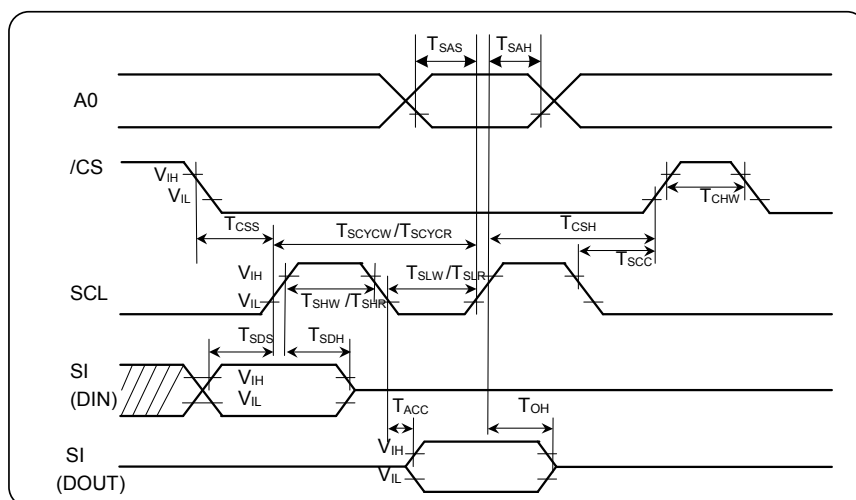


Figure 11.4 4-pin Serial Interface Characteristics

(V_{DD}=2.8V, T_a= 25°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period (write)	SCL	tSCYCW		80	—	ns
SCL "H" pulse width (write)		tSHW		25	—	
SCL "L" pulse width (write)		tSLW		25	—	
Address setup time	A0	tSAS		15	—	
Address hold time		tSAH		20	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		20	—	
READ access time		tACC	CL = 16 pF	—	70	
READ Output disable time		tOH	CL = 16 pF	—	50	
CS-SCL time	/CS	tCSS		25	—	
CS-SCL time		tCSH		25	—	

(V_{DD}=1.8V, Ta=25°C, die)

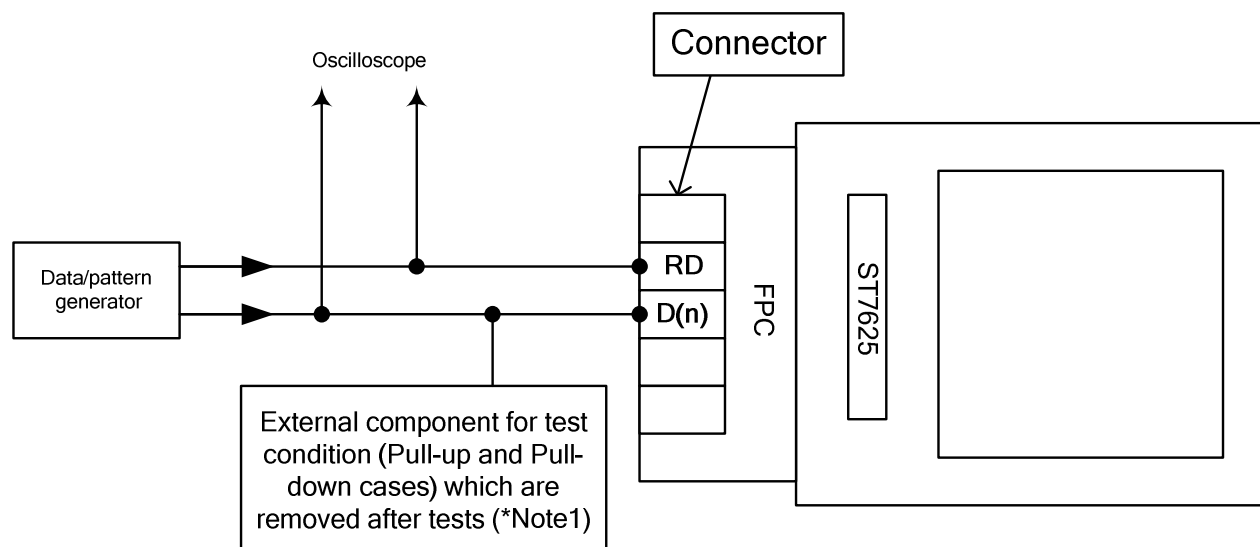
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period (write)	SCL	tSCYCW		100	—	ns
SCL "H" pulse width (write)		tSHW		35	—	
SCL "L" pulse width (write)		tSLW		35	—	
Address setup time	A0	tSAS		25	—	
Address hold time		tSAH		30	—	
Data setup time	SI	tSDS		30	—	
Data hold time		tSDH		30	—	
READ access time		tACC	CL = 16 pF	—	90	
READ Output disable time		tOH	CL = 16 pF	—	70	
CS-SCL time	/CS	tCSS		35	—	
CS-SCL time		tCSH		35	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

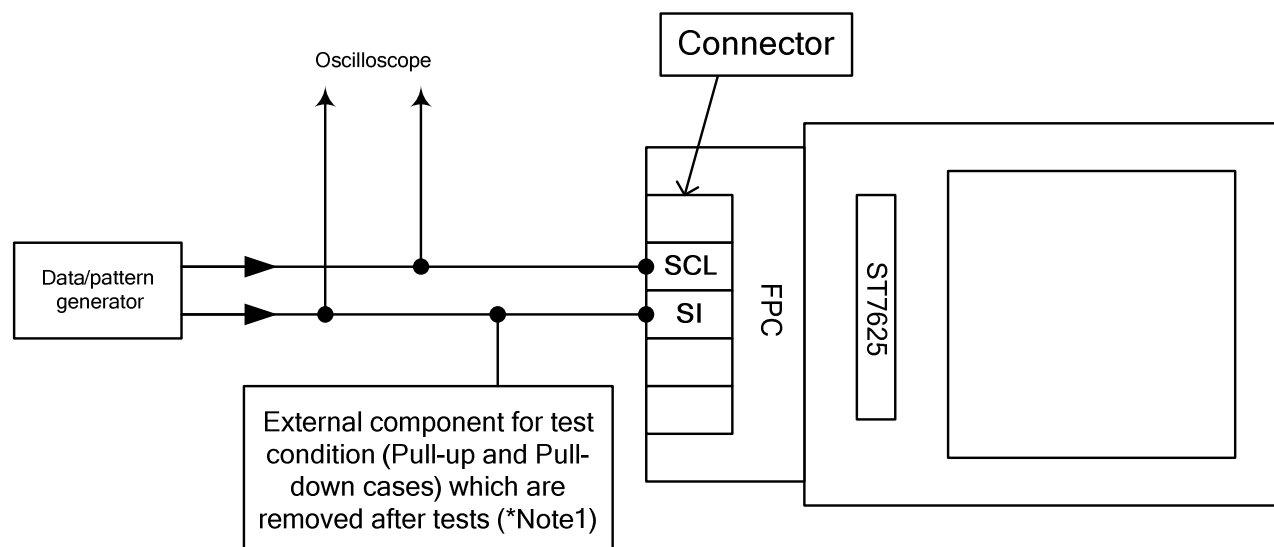
*2 All timing is specified using 20% and 80% of VDD as the standard.

11.5 Output access/disable timing measurement method

◆ Parallel interface (8080-series)



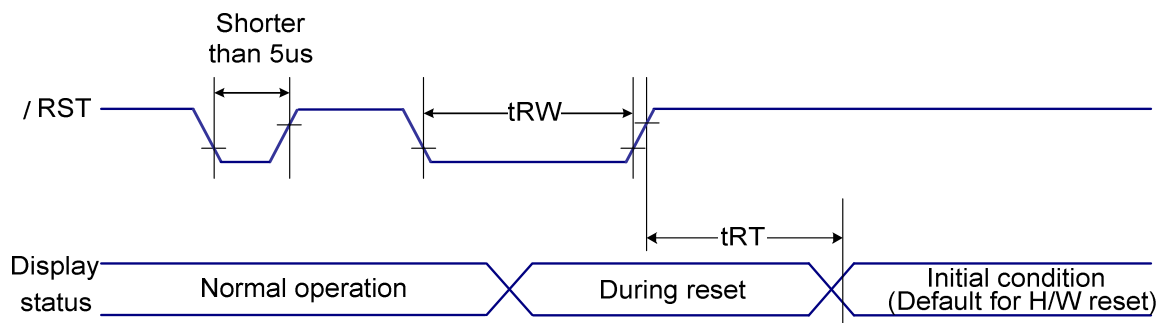
◆ Serial interface (3-line)



Note:

1. pull-up/pull-down resistor: $3K\Omega \pm 5\%$; pull-up/pull-down capacitor: $16pF \pm 10\%$
2. Capacitances and resistances of the oscilloscope's probe must be included external components in these measurements.

12. RESET TIMING



(VSS=0V, VDDI=1.65V to 3.0V, VDDA=2.4V to 3.3V, Ta =25°C)

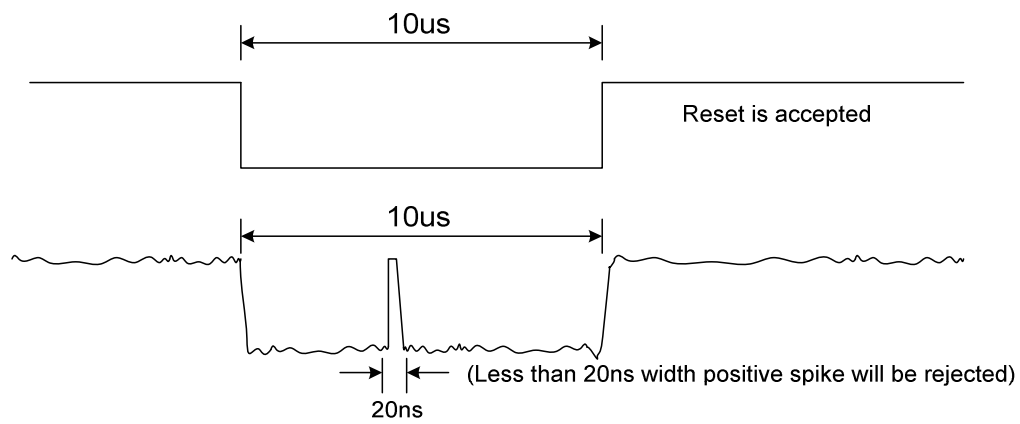
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Reset "L" pulse width	/RST	tRW		10	—	us
Reset time		tRT		—	5 (*note 5)	ms
				—	120 (*note 6,7)	ms

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from EEPROM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of /RST
2. Spike due to an electrostatic discharge on /RST line does not cause irregular system reset according to the table below:

/RST Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 9μs	Reset
Between 5μs and 9μs	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



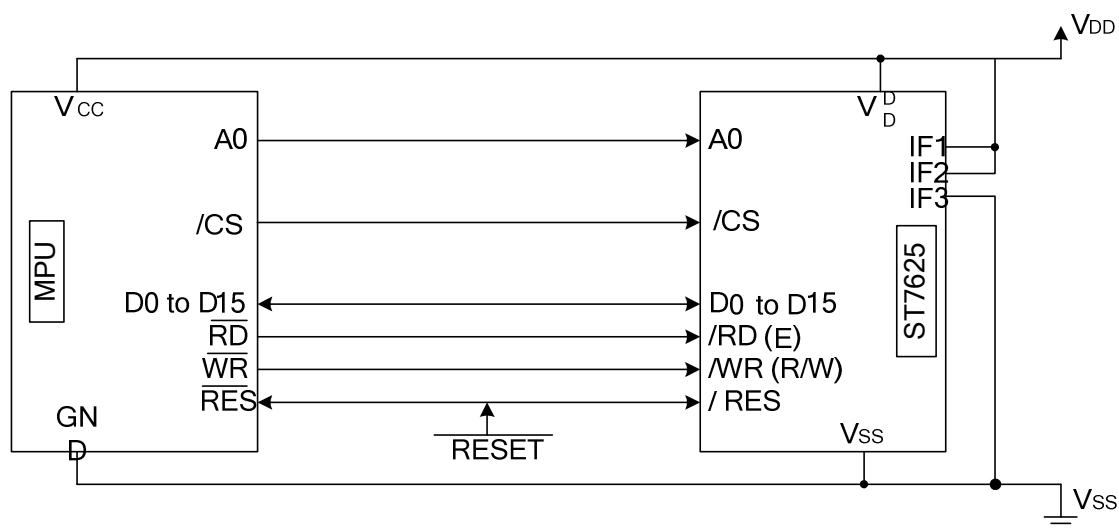
5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 120msec after releasing RST before sending commands. Also Sleep Out command cannot be sent for 120msec.

13. THE MPU INTERFACE (REFERENCE EXAMPLES)

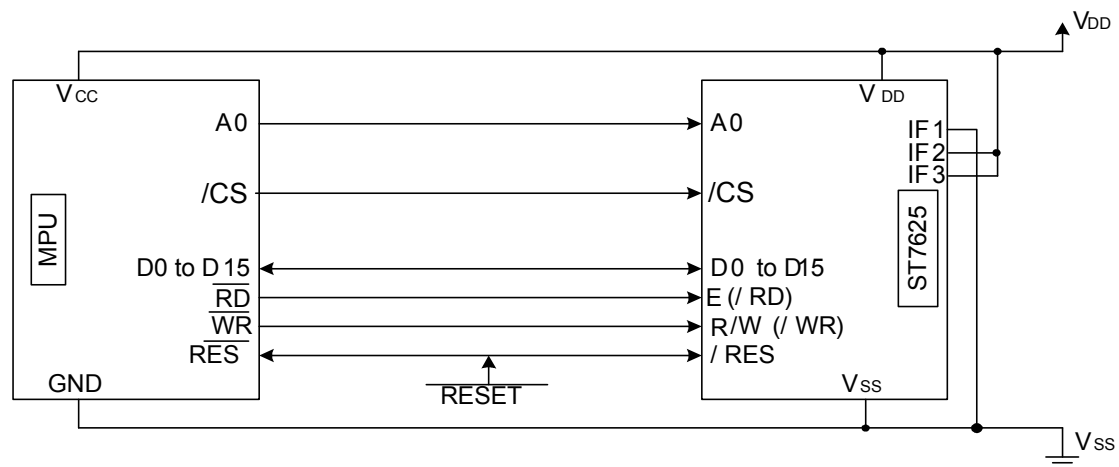
The ST7625 Series can be connected to either 8080 Series MPUs or to 6800 Series MPUs. Moreover, using the serial interface it is possible to operate the ST7625 series chips with fewer signal lines.

The display area can be enlarged by using multiple ST7625 Series chips. When this is done, the chip select signal can be used to select the individual ICs to access.

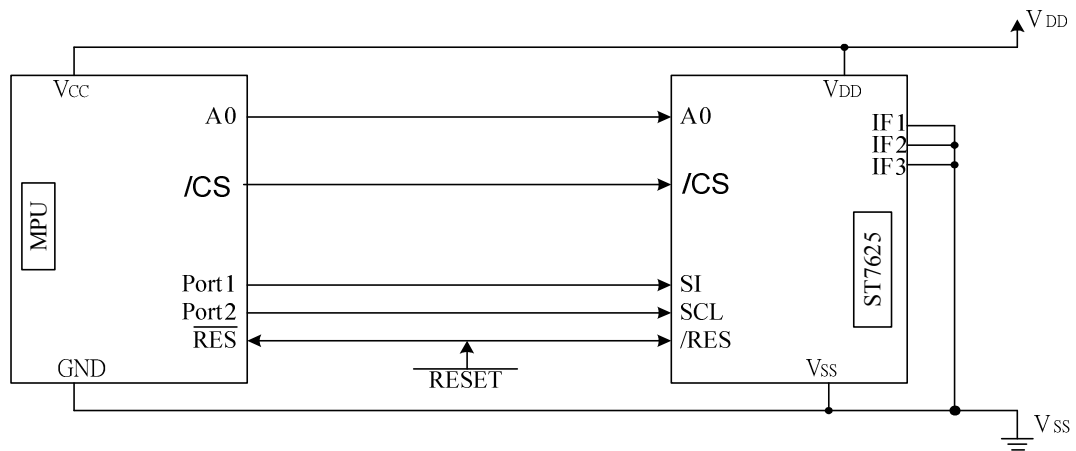
(1) 8080 Series MPUs



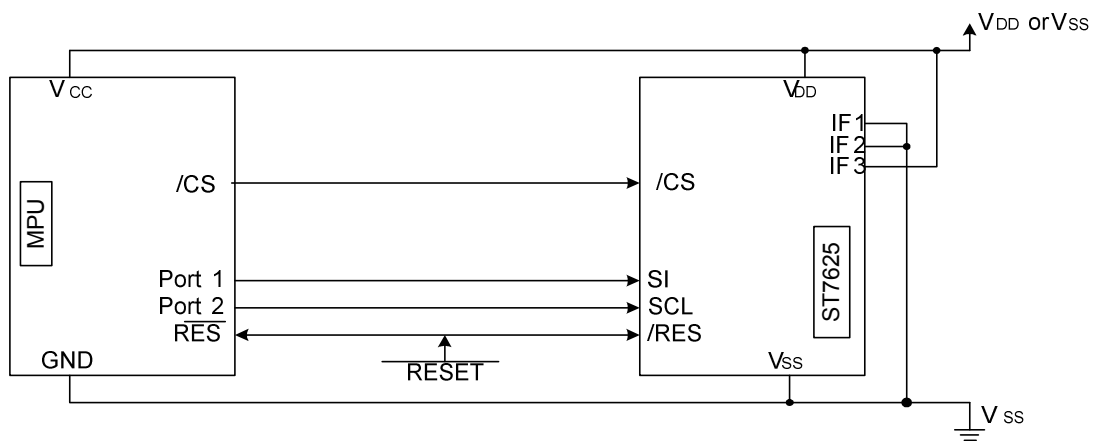
(2) 6800 Series MPUs



(3) Using the Serial Interface (4-line interface)



(4) Using the Serial Interface (3-line interface)



The diagram illustrates the internal structure of the ST7625 microcontroller, showing its connections to various components and power sources.

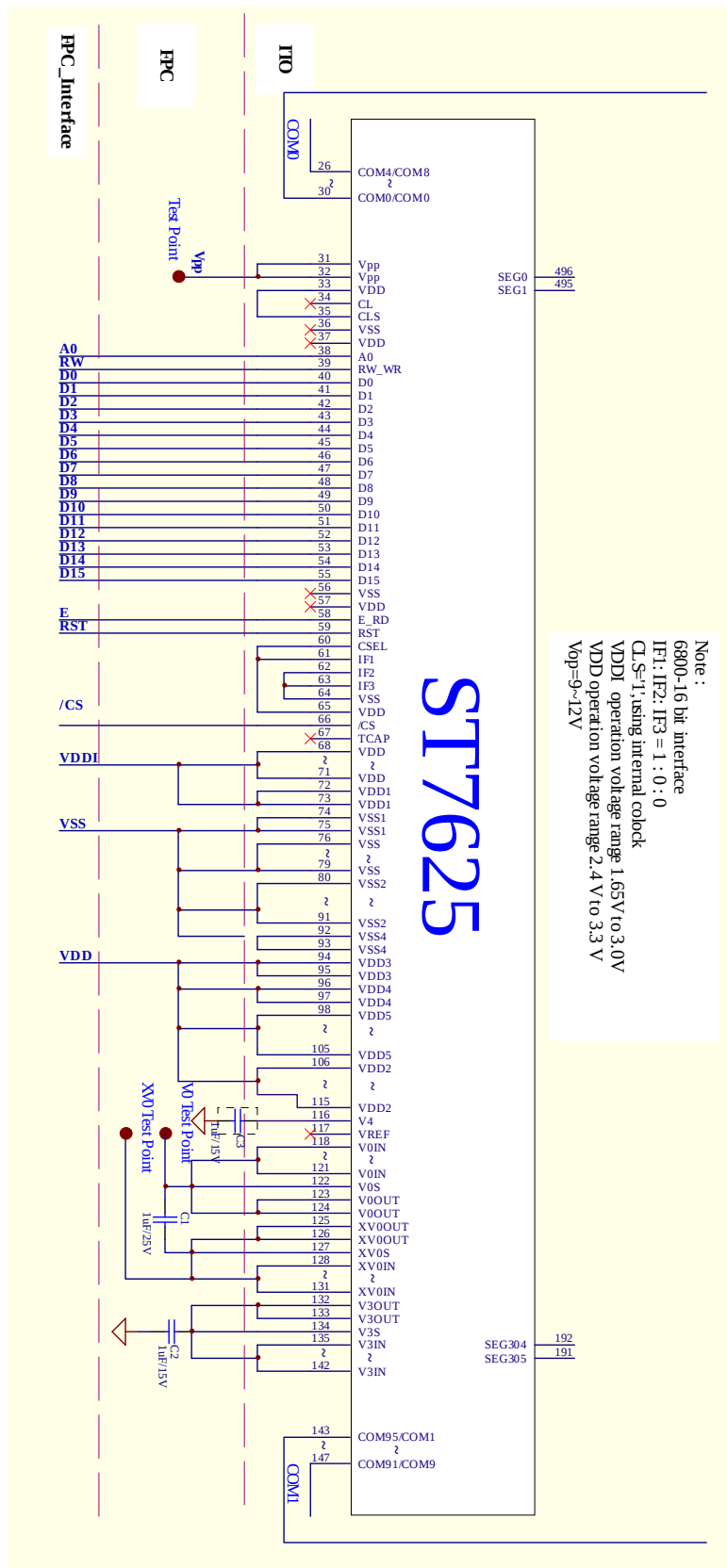
Microcontroller Pins and Connections:

- COM0/COM1:** Pins 26 and 30 are connected to COM0/COM1.
- COM2/COM3:** Pins 31 and 32 are connected to COM2/COM3.
- COM4/COM5:** Pins 33 and 34 are connected to COM4/COM5.
- COM6/COM7:** Pins 35 and 36 are connected to COM6/COM7.
- COM8/COM9:** Pins 37 and 38 are connected to COM8/COM9.
- COM10/COM11:** Pins 39 and 40 are connected to COM10/COM11.
- COM12/COM13:** Pins 41 and 42 are connected to COM12/COM13.
- COM14/COM15:** Pins 43 and 44 are connected to COM14/COM15.
- COM16/COM17:** Pins 45 and 46 are connected to COM16/COM17.
- COM18/COM19:** Pins 47 and 48 are connected to COM18/COM19.
- COM20/COM21:** Pins 49 and 50 are connected to COM20/COM21.
- COM22/COM23:** Pins 51 and 52 are connected to COM22/COM23.
- COM24/COM25:** Pins 53 and 54 are connected to COM24/COM25.
- COM26/COM27:** Pins 55 and 56 are connected to COM26/COM27.
- COM28/COM29:** Pins 57 and 58 are connected to COM28/COM29.
- COM30/COM31:** Pins 59 and 60 are connected to COM30/COM31.
- COM32/COM33:** Pins 61 and 62 are connected to COM32/COM33.
- COM34/COM35:** Pins 63 and 64 are connected to COM34/COM35.
- COM36/COM37:** Pins 65 and 66 are connected to COM36/COM37.
- COM38/COM39:** Pins 67 and 68 are connected to COM38/COM39.
- COM40/COM41:** Pins 69 and 70 are connected to COM40/COM41.
- COM42/COM43:** Pins 71 and 72 are connected to COM42/COM43.
- COM44/COM45:** Pins 73 and 74 are connected to COM44/COM45.
- COM46/COM47:** Pins 75 and 76 are connected to COM46/COM47.
- COM48/COM49:** Pins 77 and 78 are connected to COM48/COM49.
- COM50/COM51:** Pins 79 and 80 are connected to COM50/COM51.
- COM52/COM53:** Pins 81 and 82 are connected to COM52/COM53.
- COM54/COM55:** Pins 83 and 84 are connected to COM54/COM55.
- COM56/COM57:** Pins 85 and 86 are connected to COM56/COM57.
- COM58/COM59:** Pins 87 and 88 are connected to COM58/COM59.
- COM60/COM61:** Pins 89 and 90 are connected to COM60/COM61.
- COM62/COM63:** Pins 91 and 92 are connected to COM62/COM63.
- COM64/COM65:** Pins 93 and 94 are connected to COM64/COM65.
- COM66/COM67:** Pins 95 and 96 are connected to COM66/COM67.
- COM68/COM69:** Pins 97 and 98 are connected to COM68/COM69.
- COM70/COM71:** Pins 99 and 100 are connected to COM70/COM71.
- COM72/COM73:** Pins 101 and 102 are connected to COM72/COM73.
- COM74/COM75:** Pins 103 and 104 are connected to COM74/COM75.
- COM76/COM77:** Pins 105 and 106 are connected to COM76/COM77.
- COM78/COM79:** Pins 107 and 108 are connected to COM78/COM79.
- COM80/COM81:** Pins 109 and 110 are connected to COM80/COM81.
- COM82/COM83:** Pins 111 and 112 are connected to COM82/COM83.
- COM84/COM85:** Pins 113 and 114 are connected to COM84/COM85.
- COM86/COM87:** Pins 115 and 116 are connected to COM86/COM87.
- COM88/COM89:** Pins 117 and 118 are connected to COM88/COM89.
- COM90/COM91:** Pins 119 and 120 are connected to COM90/COM91.
- COM92/COM93:** Pins 121 and 122 are connected to COM92/COM93.
- COM94/COM95:** Pins 123 and 124 are connected to COM94/COM95.
- COM96/COM97:** Pins 125 and 126 are connected to COM96/COM97.
- COM98/COM99:** Pins 127 and 128 are connected to COM98/COM99.
- COM100/COM101:** Pins 129 and 130 are connected to COM100/COM101.
- COM102/COM103:** Pins 131 and 132 are connected to COM102/COM103.
- COM104/COM105:** Pins 133 and 134 are connected to COM104/COM105.
- COM106/COM107:** Pins 135 and 136 are connected to COM106/COM107.
- COM108/COM109:** Pins 137 and 138 are connected to COM108/COM109.
- COM110/COM111:** Pins 139 and 140 are connected to COM110/COM111.
- COM112/COM113:** Pins 141 and 142 are connected to COM112/COM113.
- COM114/COM115:** Pins 143 and 144 are connected to COM114/COM115.
- COM116/COM117:** Pins 145 and 146 are connected to COM116/COM117.
- COM118/COM119:** Pins 147 and 148 are connected to COM118/COM119.
- COM120/COM121:** Pins 149 and 150 are connected to COM120/COM121.
- COM122/COM123:** Pins 151 and 152 are connected to COM122/COM123.
- COM124/COM125:** Pins 153 and 154 are connected to COM124/COM125.
- COM126/COM127:** Pins 155 and 156 are connected to COM126/COM127.
- COM128/COM129:** Pins 157 and 158 are connected to COM128/COM129.
- COM130/COM131:** Pins 159 and 160 are connected to COM130/COM131.
- COM132/COM133:** Pins 161 and 162 are connected to COM132/COM133.
- COM134/COM135:** Pins 163 and 164 are connected to COM134/COM135.
- COM136/COM137:** Pins 165 and 166 are connected to COM136/COM137.
- COM138/COM139:** Pins 167 and 168 are connected to COM138/COM139.
- COM140/COM141:** Pins 169 and 170 are connected to COM140/COM141.
- COM142/COM143:** Pins 171 and 172 are connected to COM142/COM143.
- COM144/COM145:** Pins 173 and 174 are connected to COM144/COM145.
- COM146/COM147:** Pins 175 and 176 are connected to COM146/COM147.
- COM148/COM149:** Pins 177 and 178 are connected to COM148/COM149.
- COM150/COM151:** Pins 179 and 180 are connected to COM150/COM151.
- COM152/COM153:** Pins 181 and 182 are connected to COM152/COM153.
- COM154/COM155:** Pins 183 and 184 are connected to COM154/COM155.
- COM156/COM157:** Pins 185 and 186 are connected to COM156/COM157.
- COM158/COM159:** Pins 187 and 188 are connected to COM158/COM159.
- COM160/COM161:** Pins 189 and 190 are connected to COM160/COM161.
- COM162/COM163:** Pins 191 and 192 are connected to COM162/COM163.
- COM164/COM165:** Pins 193 and 194 are connected to COM164/COM165.
- COM166/COM167:** Pins 195 and 196 are connected to COM166/COM167.
- COM168/COM169:** Pins 197 and 198 are connected to COM168/COM169.
- COM170/COM171:** Pins 199 and 200 are connected to COM170/COM171.
- COM172/COM173:** Pins 201 and 202 are connected to COM172/COM173.
- COM174/COM175:** Pins 203 and 204 are connected to COM174/COM175.
- COM176/COM177:** Pins 205 and 206 are connected to COM176/COM177.
- COM178/COM179:** Pins 207 and 208 are connected to COM178/COM179.
- COM180/COM181:** Pins 209 and 210 are connected to COM180/COM181.
- COM182/COM183:** Pins 211 and 212 are connected to COM182/COM183.
- COM184/COM185:** Pins 213 and 214 are connected to COM184/COM185.
- COM186/COM187:** Pins 215 and 216 are connected to COM186/COM187.
- COM188/COM189:** Pins 217 and 218 are connected to COM188/COM189.
- COM190/COM191:** Pins 219 and 220 are connected to COM190/COM191.
- COM192/COM193:** Pins 221 and 222 are connected to COM192/COM193.
- COM194/COM195:** Pins 223 and 224 are connected to COM194/COM195.
- COM196/COM197:** Pins 225 and 226 are connected to COM196/COM197.
- COM198/COM199:** Pins 227 and 228 are connected to COM198/COM199.
- COM200/COM201:** Pins 229 and 230 are connected to COM200/COM201.
- COM202/COM203:** Pins 231 and 232 are connected to COM202/COM203.
- COM204/COM205:** Pins 233 and 234 are connected

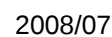
Note:
8080-16 bit interface
IE1: IF2: IF3 = 1 : 1 : 1
CLS=1, using internal clock
VDD1 operation voltage range 1.65V to 3.0V
VDD operation voltage range 2.4 V to 3.3 V
Vop=9~12V

A2 –6800-16bit / COM interlace Mode

6800-16 Bit
IF1:IF2:IF3=1:0:0



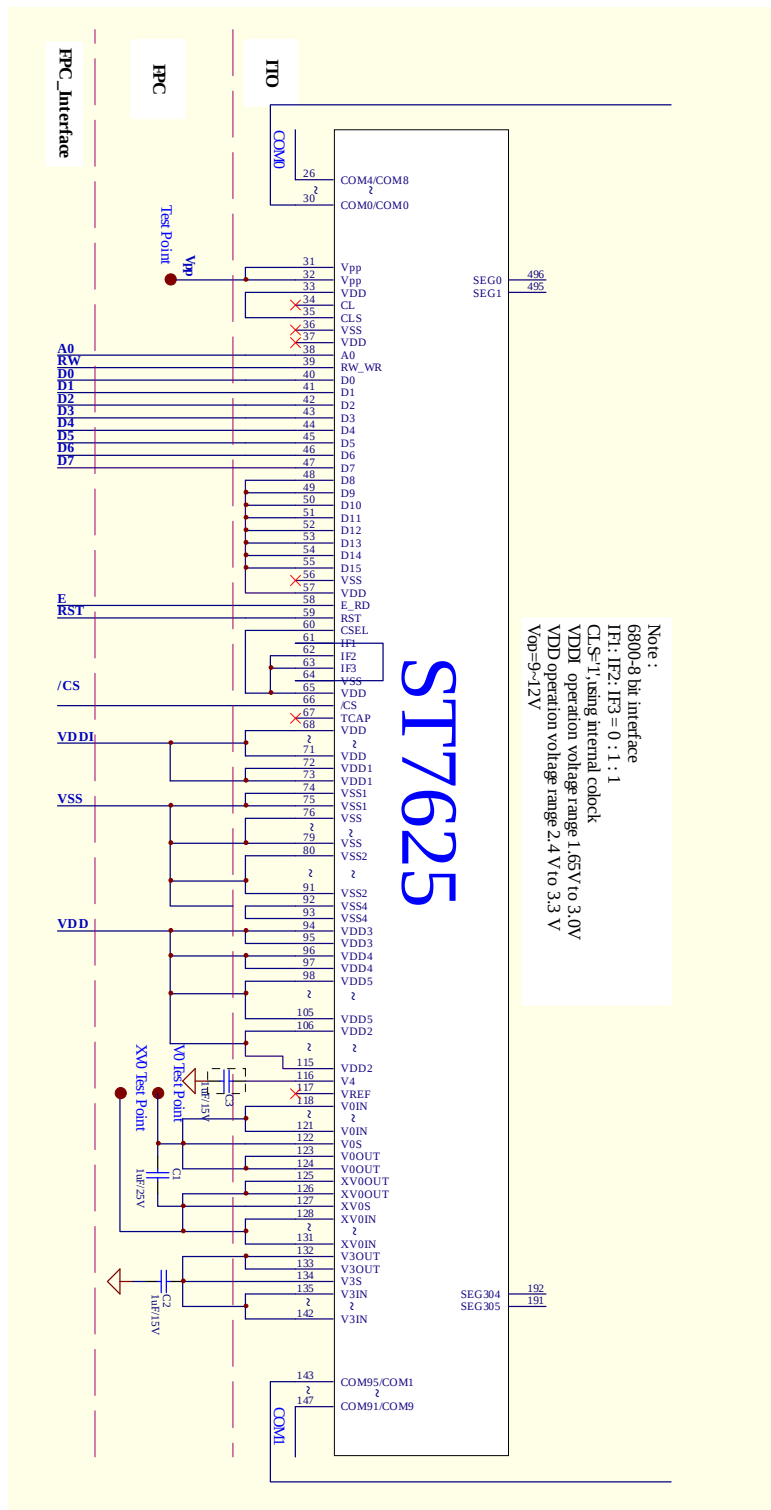
ST7625



A4 – 6800-8bit / COM interlace Mode

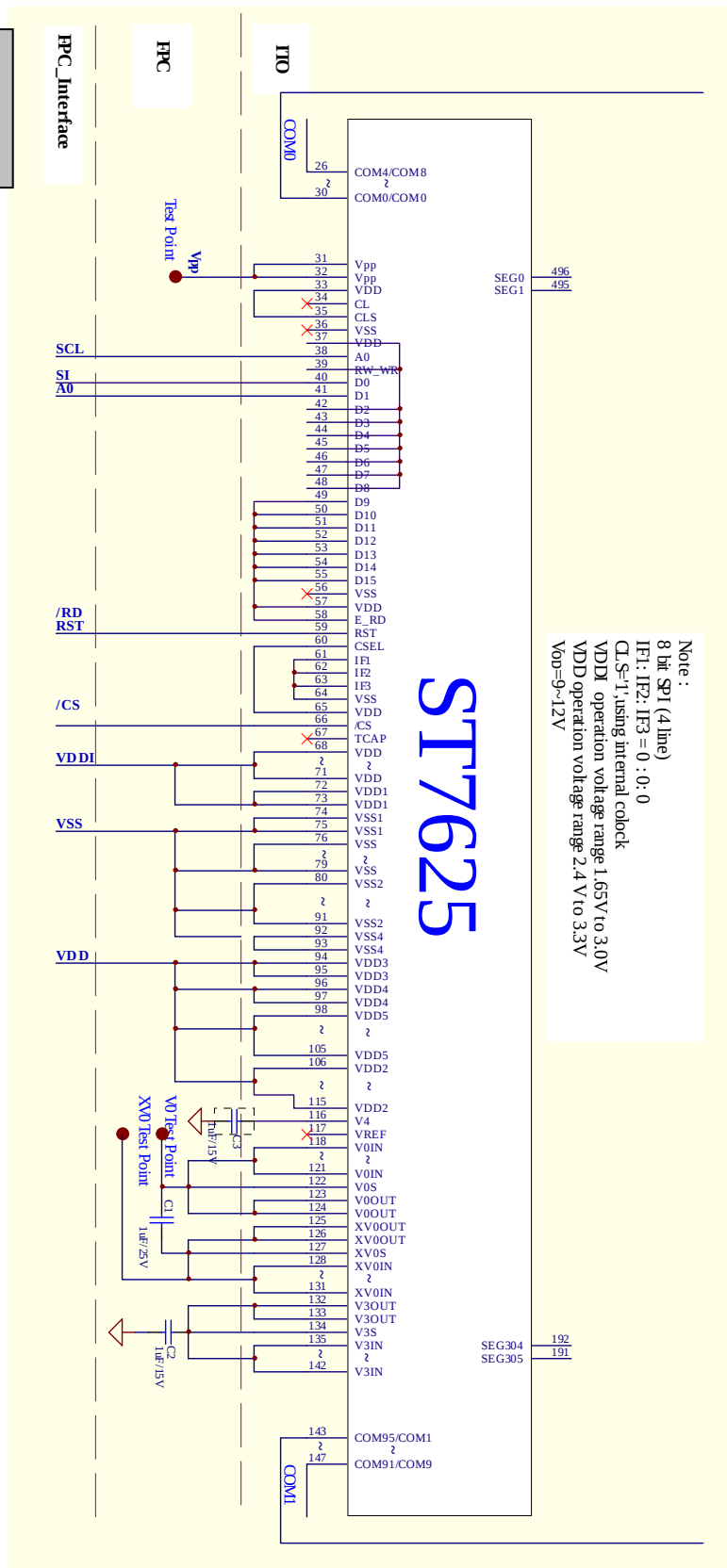
6800-8 Bit

IF1:IF2:IF3=0:1:1



A5 – 4L SPI / COM interface Mode

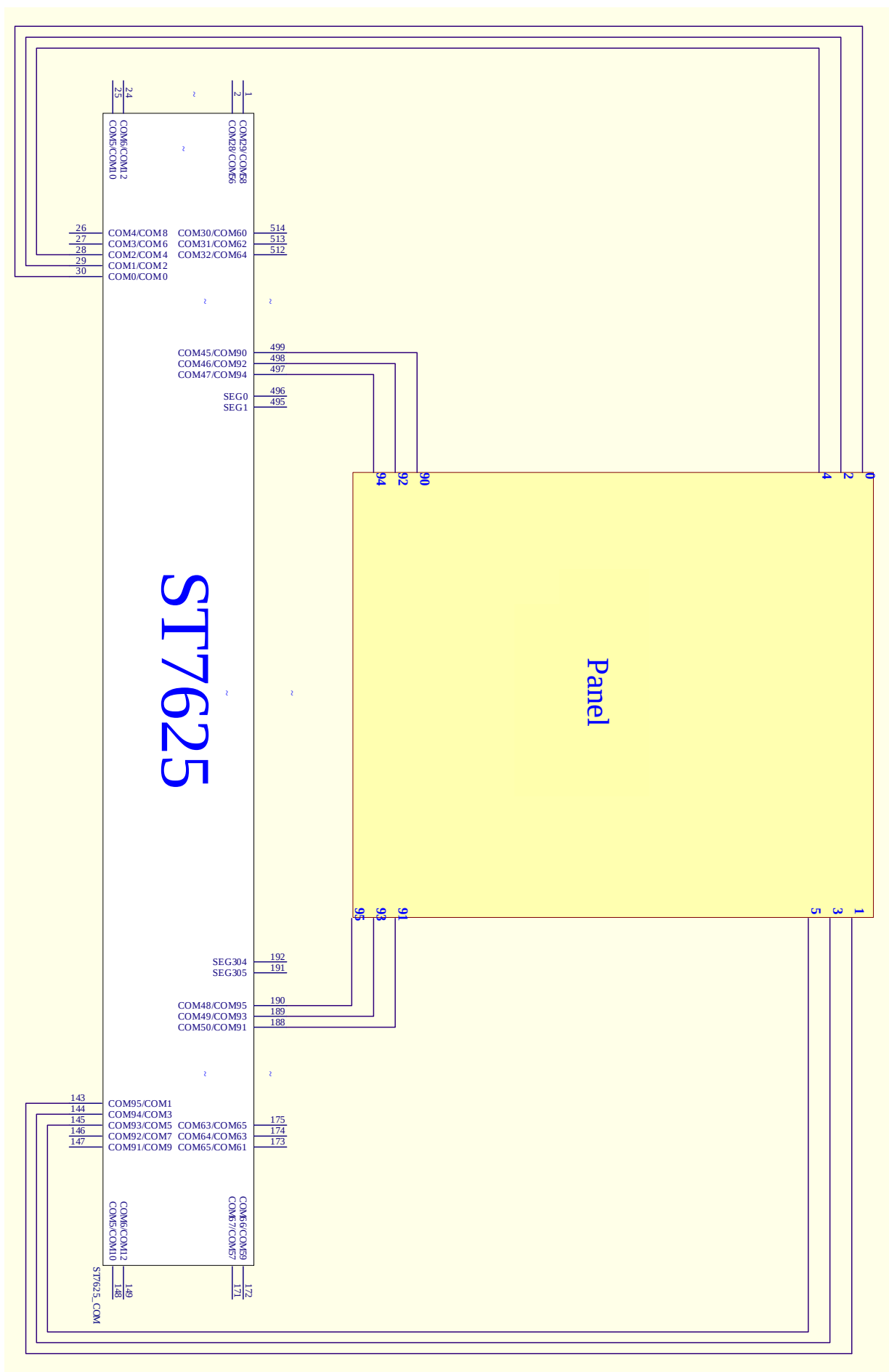
8 Bit 4SPI
IF1:IF2:IF3=0:0:1



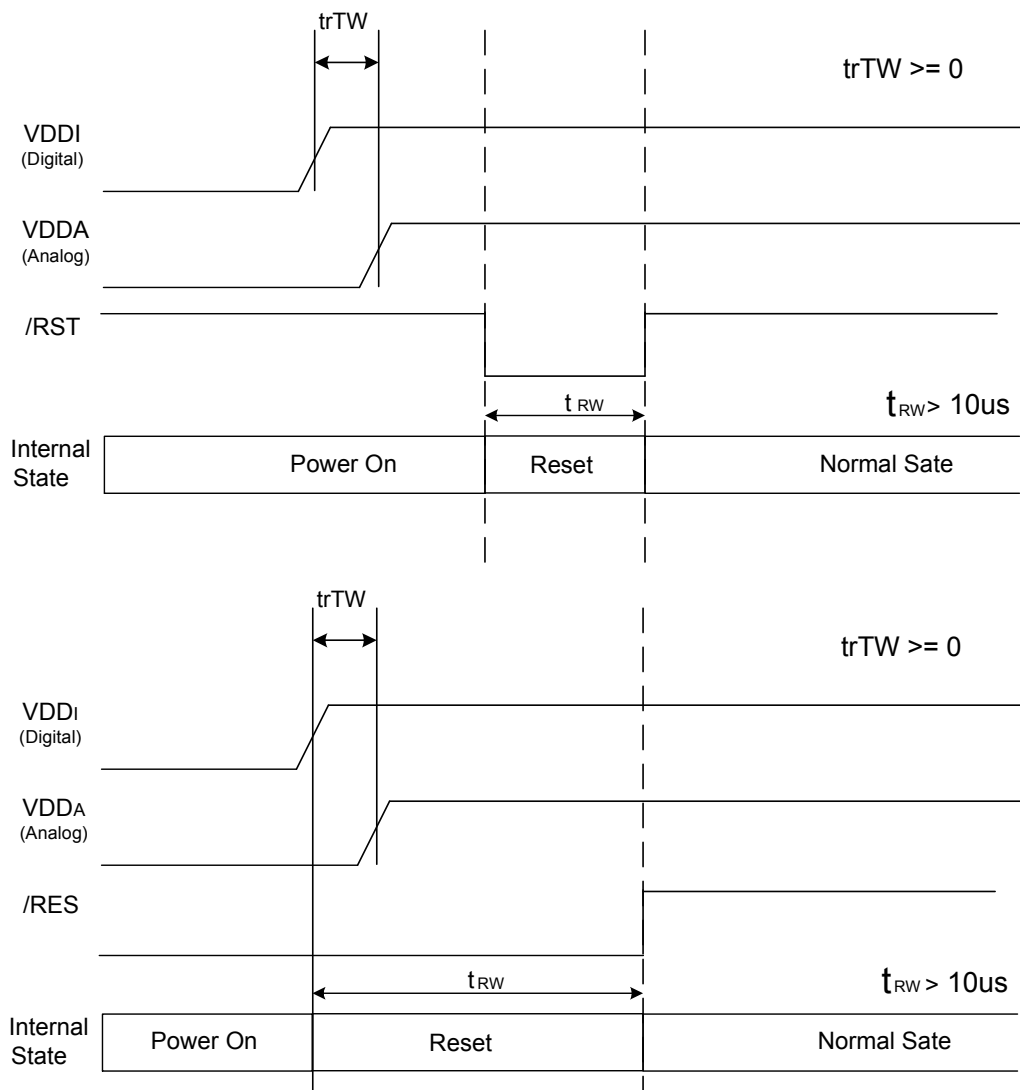
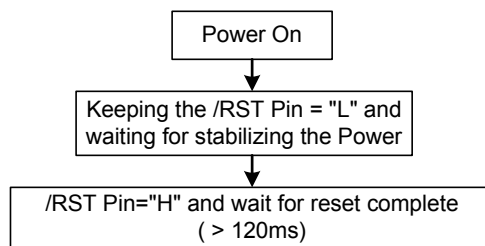
Note:

- 9 bit SPI (3line)
- IF1: IF2: IF3 = 0 : 0 : 1
- CL S=1, using internal colclock
- VDDI operation voltage range 1.65V to 3.0V
- VDD operation voltage range 2.4 V to 3.3 V
- Vop=9~12V

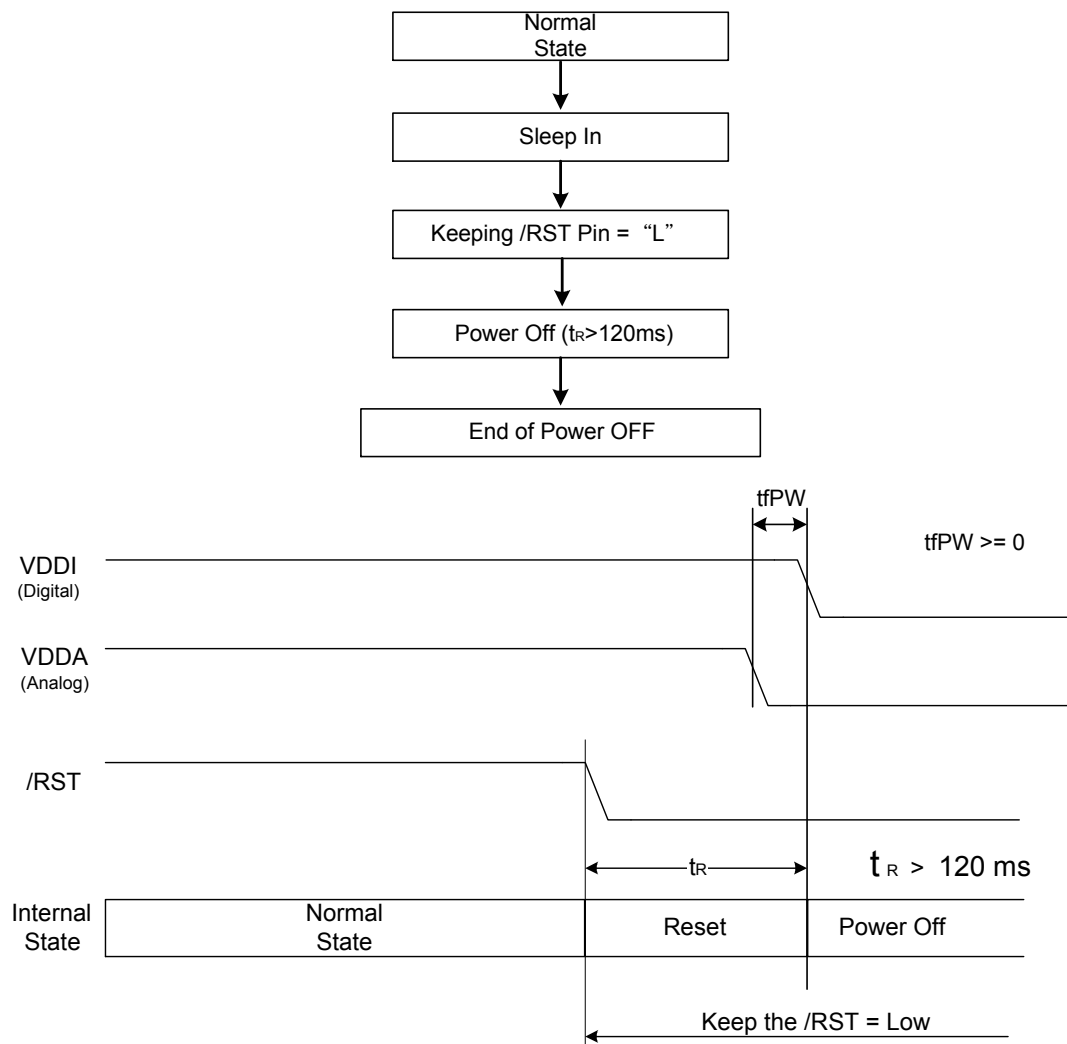
Pin	Function
1	COM4/COM8
2	COM0/COM0
3	Vpp
4	Vpp
5	VDD
6	CL
7	CLS
8	VSS
9	VDD
10	A0
11	RW-WR
12	D0
13	D1
14	D2
15	D3
16	D4
17	D5
18	D6
19	D7
20	D8
21	D9
22	D10
23	D11
24	D12
25	D13
26	D14
27	D15
28	VSS
29	VDD
30	E_RD
31	RST
32	CSEL
33	IF1
34	IF2
35	IF3
36	VSS
37	VDD
38	/CS
39	TCAP
40	VDD
41	VDD
42	VDD1
43	VDD1
44	VSS1
45	VSS1
46	VSS
47	VSS
48	VSS
49	VSS2
50	VSS2
51	VSS4
52	VSS4
53	VDD3
54	VDD3
55	VDD4
56	VDD4
57	VDD5
58	VDD5
59	VDD2
60	VDD2
61	VDD2
62	VREF
63	V0IN
64	V0IN
65	V0S
66	V0OUT
67	V0OUT
68	XV0OUT
69	XV0OUT
70	XV0S
71	XV0IN
72	XV0IN
73	V3OUT
74	V3OUT
75	V3S
76	V3IN
77	V3IN
78	COM95/COM1
79	COM91/COM9



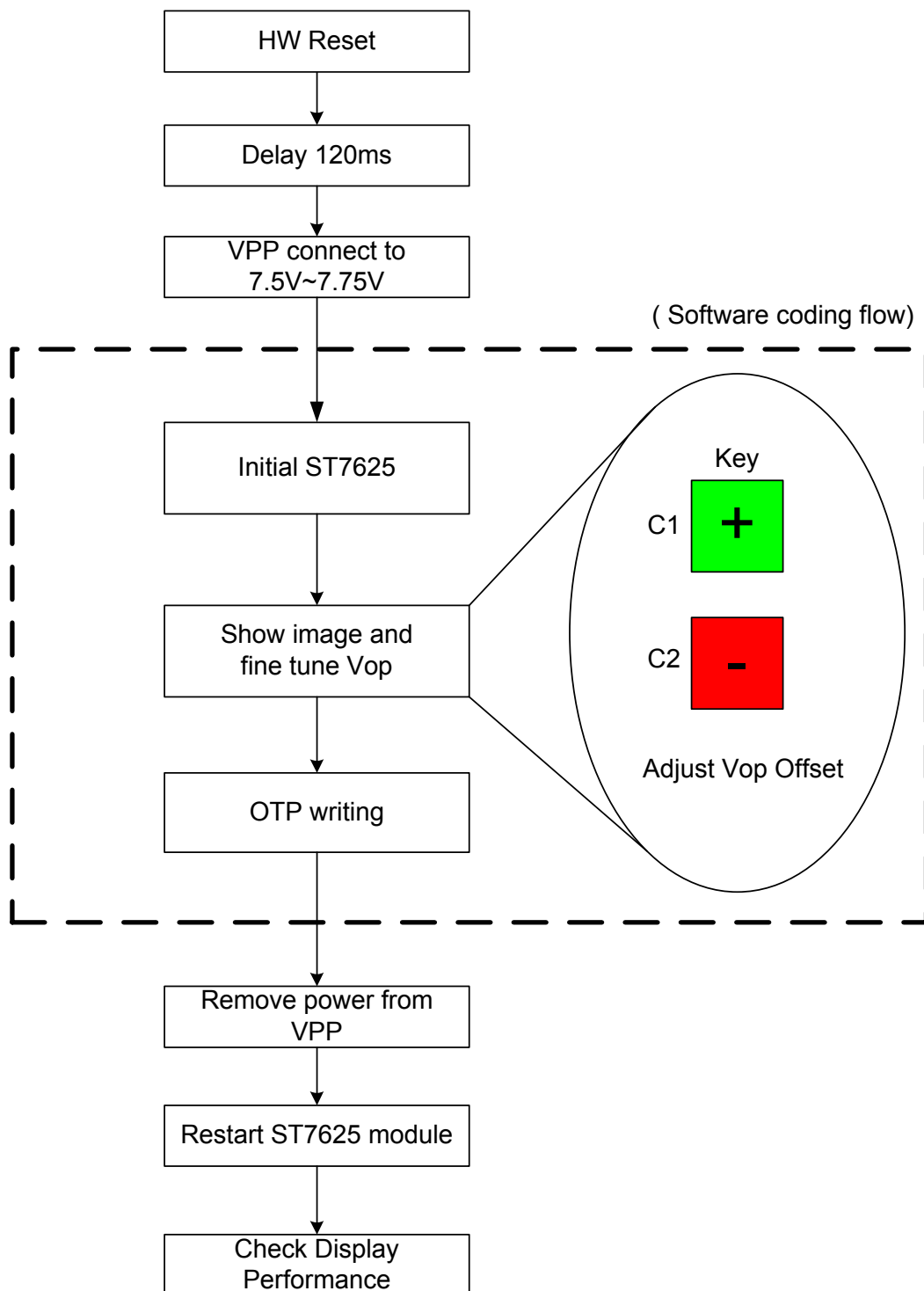
A7 - Power On flow and sequence



A8 - Power off flow and sequence



A9 –OTP Burning Flow:



A10 – Software coding flow

void Initial_LCD_Module(void)

```
{
//-----disable autoread + Manual read once -----
    Write(COMMAND,0xD7);           // Auto Load Set
    Write(DATA,0x1F);              // Auto Load Disable
    Write(COMMAND,0xE0);           // EE Read/write mode
    Write(DATA,0x00);              // Set read mode
    delays(10);                   // Delay 10ms
    Write(COMMAND,0xE3);           // Read active
    delays(20);                   // Delay 20ms
    Write(COMMAND,0xE1);           // Cancel control

//----- Sleep OUT -----
    Write(COMMAND, 0x28 );         // Display Off
    Write(COMMAND, 0x11 );         // Sleep Out
    delays(50);                   // Delay 50ms

//-----Vop setting-----
    Write(COMMAND,0xC0);           //Set Vop by initial Module
    Write(DATA, 0xB9);             //Vop = 11V
    Write(DATA, 0x00);             // base on Module

//-----Set Register-----
    Write(COMMAND,0xC3);           // Bias select
    Write(DATA,0x02);              // 1/10 Bias, base on Module
    Write(COMMAND,0xC4);           // Setting Booster times
    Write(DATA,0x07);              // Booster X 8
    Write(COMMAND,0xC5);           // Booster eff
    Write(DATA,0x01);              // BE = 0x01 (Level 2)
    Write(COMMAND,0xCB);           // Vg with booster x2 control
    Write(DATA,0x01);              // Vg from Vdd2
    Write(COMMAND,0xD0);           // Analog circuit setting
    Write(DATA,0x1D);              //
    Write(COMMAND,0x3A);           // Color mode = 65k
    Write(DATA,0x05);              //
    Write(COMMAND,0x36);           // Memory Access Control //
    Write(DATA,0x08);              //
    Write(COMMAND, 0xB5 );         // N-Line
    Write(DATA, 0x01);             // RST, 2-line inversion

    Write(COMMAND,0xF7 );         // command for temp sensitivity.
    Write(DATA,0x06);             //

    1. Set Gamma table for Module, please refer spec setting.
    2. Set Temp compensation for Module, please refer spec setting.

    Write(COMMAND,0x2A);           // Set COL By Module
    Write(DATA,0x00);              // 0~95
    Write(DATA,0x5F);              //

    Write(COMMAND,0x2B);           // Set Page By Module
    Write(DATA,0x00);              // 0~95
    Write(DATA,0x5F);              //
    Write(COMMAND, 0x29 );         // Display On
}
```

```
//-----Fine tune vop offset-----
void Fine_Tune_Vop(void)
{
    Show_Image(); //Display a image
//----- Display ON -----
    Write(COMMAND, 0x29 ); // Display On
//-----Fine tune Vop offset-----
    Write( COMMAND, 0xC1); //Fine tuning Vop here by command
    or //0xc1(VopOffsetInc),0xc2(VopOffsetDec).
    Write( COMMAND, 0xC2);
Note#1
}
```

```
void OTP_Writing(void)
{
//-----Display OFF-----
    Write(COMMAND, 0x28 ); // Display Off
    Delayms(50); // delay 50ms
//-----OTP writing-----
    Write( COMMAND, 0x00F0 ); // Keep Frame Rate
    Write( DATA, 0x0012 ); //
    Write( DATA, 0x0012 );
    Write( DATA, 0x0012 );
    Write( DATA, 0x0012 );
    Write( COMMAND, 0x00E4 ); //OTP selection
    Write( DATA, 0x0058 ); // Select OTP
    Write( COMMAND, 0x00E5 ); // Set OTP writing setup
    Write( DATA, 0x0009 );
    Write( COMMAND, 0x00E0 ); // Read/write mode setting
    Write( DATA, 0x0020 ); // Set Write mode
    Delayms(100); //Delay 100ms
    Write( COMMAND, 0x00E2 ); // Write active
    Delayms(100); //Delay 100ms
    Write( COMMAND, 0x00E1 );
}
```

Note:

- #1. In this section "+" & "-" key button, please execute Write(COMMAND,0xC1) to increase one step at Vop and execute Write(COMMAND,0xC2) to decrease one step at Vop, if necessary.
- #2. TC is turned on in burning flow. If LCD module is too dark or bright, it's an effect of backlight.
- #3. The OTP function can not be guaranteed after burned over 4 times.

ST7625 Specification Revision History		
Version	Date	Description
0.x		Preliminary version
1.0	2007/2/14	First issue
1.1	2007/5/9	Redefine the programming mechanism of non-volatility memory.
1.2	2007/6/5	1. Add cmd E5 description 2. 8080 interface timing modify
1.3	2007/8/22	Add ST7625-G3 and ST7625-G4 description.
1.4	2008/01	1. Update current consumption table 2. Update logic operating voltage range 3 Modify the voltage range in application note. 4. Remove 256 color 16bits mode
1.5	2008/03	1. Modify description in software coding flow.
1.6	2008/07	1. Modify AC/DC characteristics condition 2. remove CL pin function 3. add read access time and output disable time timing data