Power MOSFET -10 Amps, -20 Volts

P-Channel Enhancement-Mode Single SO-8 Package

Features

- Ultra Low R_{DS(on)}
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Miniature SO-8 Surface Mount Package
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- SO-8 Mounting Information Provided

Applications

 Power Management in Portable and Battery-Powered Products, i.e.: Cellular and Cordless Telephones and PCMCIA Cards

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	-20	Vdc
Gate-to-Source Voltage - Continuous	V _{GS}	±12	Vdc
Thermal Resistance – Junction–to–Ambient (Note 1.) Total Power Dissipation @ T _A = 25°C Continuous Drain Current @ 25°C Continuous Drain Current @ 70°C Maximum Operating Power Dissipation Maximum Operating Drain Current	R _{0JA} P _D I _D I _D P _D	50 2.5 -10 -8.0 0.6 -5.5	°C/W W A A W
Pulsed Drain Current (Note 3.)	I _D I _{DM}	-5.5 -50	A
Thermal Resistance – Junction–to–Ambient (Note 2.) Total Power Dissipation @ T _A = 25°C Continuous Drain Current @ 25°C Continuous Drain Current @ 70°C Maximum Operating Power Dissipation Maximum Operating Drain Current Pulsed Drain Current (Note 3.)	R _{θJA} P _D I _D I _D I _D I _D I _D I _D	80 1.6 -8.8 -6.4 0.4 -4.5 -44	°C/W W A A W A
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C
Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J=25^{\circ}C$ ($V_{DD}=-20$ Vdc, $V_{GS}=-4.5$ Vdc, Peak $I_L=5.0$ Apk, $L=40$ mH, $R_G=25~\Omega$)	E _{AS}	500	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	TL	260	°C

- Mounted onto a 2" square FR-4 Board (1" sq. Cu 0.06" thick single sided), t = 10 seconds.
- Mounted onto a 2" square FR-4 Board (1" sq. Cu 0.06" thick single sided), t = steady state.
- 3. Pulse Test: Pulse Width < 300 $\mu\text{s},$ Duty Cycle < 2%.



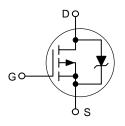
ON Semiconductor®

http://onsemi.com

-10 AMPERES
-20 VOLTS

14 m Ω @ V_{GS} = -4.5 V

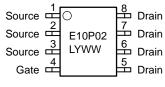
P-Channel





SO-8 CASE 751 STYLE 12

MARKING DIAGRAM & PIN ASSIGNMENT



Top View

E10P02 = Device Code L = Assembly Location

Y = Year WW = Work Week

ORDERING INFORMATION

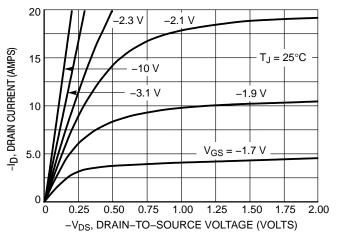
Device	Package	Shipping [†]	
NTMS10P02R2	SO-8	2500/Tape & Reel	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted) (Note 4.)

Characteristic			Min	Тур	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = –250 μAdc) Temperature Coefficient (Positive)			-20 -	_ _12.1		Vdc mV/°C
Temperature Coefficient (Positive) Zero Gate Voltage Drain Current (V _{DS} = -20 Vdc, V _{GS} = 0 Vdc, T _J = 25°C) (V _{DS} = -20 Vdc, V _{GS} = 0 Vdc, T _J = 70°C)			- -	_ _ _	-1.0 -5.0	μAdc
Gate–Body Leakage Current (V _{GS} = -12 Vdc, V _{DS} = 0 Vdc)			_	-	-100	nAdc
Gate-Body Leakage Current (V _{GS} = +12 Vdc, V _{DS} = 0 Vdc)			-	-	100	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage $(V_{DS} = V_{GS}, I_D = -250 \mu Adc)$ Temperature Coefficient (Negative)			-0.6 -	-0.88 2.8	-1.20 -	Vdc mV/°C
Static Drain-to-Source On-State Resistance ($V_{GS} = -4.5 \text{ Vdc}$, $I_D = -10 \text{ Adc}$) ($V_{GS} = -2.5 \text{ Vdc}$, $I_D = -8.8 \text{ Adc}$)			- -	0.012 0.017	0.014 0.020	Ω
Forward Transconductance (V _{DS} = -10 Vdc, I _D = -10 Adc)			_	30	_	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	0/ 40 // 1/ 0 // 1	C _{iss}	-	3100	3640	pF
Output Capacitance	$(V_{DS} = -16 \text{ Vdc}, V_{GS} = 0 \text{ Vdc}, $ f = 1.0 MHz)	C _{oss}	-	1100	1670	
Reverse Transfer Capacitance	,	C _{rss}	-	475	1010	
SWITCHING CHARACTERISTICS (Notes 5. & 6.)					
Turn-On Delay Time		t _{d(on)}	-	25	35	ns
Rise Time	$(V_{DD} = -10 \text{ Vdc}, I_D = -1.0 \text{ Adc}, V_{GS} = -4.5 \text{ Vdc},$	t _r	-	40	65	-
Turn-Off Delay Time	$R_G = 6.0 \Omega$)	t _{d(off)}	-	110	190	
Fall Time		t _f	-	110	190	
Turn-On Delay Time		t _{d(on)}	-	25	-	ns
Rise Time	$(V_{DD} = -10 \text{ Vdc}, I_D = -10 \text{ Adc}, V_{GS} = -4.5 \text{ Vdc},$	t _r	-	100	-	
Turn-Off Delay Time	$R_{GS} = -4.3 \text{ VdC},$ $R_{G} = 6.0 \Omega)$	t _{d(off)}	-	100	-	
Fall Time		t _f	_	125	-	
Total Gate Charge	(V _{DS} = -10 Vdc,	Q _{tot}	_	48	70	nC
Gate-Source Charge	$V_{GS} = -4.5 \text{ Vdc},$	Q _{gs}	-	6.5	_	
Gate-Drain Charge	$I_{D} = -10 \text{ Adc}$	Q _{gd}	-	17	_	
BODY-DRAIN DIODE RATINGS (N	ote 5.)					
Diode Forward On–Voltage	$(I_S = -2.1 \text{ Adc}, V_{GS} = 0 \text{ Vdc})$ $(I_S = -2.1 \text{ Adc}, V_{GS} = 0 \text{ Vdc}, T_J = 125^{\circ}\text{C})$	V _{SD}	- -	-0.72 -0.60	-1.2 -	Vdc
Diode Forward On–Voltage	$(I_S = -10 \text{ Adc}, V_{GS} = 0 \text{ Vdc})$ $(I_S = -10 \text{ Adc}, V_{GS} = 0 \text{ Vdc}, T_J = 125^{\circ}\text{C})$	V _{SD}	- -	-0.90 -0.75	- -	Vdc
Reverse Recovery Time	(1 04 A (1) (2) (1)	t _{rr}	-	65	100	ns
	$(I_S = -2.1 \text{ Adc}, V_{GS} = 0 \text{ Vdc},$ $dI_S/dt = 100 \text{ A/}\mu\text{s})$	t _a	-	25	_	
		t _b	-	40	-	
Reverse Recovery Stored Charge			_	0.075	_	μС

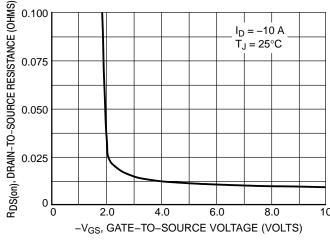
- Handling precautions to protect against electrostatic discharge is mandatory.
 Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.
 Switching characteristics are independent of operating junction temperature.



10 $V_{DS} \ge -10 \text{ V}$ 8.0 -ID, DRAIN CURRENT (AMPS) 6.0 25°C 4.0 $T_J = -55^{\circ}C$ 100°C 2.0 0 6 2.5 0.5 1.0 1.5 2.0 -V_{GS}, GATE-TO-SOURCE VOLTAGE (VOLTS)

Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



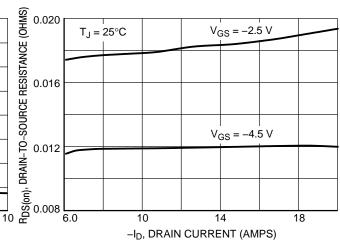
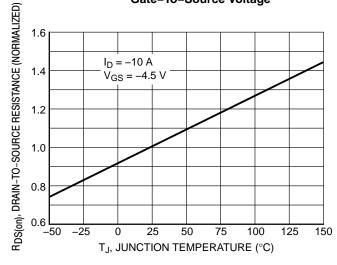


Figure 3. On–Resistance versus Gate–To–Source Voltage

Figure 4. On-Resistance versus Drain Current and Gate Voltage



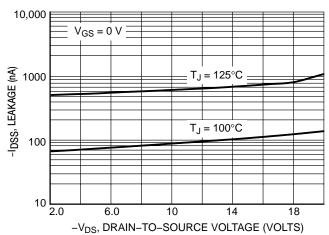
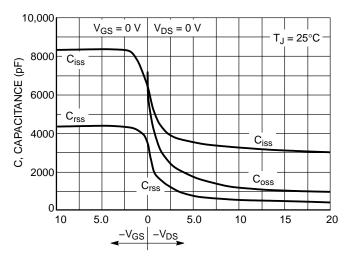


Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-To-Source Leakage Current versus Voltage



GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 7. Capacitance Variation

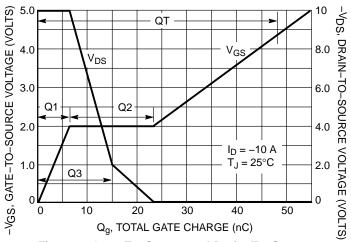


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

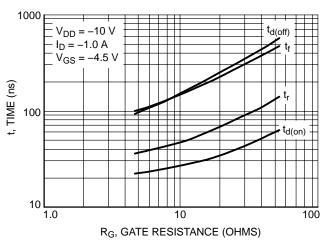


Figure 9. Resistive Switching Time Variation versus Gate Resistance

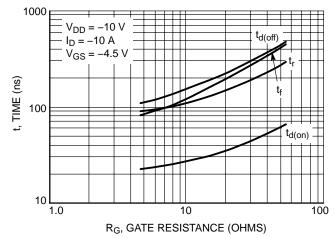


Figure 10. Resistive Switching Time Variation versus Gate Resistance

DRAIN-TO-SOURCE DIODE CHARACTERISTICS

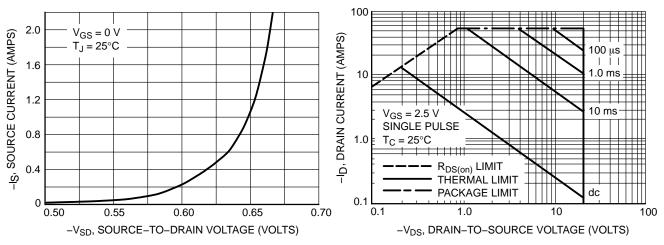


Figure 11. Diode Forward Voltage versus Current

Figure 12. Maximum Rated Forward Biased Safe Operating Area

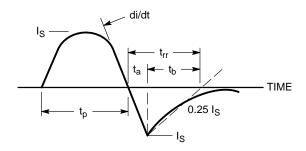


Figure 13. Diode Reverse Recovery Waveform

TYPICAL ELECTRICAL CHARACTERISTICS

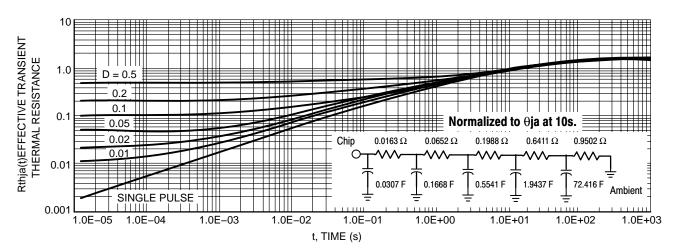
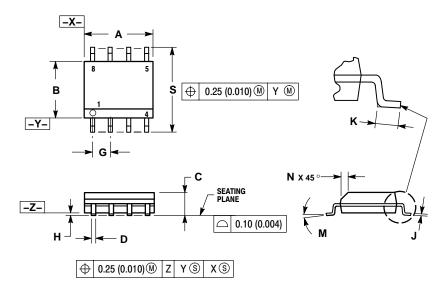


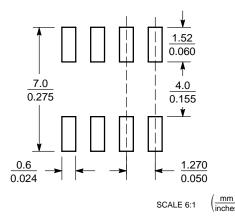
Figure 14. Thermal Response

PACKAGE DIMENSIONS

SO-8 CASE 751-07 ISSUE AA



SOLDERING FOOTPRINT*



*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI
 Y14 5M 1982
- 2. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE J. 127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
- 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07

	MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	4.80	5.00	0.189	0.197	
В	3.80	4.00	0.150	0.157	
С	1.35	1.75	0.053	0.069	
D	0.33	0.51	0.013	0.020	
G	1.27 BSC		0.050 BSC		
Н	0.10	0.25	0.004	0.010	
J	0.19	0.25	0.007	0.010	
K	0.40	1.27	0.016	0.050	
M	0 °	8 °	0 °	8 °	
N	0.25	0.50	0.010	0.020	
S	5.80	6.20	0.228	0.244	

STYLE 12:

- PIN 1. SOURCE
 - SOURCE
 SOURCE
 - SOURCE
 GATE
 - 5 DRAIN
 - 6. DRAIN
 - 7. DRAIN
 - 8. DRAIN

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