Power MOSFET

-20 V, -7.7 A, μCool™ Single P-Channel, 2x2 mm, WDFN Package

Features

- WDFN Package Provides Exposed Drain Pad for Excellent Thermal Conduction
- 2x2 mm Footprint Same as SC-88 Package
- Lowest R_{DS(on)} Solution in 2x2 mm Package
- 1.5 V R_{DS(on)} Rating for Operation at Low Voltage Logic Level Gate Drive
- Low Profile (< 0.8 mm) for Easy Fit in Thin Environments
- This is a Pb-Free Device

Applications

- DC-DC Converters (Buck and Boost Circuits)
- Optimized for Battery and Load Management Applications in Portable Equipment such as, Cell Phones, PDA's, Media Players, etc.
- High Side Load Switch

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	-20	V
Gate-to-Source Voltage	ge		V_{GS}	±8.0	V
Continuous Drain	Steady	T _A = 25°C	I _D	-5.8	Α
Current (Note 1)	State $T_A = 85^{\circ}C$		-4.4		
	t ≤ 5 s	T _A = 25°C		-7.7	
Power Dissipation (Note 1)	Steady State	T _A = 25°C	P _D	1.9	W
	t ≤ 5 s			3.3	
Continuous Drain		T _A = 25°C	I _D	-3.5	Α
Current (Note 2)	Steady	T _A = 85°C		-2.5	
Power Dissipation (Note 2)	State	T _A = 25°C	P _D	0.7	W
Pulsed Drain Current	t _p = 10 μs		I _{DM}	-23	Α
Operating Junction and Storage Temperature			T _J , T _{STG}	–55 to 150	°C
Source Current (Body Diode) (Note 2)			I _S	-2.8	Α
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

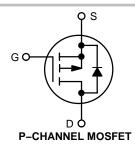
- Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
- Surface Mounted on FR4 Board using the minimum recommended pad size, (30 mm², 2 oz Cu).



ON Semiconductor®

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V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX (Note 1)
	40 mΩ @ –4.5 V	
–20 V	50 mΩ @ –2.5 V	_7.7 A
	75 mΩ @ –1.8 V	1.77
	200 mΩ @ –1.5 V	



MARKING DIAGRAM WDFN6 CASE 506AP 2 3 J8M 5 4

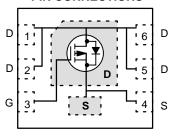
J8 = Specific Device Code

M = Date Code

= Pb–Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping [†]
NTLJS3113PT1G	WDFN6 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 3)	$R_{ heta JA}$	65	
Junction–to–Ambient – $t \le 5$ s (Note 3)	$R_{ heta JA}$	38	°C/W
Junction-to-Ambient - Steady State Min Pad (Note 4)	$R_{ heta JA}$	180	

- Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
 Surface Mounted on FR4 Board using the minimum recommended pad size (30 mm², 2 oz Cu).

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Test Conditions		Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V, } I_D = -250 \mu\text{A}$		-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	$I_D = -250 \mu\text{A}$, Ref to 25°C			-10.1		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16 V, V _{GS} = 0 V	$T_J = 25^{\circ}C$			-1.0	μΑ
			$T_J = 85^{\circ}C$			-10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0 V$, $V_{GS} = \pm$	8.0 V			±1.0	μΑ
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}$, $I_D = -2$	50 μΑ	-0.45	-0.67	-1.0	V
Negative Gate Threshold Temperature Coefficient	V _{GS(TH)} /T _J				2.68		mV/°C
Drain-to-Source On-Resistance	R _{DS(on)}	$V_{GS} = -4.5, I_D = -3$	3.0 A		32	40	mΩ
		$V_{GS} = -2.5, I_D = -3$	3.0 A		44	50	
		$V_{GS} = -1.8, I_D = -2$			67	75	
		$V_{GS} = -1.5, I_D = -1.5$	1.8 A		90	200	
Forward Transconductance	9FS	$V_{DS} = -16 \text{ V}, I_{D} = -$	-3.0 A		5.9		S
CHARGES, CAPACITANCES AND GA	ATE RESISTAN	CE					
Input Capacitance	C _{ISS}				1329		pF
Output Capacitance	C _{OSS}	$V_{GS} = 0 \text{ V, f} = 1.0 \text{ MHz,}$ $V_{DS} = -16 \text{ V}$			213		1
Reverse Transfer Capacitance	C _{RSS}				120		1
Total Gate Charge	Q _{G(TOT)}	$V_{GS} = -4.5 \text{ V}, V_{DS} = -16 \text{ V},$ $I_{D} = -3.0 \text{ A}$			13	15.7	nC
Threshold Gate Charge	Q _{G(TH)}				1.5		1
Gate-to-Source Charge	Q_{GS}				2.2		1
Gate-to-Drain Charge	Q_{GD}				2.9		1
Gate Resistance	R_{G}				14.4		Ω
SWITCHING CHARACTERISTICS (No	ote 6)						
Turn-On Delay Time	t _{d(ON)}				6.9		ns
Rise Time	t _r	$V_{GS} = -4.5 \text{ V}, V_{DD} =$	–10 V,		17.5		1
Turn-Off Delay Time	t _{d(OFF)}	$I_D = -3.0 \text{ A}, R_G = 3.0 \Omega$			60		1
Fall Time	t _f				56.5		1
DRAIN-SOURCE DIODE CHARACTE	RISTICS				•		-
Forward Recovery Voltage	V_{SD}	$T_J = 25^{\circ}$	$T_J = 25^{\circ}C$		-0.78	-1.2	.,
-		$V_{GS} = 0 \text{ V, IS} = -1.0 \text{ A}$	T _J = 125°C		-0.67		V
Reverse Recovery Time	t _{RR}				70.8	106	1
Charge Time	ta	$V_{GS} = 0 \text{ V, } d_{ISD}/d_t = 100 \text{ A/}\mu\text{s,} \\ I_S = -1.0 \text{ A}$			14.3		ns
Discharge Time	t _b				56.4		1
Reverse Recovery Time	Q_{RR}				44		nC

- 5. Pulse Test: Pulse Width \leq 300 $\mu s,$ Duty Cycle \leq 2%.
- 6. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

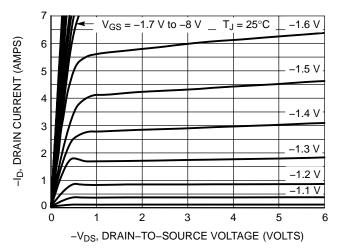


Figure 1. On-Region Characteristics

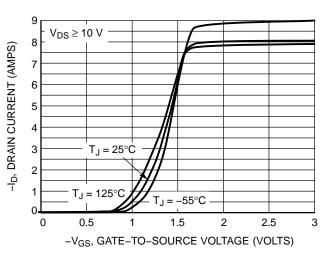


Figure 2. Transfer Characteristics

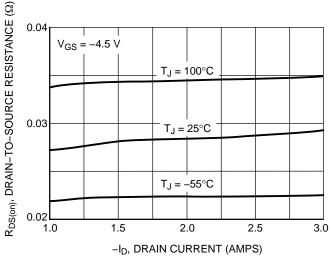


Figure 3. On-Resistance versus Drain Current

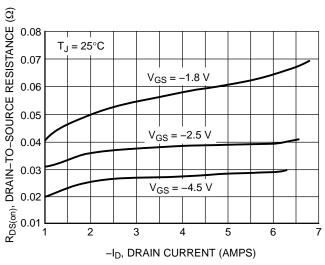


Figure 4. On–Resistance versus Drain Current and Gate Voltage

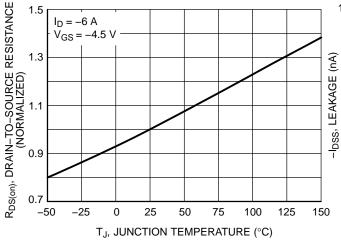


Figure 5. On–Resistance Variation with Temperature

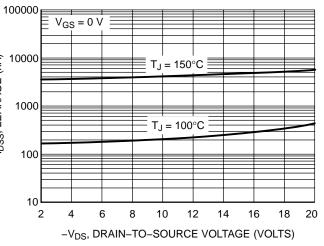
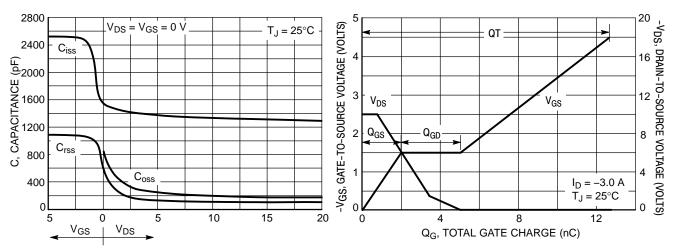


Figure 6. Drain-to-Source Leakage Current versus Voltage

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)



GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 7. Capacitance Variation

Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

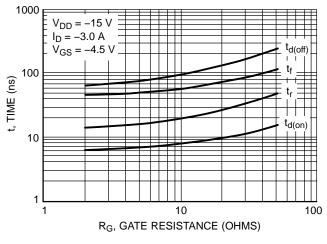


Figure 9. Resistive Switching Time Variation versus Gate Resistance

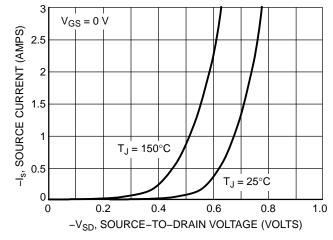


Figure 10. Diode Forward Voltage versus Current

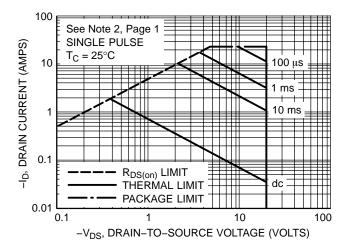


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL PERFORMANCE CURVES ($T_J = 25^{\circ}C$ unless otherwise noted)

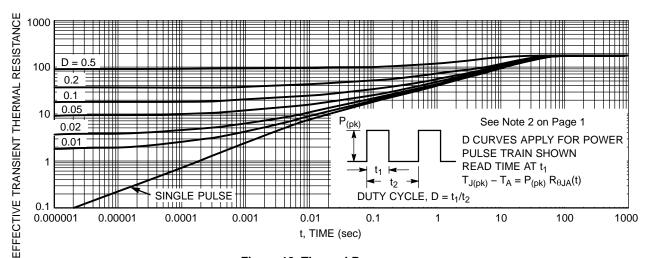
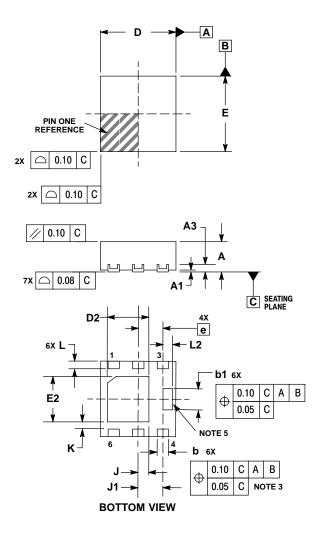


Figure 12. Thermal Response

PACKAGE DIMENSIONS

WDFN6

CASE 506AP-01 **ISSUE A**

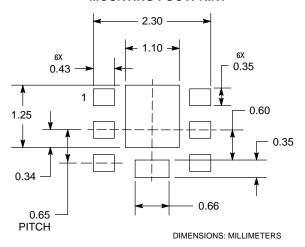


- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETERS.
- 3. DIMENSION & APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL.
- 1 COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

 CENTER TERMINAL LEAD IS OPTIONAL TERMINAL LEAD IS CONNECTED TO TERMINAL LEAD # 4.
- 6. PINS 1, 2, 5 AND 6 ARE TIED TO THE FLAG.

	MILLIMETERS			
DIM	MIN	MAX		
Α	0.70	0.80		
A1	0.00	0.05		
A3	0.20	REF		
b	0.25	0.35		
b1	0.51	0.61		
D	2.00 BSC			
D2	1.00	1.20		
E	2.00 BSC			
E2	1.10	1.30		
е	0.65 BSC			
K	0.15 REF			
L	0.20	0.30		
L2	0.20	0.30		
J	0.27 REF			
J1	0.65 REF			

SOLDERMASK DEFINED **MOUNTING FOOTPRINT**



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