NST30010MXV6T1G

Dual Matched General Purpose Transistor

PNP Matched Pair

These transistors are housed in an ultra−small SOT563 package ideally suited for portable products. They are assembled to create a pair of devices highly matched in all parameters, eliminating the need for costly trimming. Applications are Current Mirrors; Differential, Sense and Balanced Amplifiers; Mixers; Detectors and Limiters.

Features

- Current Gain Matching to 10%
- Base−Emitter Voltage Matched to 2 mV
- Drop−In Replacement for Standard Device
- These are Pb−Free Devices

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	−30	V
Collector−Base Voltage	V_{CBO}	−30	V
Emitter−Base Voltage	V_{EBO}	−5.0	V
Collector Current − Continuous	I_C	−100	mAdc

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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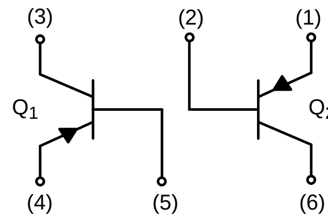
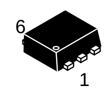
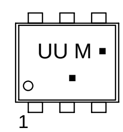




SOT−563
CASE 463A
PLASTIC

MARKING DIAGRAMS



UU = Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NST30010MXV6T1G	SOT−563 (Pb−Free)	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Characteristic	Parameter	Symbol	One Device Heated	Both Devices Heated	Unit
Total Device Dissipation, T_A = 25°C (Note 1) Derate above 25°C (Note 1) T_A = 25°C (Note 2) Derate above 25°C (Note 2)	Two Devices Heated Total Package	P_D	 357 2.9 429 3.4	 500 (250 ea) 4.0 661 (331 ea) 5.3	 mW mW/°C mW mW/°C
Thermal Resistance Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2)	One Heated Device	$R_{\theta JA}$	 350 291	 250 189	°C/W
Thermal Resistance Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2)	Unheated Device Heated by Heated Device	Ψ_{JA}	 149 88	 – –	°C/W
Thermal Resistance Junction-to-Lead (Note 1) Junction-to-Lead (Note 2)	Lead Attached to Heated Device	Ψ_{JL}	 128 152	 76 85	°C/W
Thermal Resistance Junction-to-Lead (Note 1) Junction-to-Lead (Note 2)	Heated Device Heating Lead Attached to Unheated Device	Ψ_{JL}	 224 222	 – –	°C/W
Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +150		°C

1. PCB with 51 square millimeter of 2 oz (0.070mm thick) copper heat spreading connected to package leads. Mounted on a FR4 PCB 76x76x1.5mm Single layer traces. Natural convection test according to JEDEC 51.
2. PCB with 250 square millimeter of 2 oz (0.070mm thick) copper heat spreading connected to package leads. Mounted on a FR4 PCB 76x76x1.5mm Single layer traces. Natural convection test according to JEDEC 51.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Breakdown Voltage, (I_C = −10 mA)	$V_{(BR)CEO}$	−30	–	–	V
Collector−Emitter Breakdown Voltage, (I_C = −10 μA, V_{EB} = 0)	$V_{(BR)CES}$	−30	–	–	V
Collector−Base Breakdown Voltage, (I_C = −10 μA)	$V_{(BR)CBO}$	−30	–	–	V
Emitter−Base Breakdown Voltage, (I_E = −1.0 μA)	$V_{(BR)EBO}$	−5.0	–	–	V
Collector Cutoff Current (V_{CB} = −30 V) (V_{CB} = −30 V, T_A = 150°C)	I_{CBO}	– –	– –	−15 −4.0	nA μA
ON CHARACTERISTICS					
DC Current Gain (I_C = −10 μA, V_{CE} = −5.0 V) (I_C = −2.0 mA, V_{CE} = −5.0 V) (I_C = −2.0 mA, V_{CE} = −5.0 V) (Note 3)	h_{FE} $h_{FE(1)}/h_{FE(2)}$	 270 420 0.9	 – 520 1.0	 – 800 –	–
Collector−Emitter Saturation Voltage (I_C = −10 mA, I_B = −0.5 mA) (I_C = −100 mA, I_B = −5.0 mA)	$V_{CE(sat)}$	 – –	 – –	 −0.30 −0.60	V
Base−Emitter Saturation Voltage (I_C = −10 mA, I_B = −1.0 mA) (I_C = −100 mA, I_B = −10 mA)	$V_{BE(sat)}$	 – –	 −0.75 −0.90	 – –	V
Base−Emitter On Voltage (I_C = −2.0 mA, V_{CE} = −5.0 V) (I_C = −10 mA, V_{CE} = −5.0 V) (I_C = −2.0 mA, V_{CE} = −5.0 V) (Note 4)	$V_{BE(on)}$ $V_{BE(1)} – V_{BE(2)}$	 −0.60 – –	 – – 1.0	 −0.75 −0.82 2.0	V mV
SMALL−SIGNAL CHARACTERISTICS					
Current−Gain − Bandwidth Product, (I_C = −10 mA, V_{CE} = −5 Vdc, f = 100 MHz)	f_T	100	–	–	MHz
Output Capacitance, (V_{CB} = −10 V, f = 1.0 MHz)	C_{ob}	–	–	4.5	pF
Noise Figure, (I_C = −0.2 mA, V_{CE} = −5 Vdc, R_S = 2 kΩ, f = 1 kHz, BW = 200Hz)	NF	–	–	10	dB

3. $h_{FE(1)}/h_{FE(2)}$ is the ratio of one transistor compared to the other transistor within the same package. The smaller h_{FE} is used as numerator.
4. $V_{BE(1)} − V_{BE(2)}$ is the absolute difference of one transistor compared to the other transistor within the same package.

TYPICAL CHARACTERISTICS

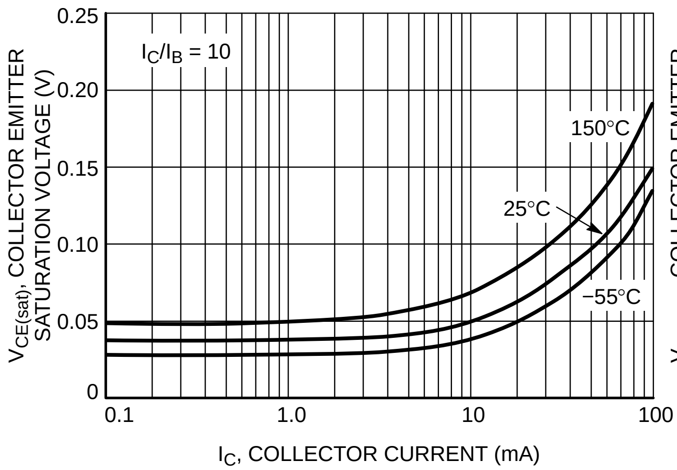


Figure 1. Collector Emitter Saturation Voltage vs. Collector Current

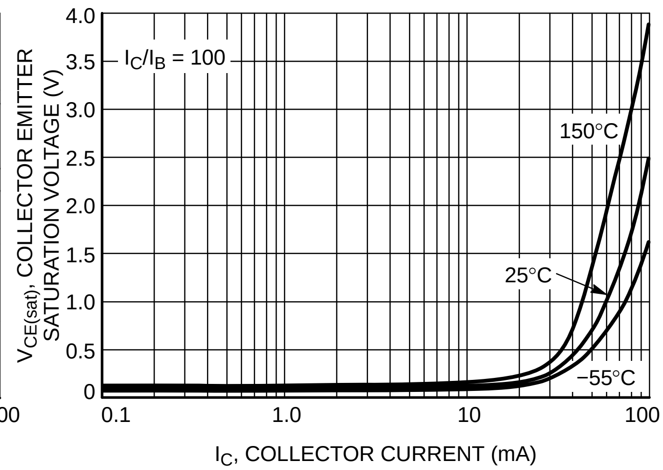


Figure 2. Collector Emitter Saturation Voltage vs. Collector Current

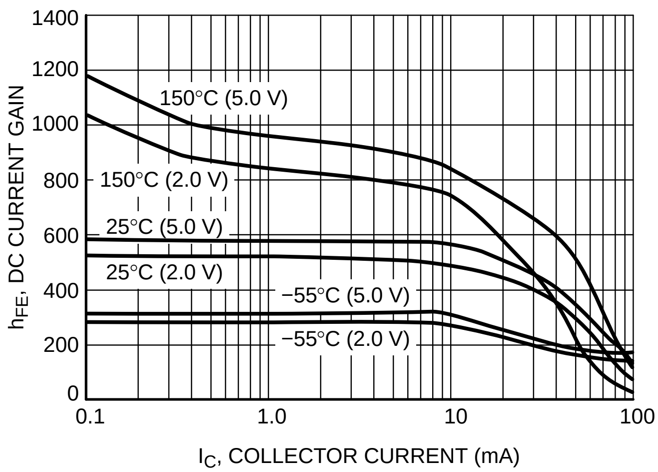


Figure 3. DC Current Gain vs. Collector Current

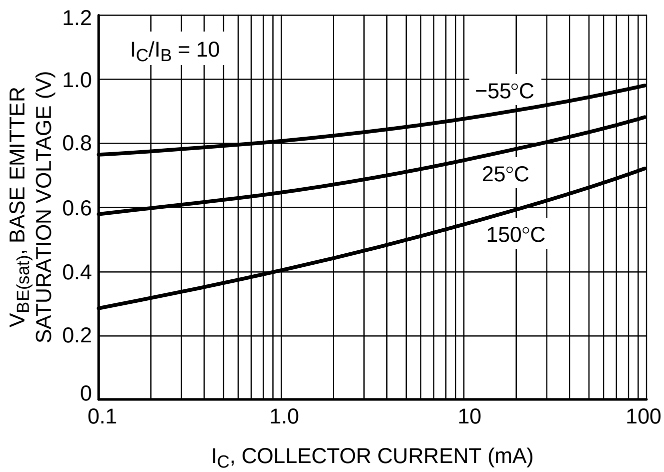


Figure 4. Base Emitter Saturation Voltage vs. Collector Current

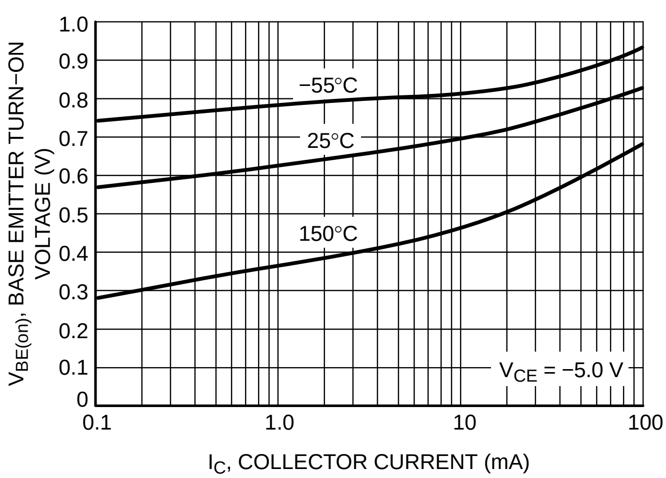


Figure 5. Base Emitter Turn−On Voltage vs. Collector Current

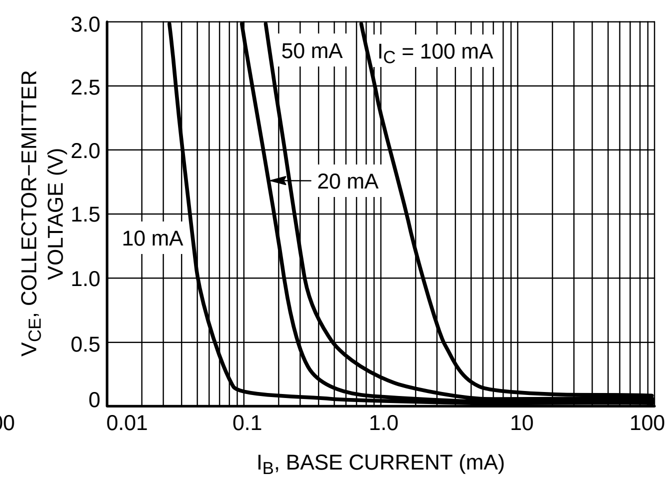


Figure 6. Saturation Region @ 25°C

TYPICAL CHARACTERISTICS

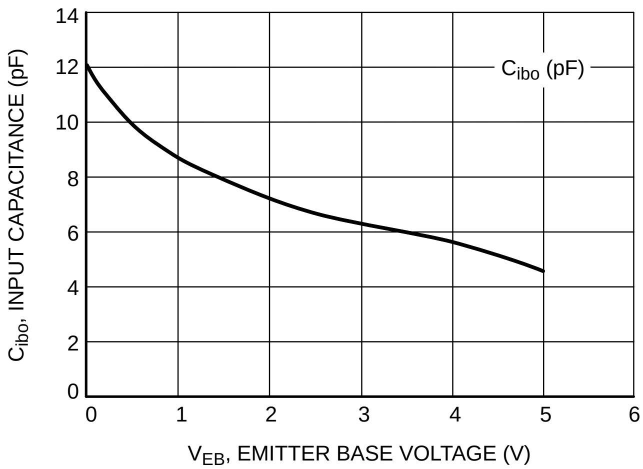


Figure 7. Input Capacitance

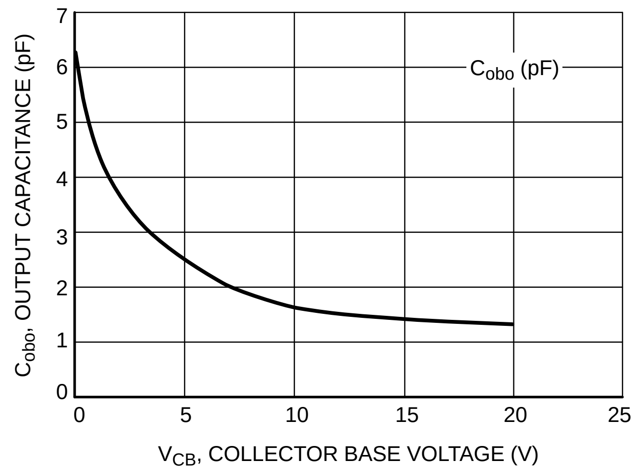
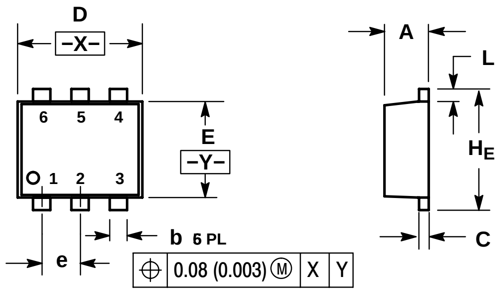


Figure 8. Output Capacitance

PACKAGE DIMENSIONS

SOT−563, 6 LEAD
CASE 463A−01
ISSUE F

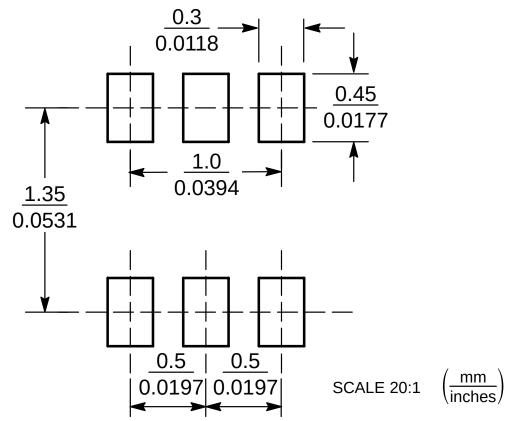


STYLE 1:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.021	0.023
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.08	0.12	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.062	0.066
E	1.10	1.20	1.30	0.043	0.047	0.051
e		0.5 BSC			0.02 BSC	
L	0.10	0.20	0.30	0.004	0.008	0.012
H_E	1.50	1.60	1.70	0.059	0.062	0.066

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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